Upgrade to the Belle II Vertex Detector with CMOS pixel sensors

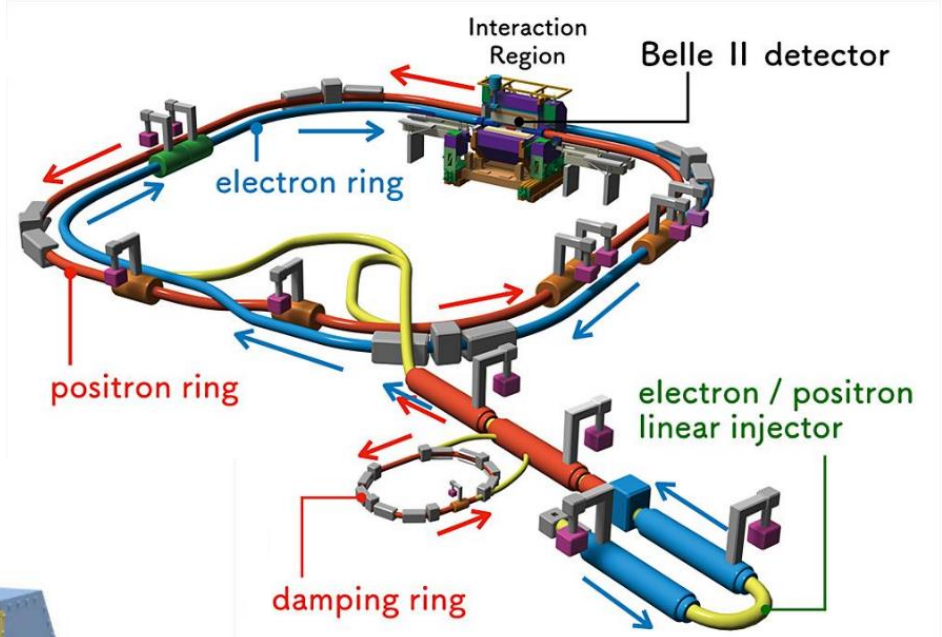
Maximilian Babeluk

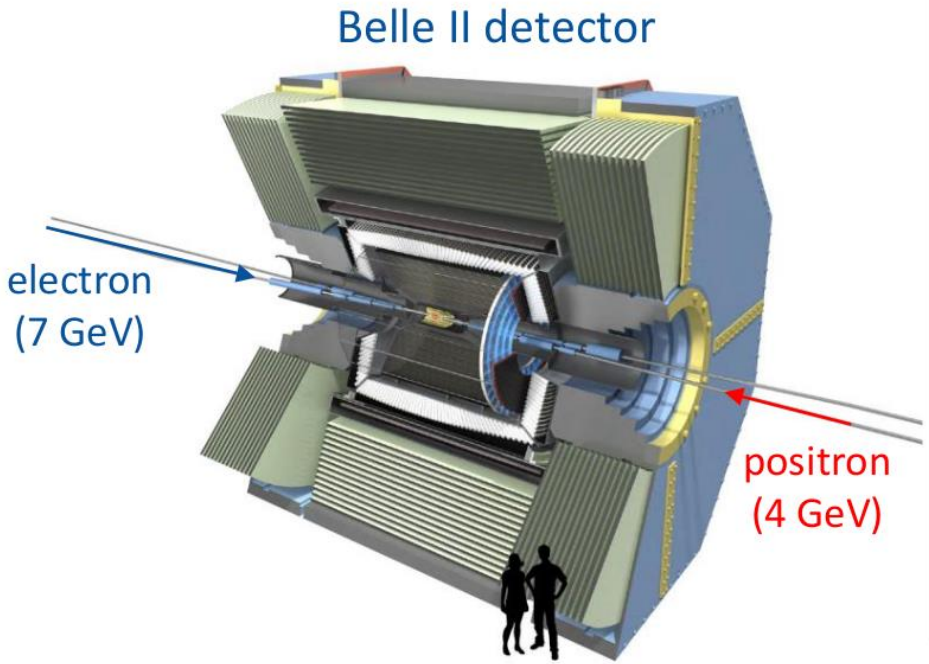
on behalf of the Belle II VXD upgrade collaboration

Belle II and SuperKEKB

Belle II experiment at the SuperKEKB collider

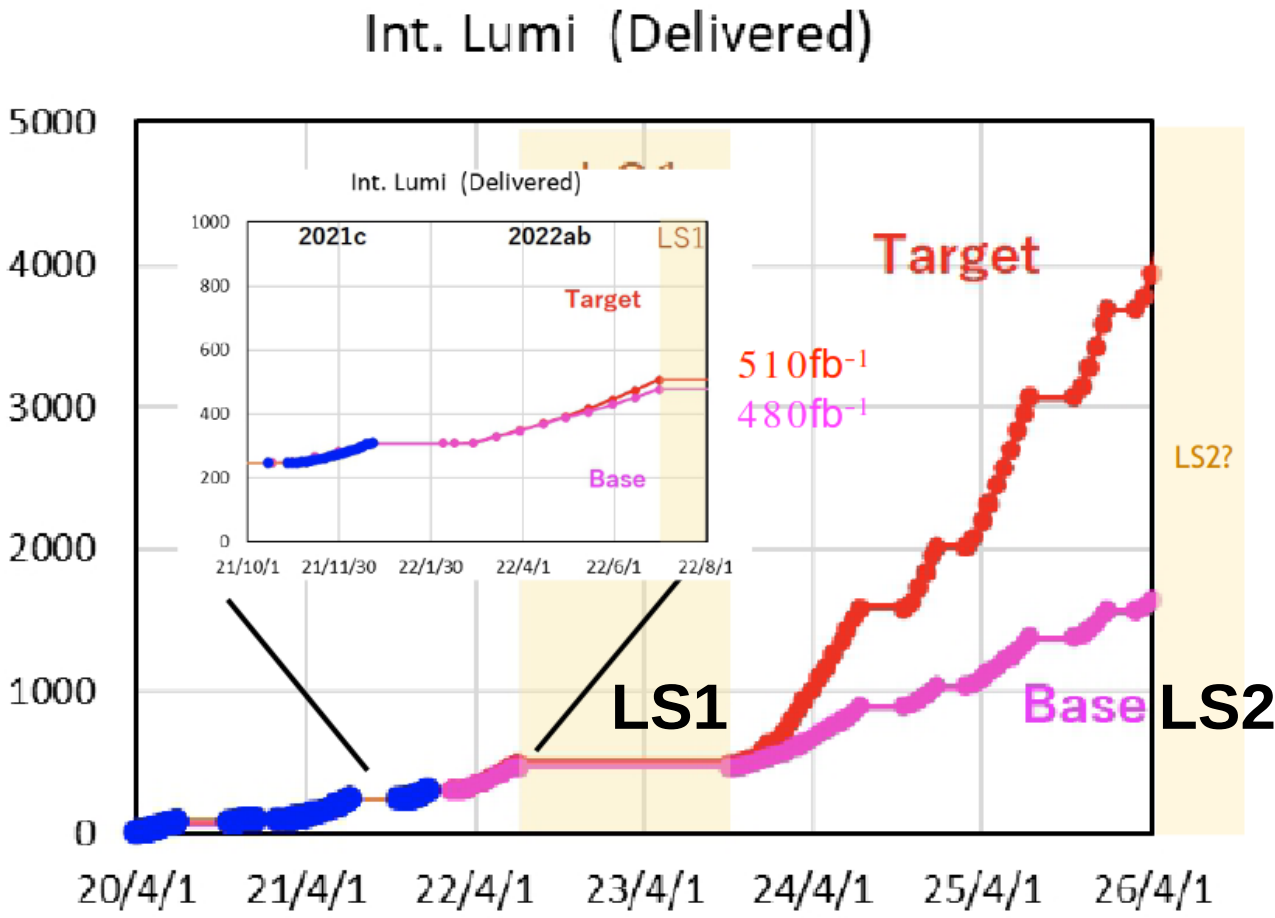
- Asymmetric $e^+ - e^-$ collisions at $\sqrt{s} = 10.58\,GeV$
- Luminosity-frontier experiment, exploring new physics
- Record peak luminosity $3.81 * 10^{34}\ cm^{-2}s^{-1}$
- Path to reach $2 * 10^{35}\ cm^{-2}s^{-1}$ identified
- Target of $6 * 10^{35}\ cm^{-2}s^{-1}$





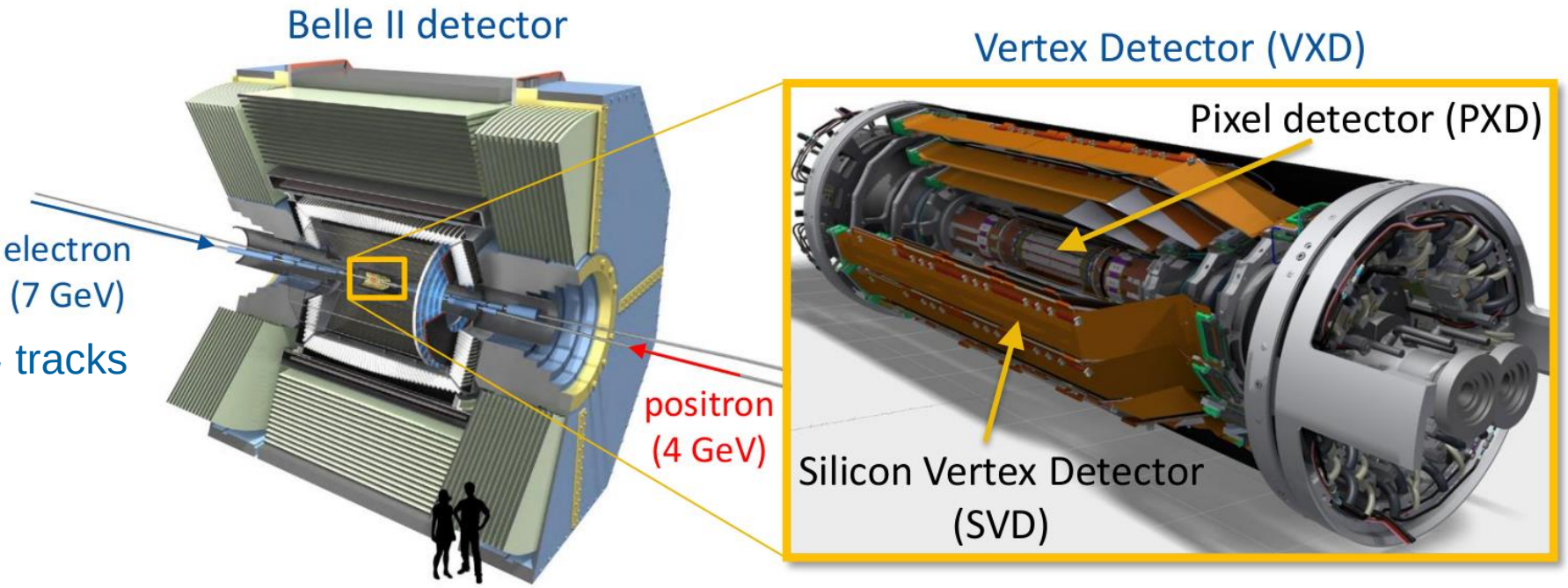
Overview and Upgrade Timeline

- Long Shutdown 1 (2022/23)
  - Exchange of pixel detector (PXD)
  - TOP-PMT replacement
- Long Shutdown 2 (2026/27)
  - SuperKEKB upgrade foreseen
  - Vertex detector upgrade
- Only few years till then
  - Need to utilize currently available technologies
- Several different options/technologies for a major upgrade of the vertex detector under discussion



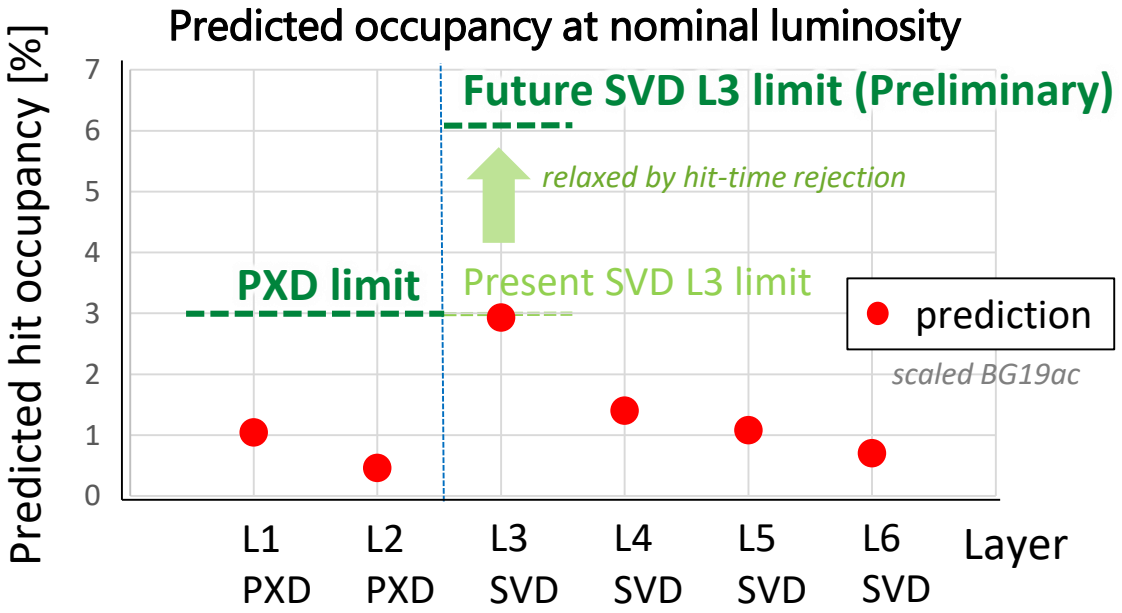
Current Belle II Vertex Detector

- 2 inner layers of Pixel Detector (PXD):
  - DEPFET sensor, 50 µm x 55-85 µm pixels
  - ~15 µm spatial resolution
  - 20 µs integration time
  - 0.2%X_0 per layer
  - Layer 2 currently only partially installed
  - Replacement of full PXD planned for 2023
- 4 outer layers of Silicon Vertex Detector (SVD):
  - Double-side silicon strip (DSSD) detector
  - ~12/25 µm spatial resolution
  - ~3 ns timing resolution
  - 0.7%X_0 per layer
- Roles of Vertex detector
  - Determine vertex position
  - Standalone tracking
  - PID using dE/dx for low p_T tracks



Vertex Detector Upgrade Motivation

- Limitations of current VXD
  - Tolerance for beam-induced background (BG)
    - Predicted occupancy in L3 will be about 3%, which is basically the limit for efficient tracking
    - Limit can be relaxed to 6% occupancy by hit-time reconstruction and BG rejection
    - Difficult to perform accurate BG prediction
    - Margin is small
  - Level 1 trigger latency
    - Belle II trigger latency is limited to 5 μs by SVD
    - Limited depth of APV25 trigger buffer
  - Tracking and vertexing performance
    - Tracking performance in low-pt limited by material budget
    - Room to improve vertex resolution with better hit position resolution
    - Improvement in KS vertexing desirable



K. Nakamura, Vertex 2021

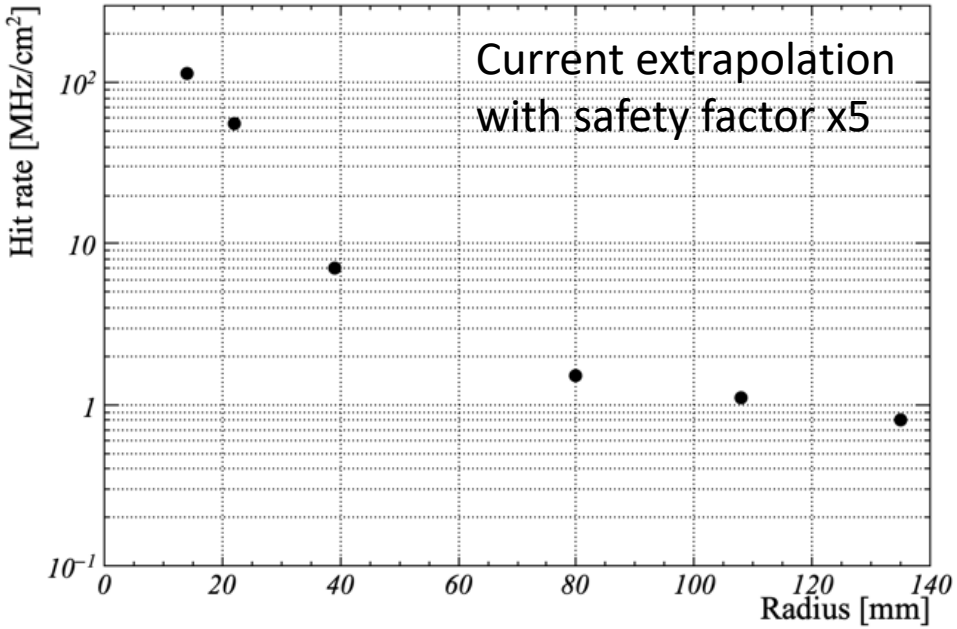
Vertex Detector Upgrade Requirements

Requirements

Radius range: R	14 – 135 mm (**)
Tracking & Vertexing performance at least as good as current VXD	
Single point resolution(*)	< 15 um
Total material budget	< (2*0.2% + 4*0.7%) X_0
Robustness against radiation environment current extrapolation with safety factor x5	
Hit rate(*)	~ 120 MHz/cm^2
Total Ionizing Dose(*)	~ 10 Mrad/year
NIEL fluence(*)	~ 5.0 × 10^{13} n_{eq}/cm^2/year

(*) requirement for the innermost layer (R=14mm)
(**) Optionally, we may include also the CDC inner region (135<R<240mm)

Required hit rate tolerance vs. Radius



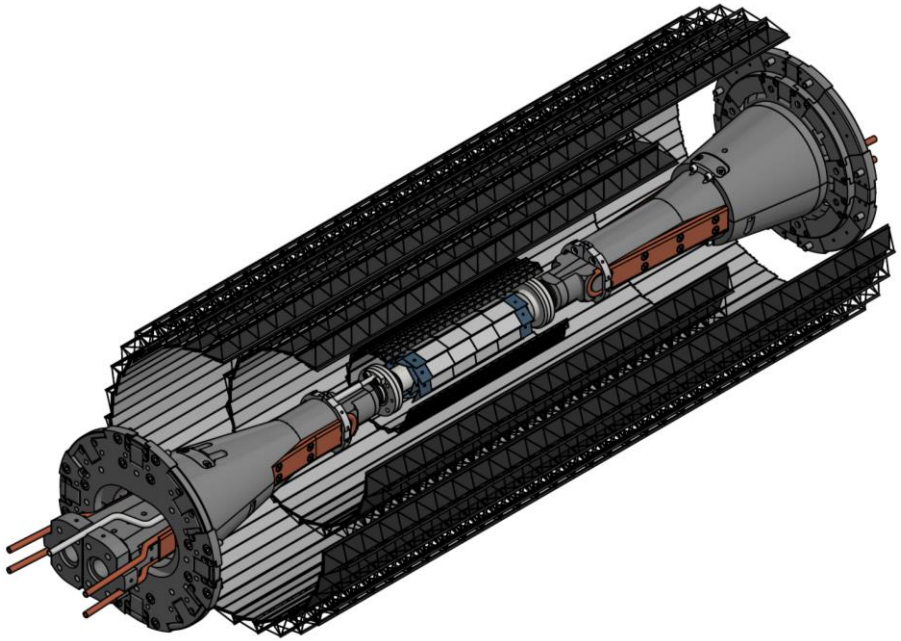
- Additional preferable improvements
  - Impact parameter resolution
  - Tracking performance for low-p_T tracks
  - Longer trigger latency (>5μs)
  - Capability of Level-1 trigger creation

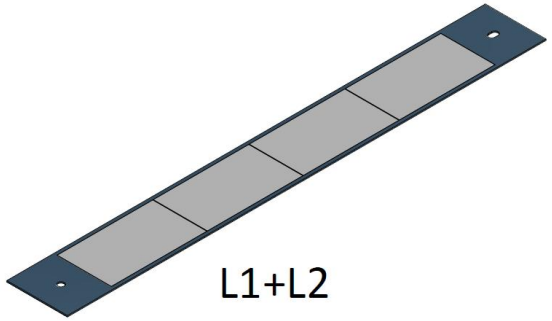
Vertex Detector Upgrade Options

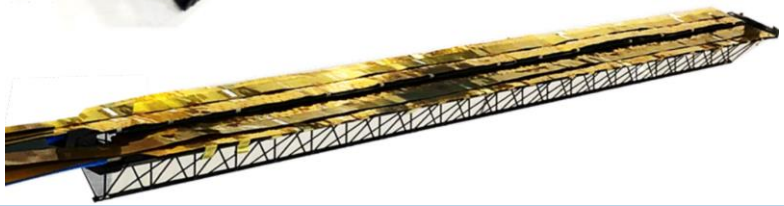
- Several sensor technologies and concepts under discussion, R&D ongoing
  - **Thin DSSD sensor**
    - DSSDs with 140µm thickness and fine pitch (~85µm) on both sides
    - Dedicated front-end ASIC (SNAP128A) with lower noise, binary readout and long buffer for larger trigger latency
    - Target: outer layers (L3-L5)
  - **DEPFET pixel sensor**
    - Improvement of currently used pixel detectors, higher gain, faster ASICs
    - Target: inner layers (L1,L2)
  - **Silicon-on-isolator pixel (SOIPIX) sensor**
    - CMOS circuit produced on silicon wafer isolated by a buried oxide (BOX) layer
    - Fully depleted sensor, fast signal, good SNR
    - Dual Timer Pixel (DuTiP) concept: alternate operation of two timers allows detect next particle hit before the previous one is red out.
  - **Depleted monolithic active pixels sensors** (DMAPS)
    - Pixel sensor in CMOS technology
    - Based on TJ-Monopix2 R&D
    - Target: full CMOS Vertex Detector (Belle II VTX)

CMOS VTX Concept

- 5 straight DMAPS layers
  - Radii: ~14, 22, 39, 90, 140 mm
- Ladder / stave design
  - Based on ALICE ITS2 design
  - Chips are identical in all layers, but the ladder / stave concept is different depending on the layer (L1 is 12 cm long, L5 is 65 cm long)
  - **L1+L2 (iVTX):** All silicon ladders, air cooling, services out of the acceptance.
  - **L3+L4+L5 (oVTX)**: Support frame, cold plate, sensors, flex, power bus, water cooling

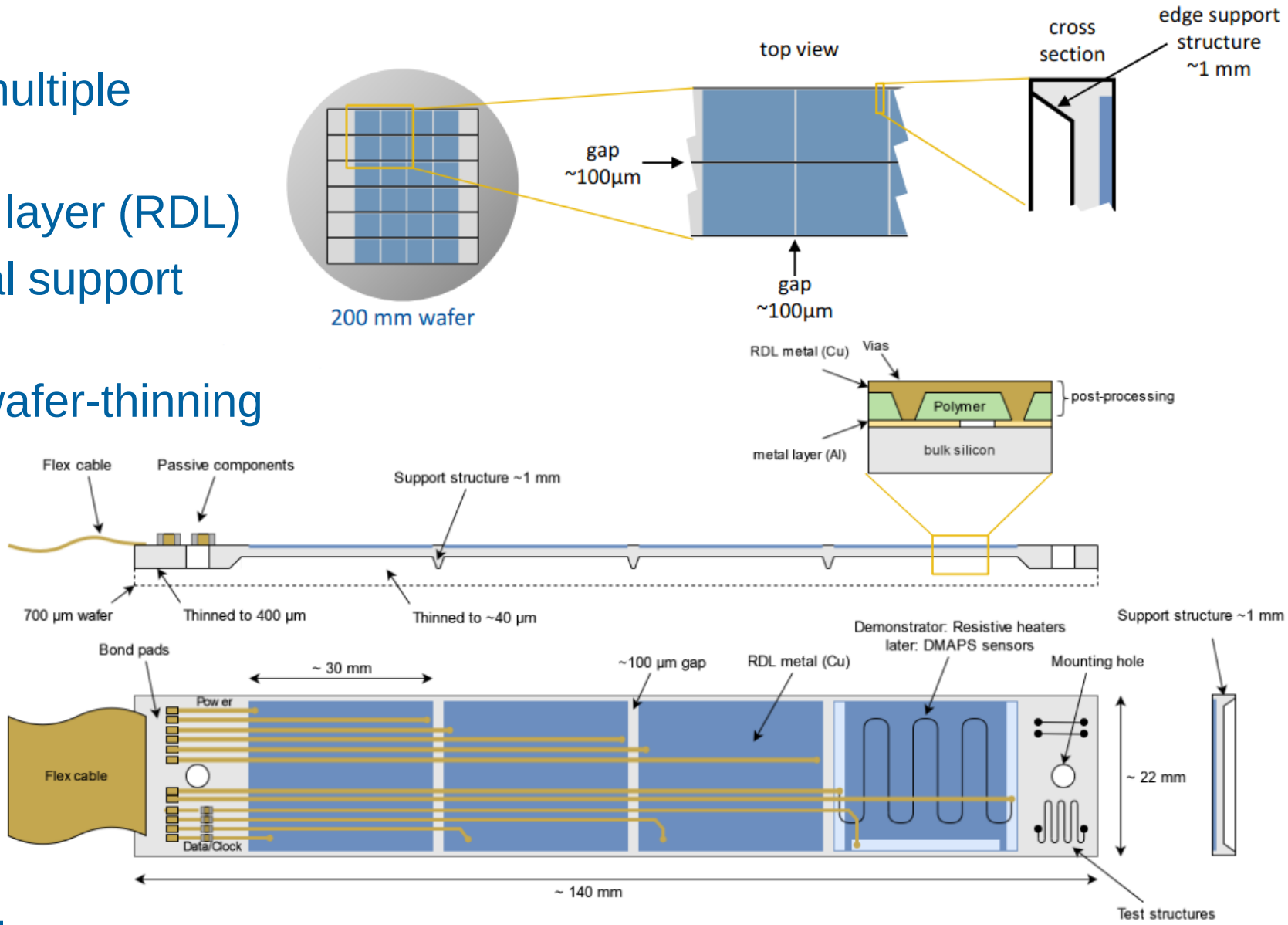






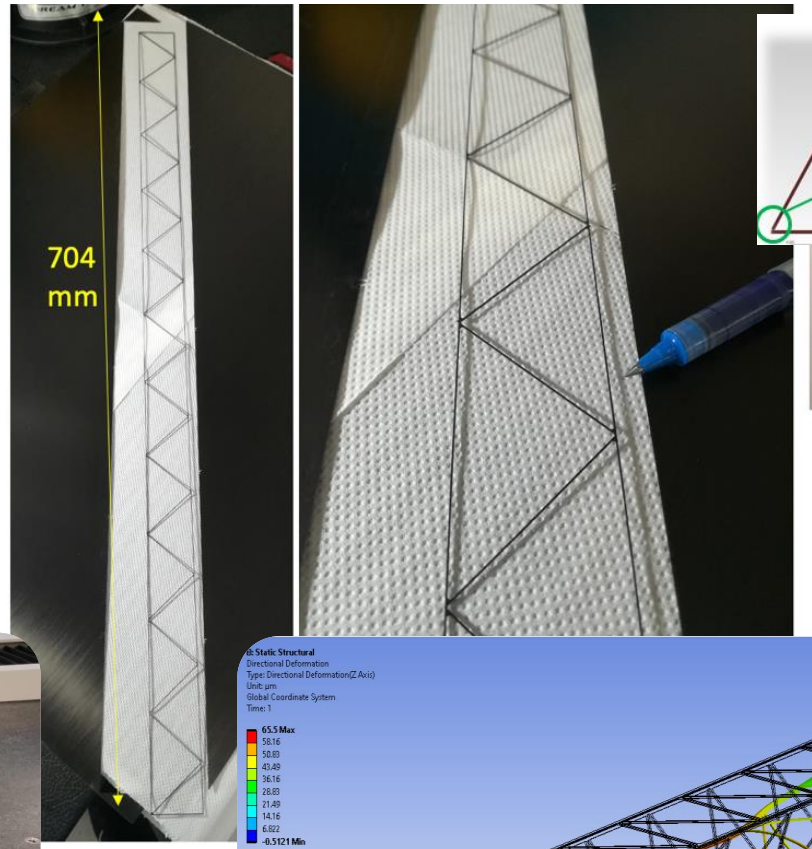
iVTX Design

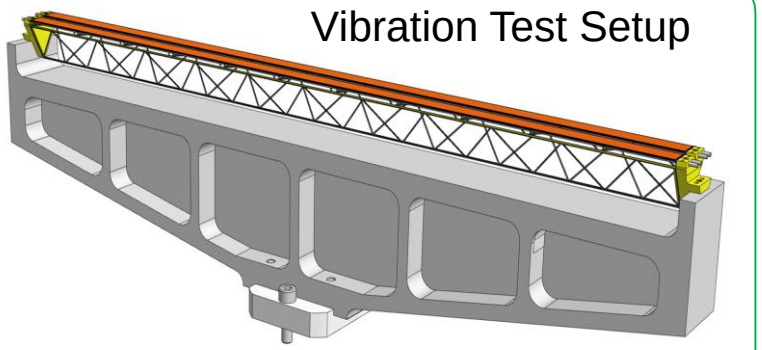
- L1+L2: full silicon design
- Single piece of silicon with multiple sensors per ladder
- Connected via redistribution layer (RDL)
- Thicker frame for mechanical support with thinned sensing area
- Specialized companies for wafer-thinning
- Different thinning-steps planned for evaluation:
  - 400 µm, 200 µm, 100 µm
- expected material budget: 2*0.1%X_0

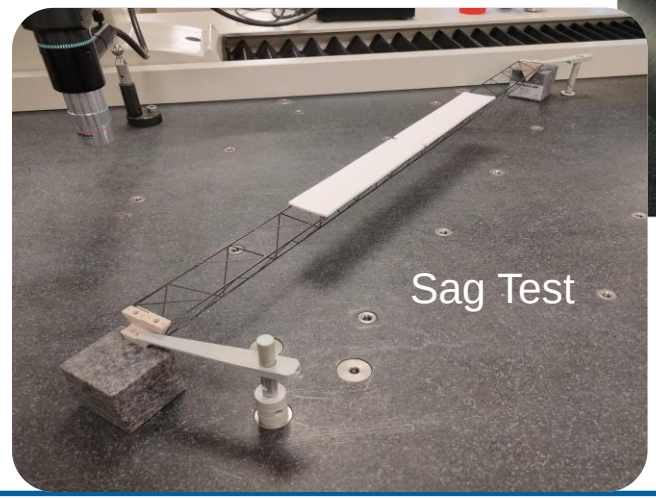


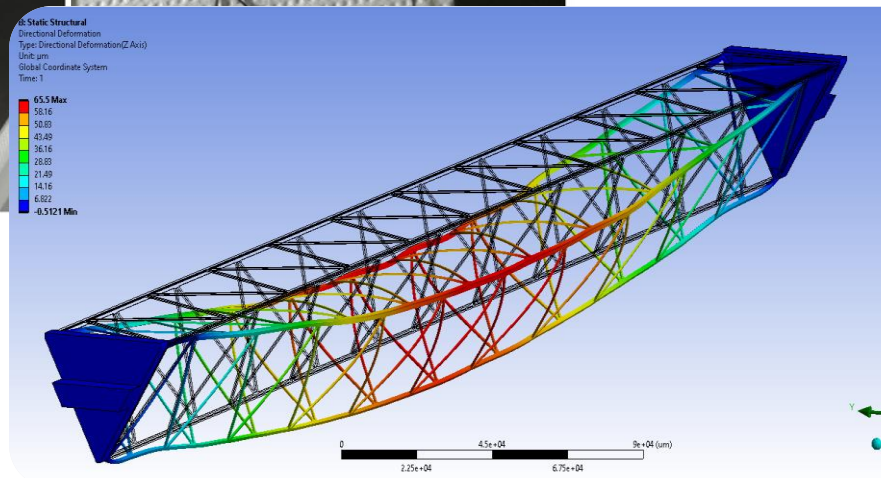
oVTX Design and Prototypes

- Three flat carbon-fiber structures glued together
- Up to 704 mm long (L5) but only 5.8 g
- Up to 60 g payload: very stiff design needed
- Vibrational Tests: mandatory to stay well above the typical earthquake frequencies (<20 Hz)
- Thermal characterization ongoing
- expected material budget: (2*0.3% + 1*0.8%) X_0









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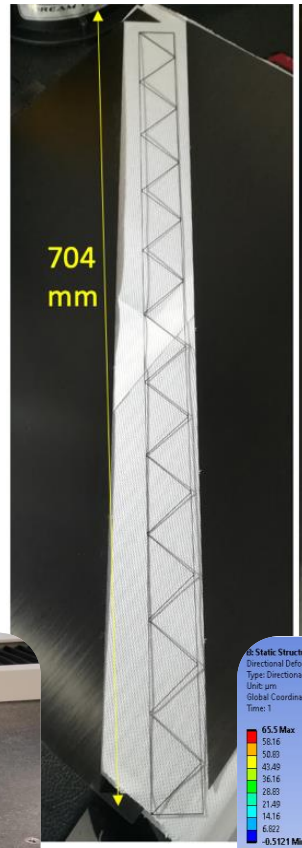
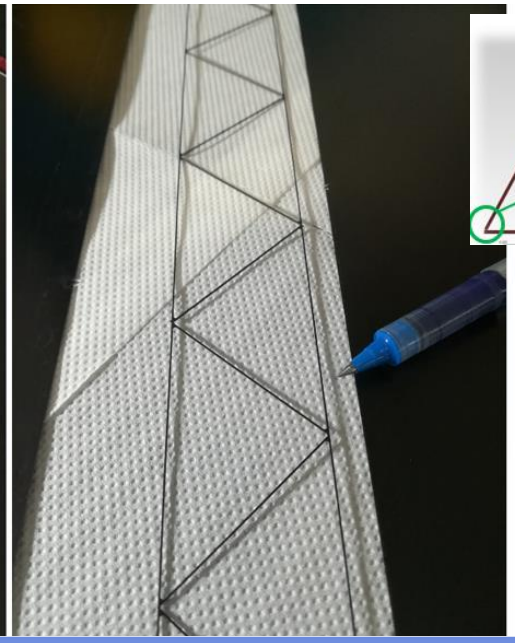
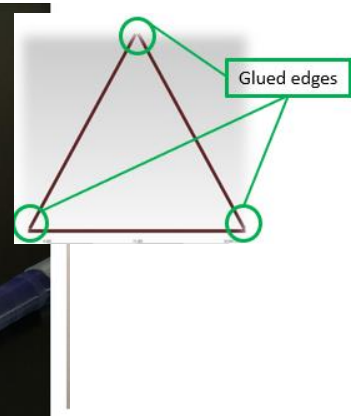
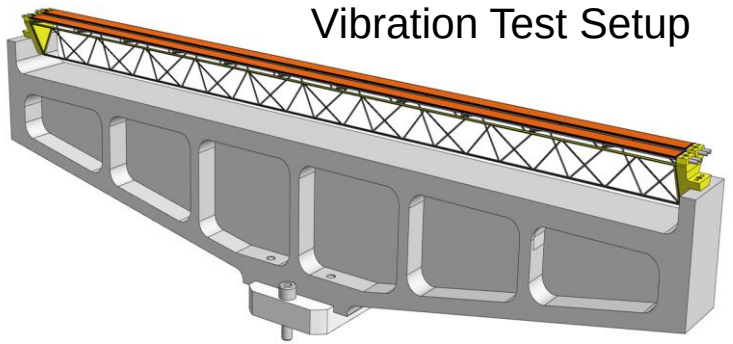
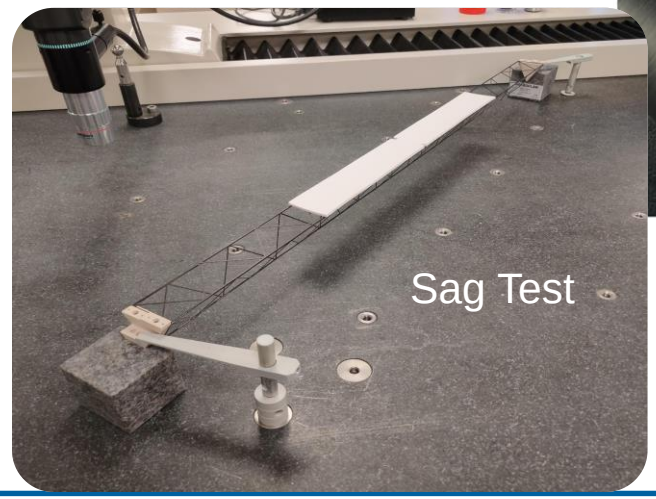
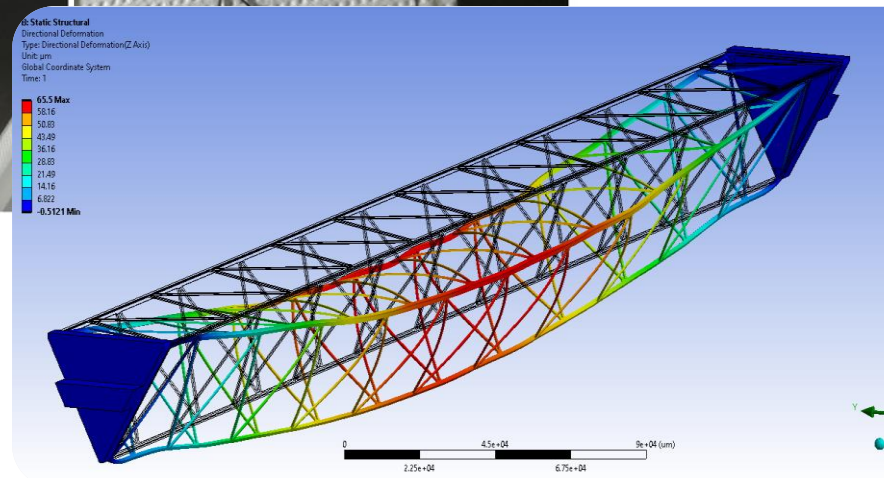




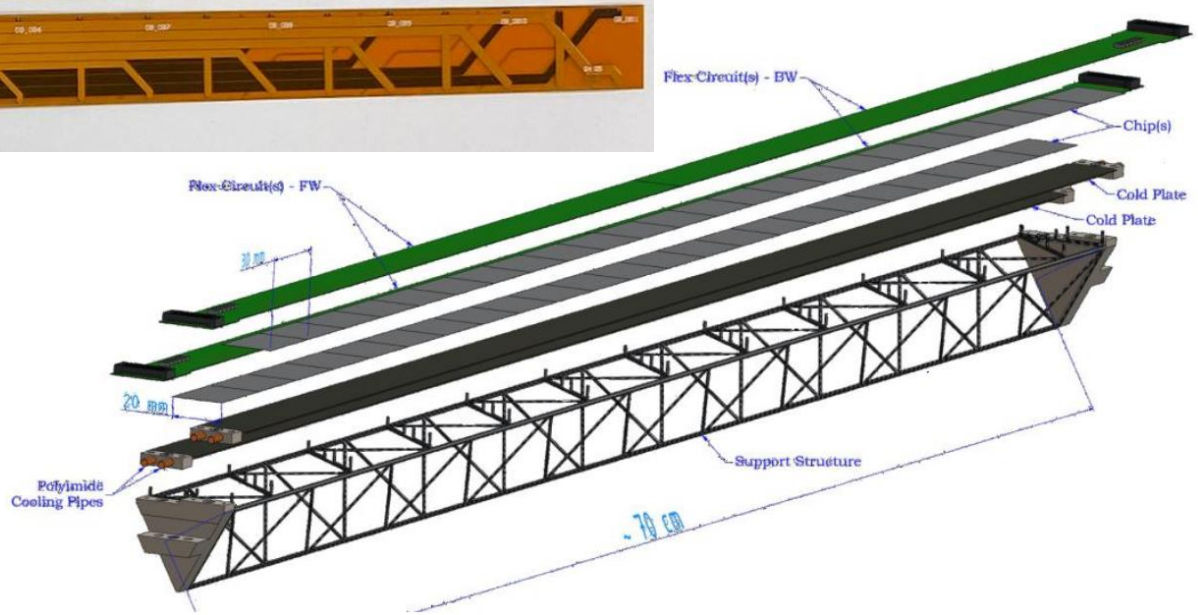




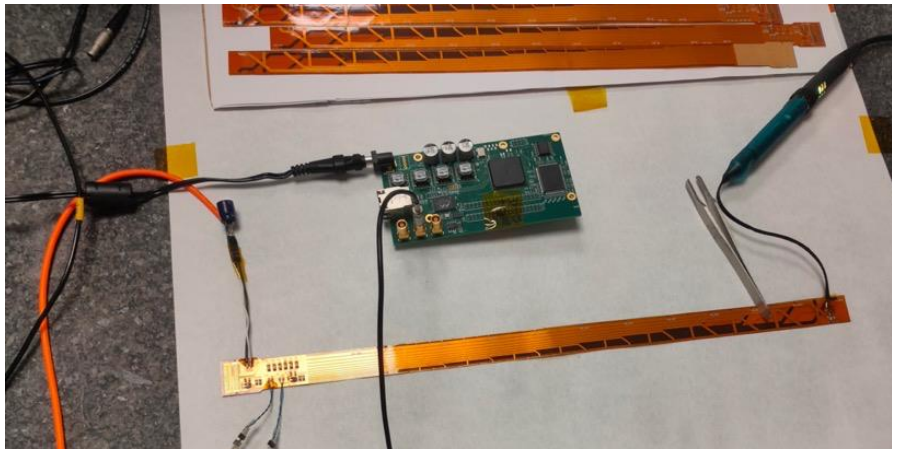


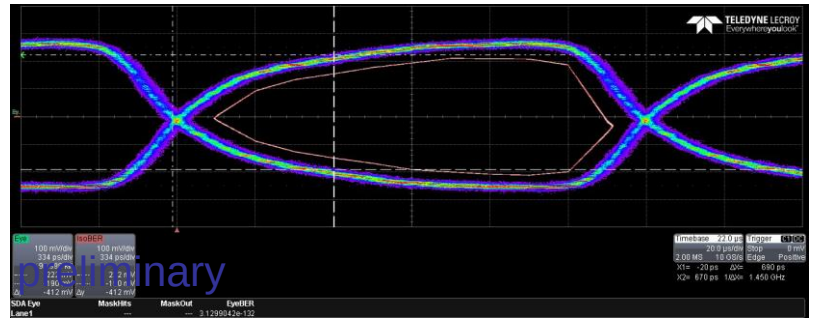


oVTX R&D and Tests



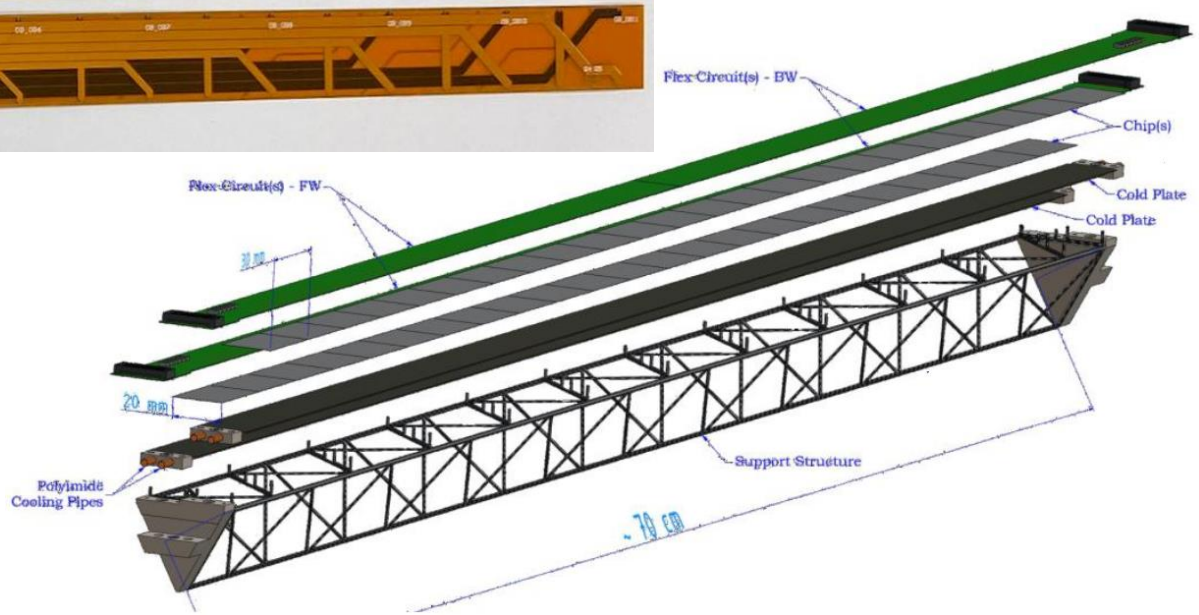
- First prototype for power and data
- Cu Flex used, plans for Al (material budget)
- Tests ongoing:
  - Signal integrity
  - Estimation of error rate
- Results look promising





eye diagram @250 MHz (500 Mbit/s)

oVTX Flex Prototype



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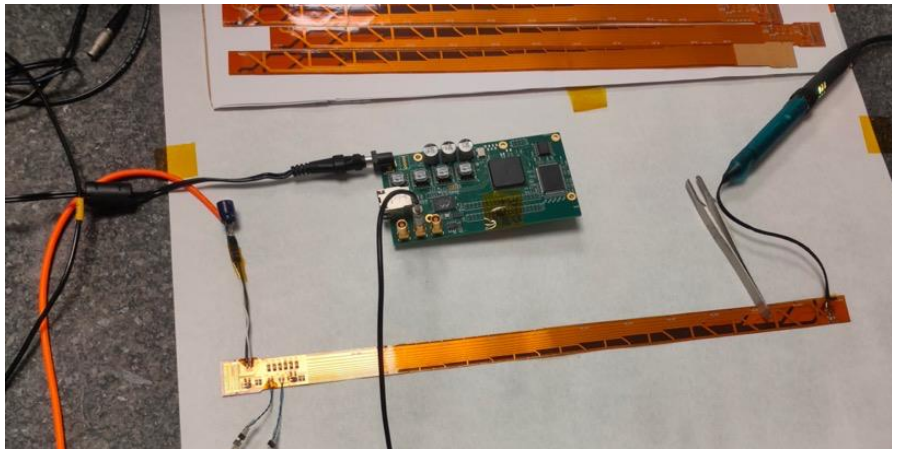

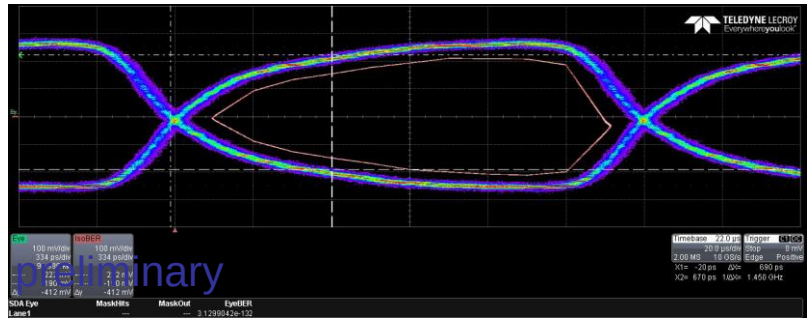

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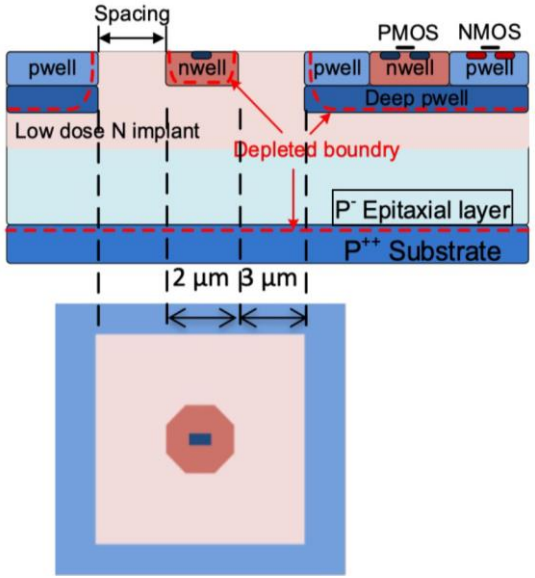
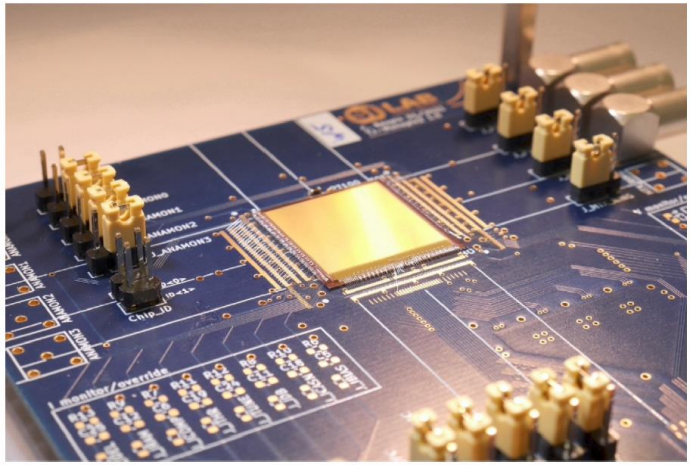
TJ-Monopix

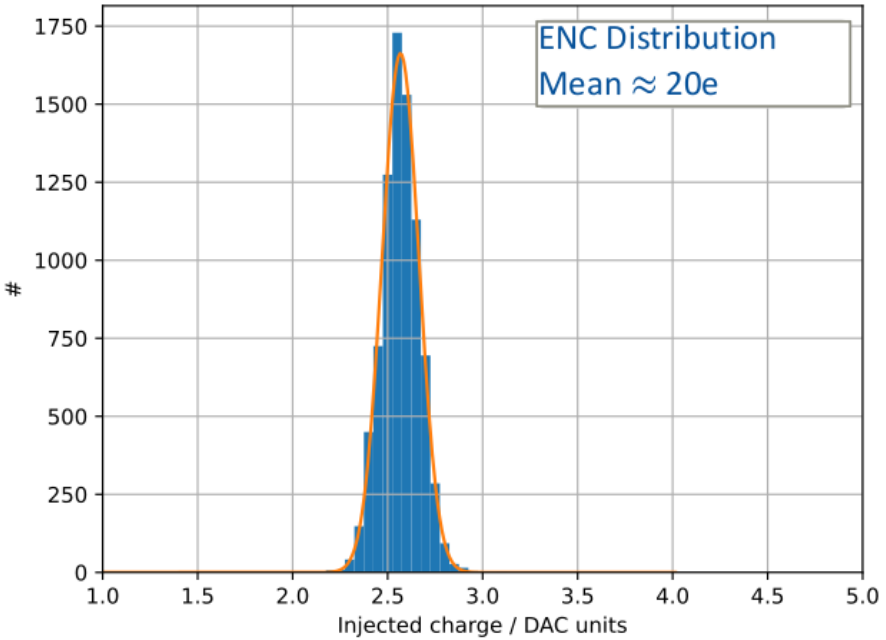


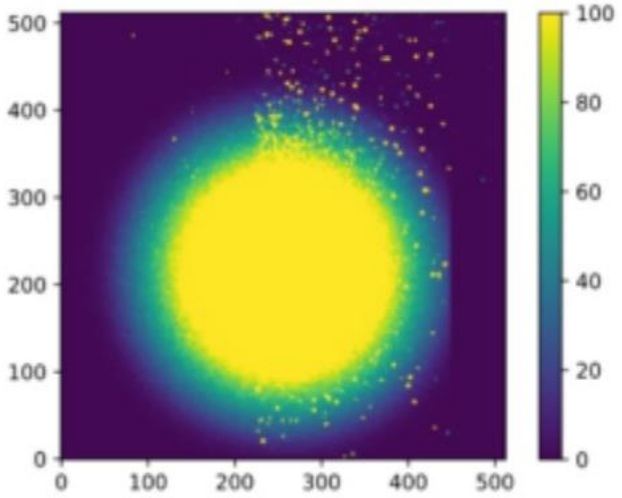


- TJ-Monopix2
  - Chosen as basis for Belle II VTX
  - DMAPS in TowerJazz (TJ) 180 nm process
  - Small collection electrode
    - small capacitance
    - low power and noise
  - High-resistivity epi layer: 1-8 kΩ cm
  - Chip size: 2 × 2 cm^2
  - Pixel pitch: 33 × 33 μm^2
  - 512 × 512 pixels
  - Power: ~ 1 µW/pixel
  - Column drain readout → **triggerless**

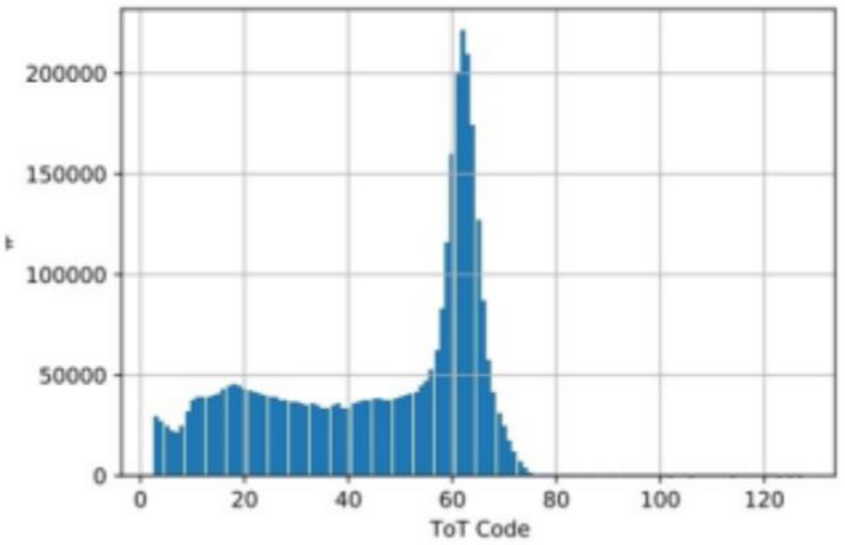
First Results from TJ-Monopix2

- First lab tests done checking ENC and threshold (still room for tuning)
- ENC is higher than expected due to some crosstalk, but still on a small level
- Further tests necessary
- Chips seem very sensitive (ESD suspeced)
  - Investigations ongoing
  - Needs to be resolved before further tests



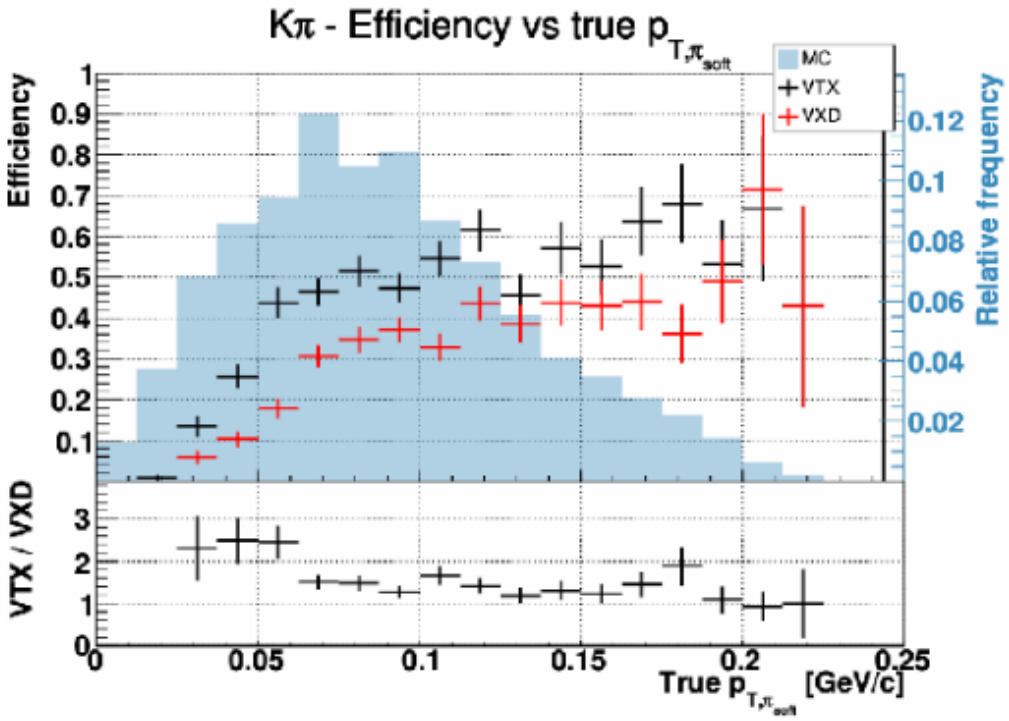


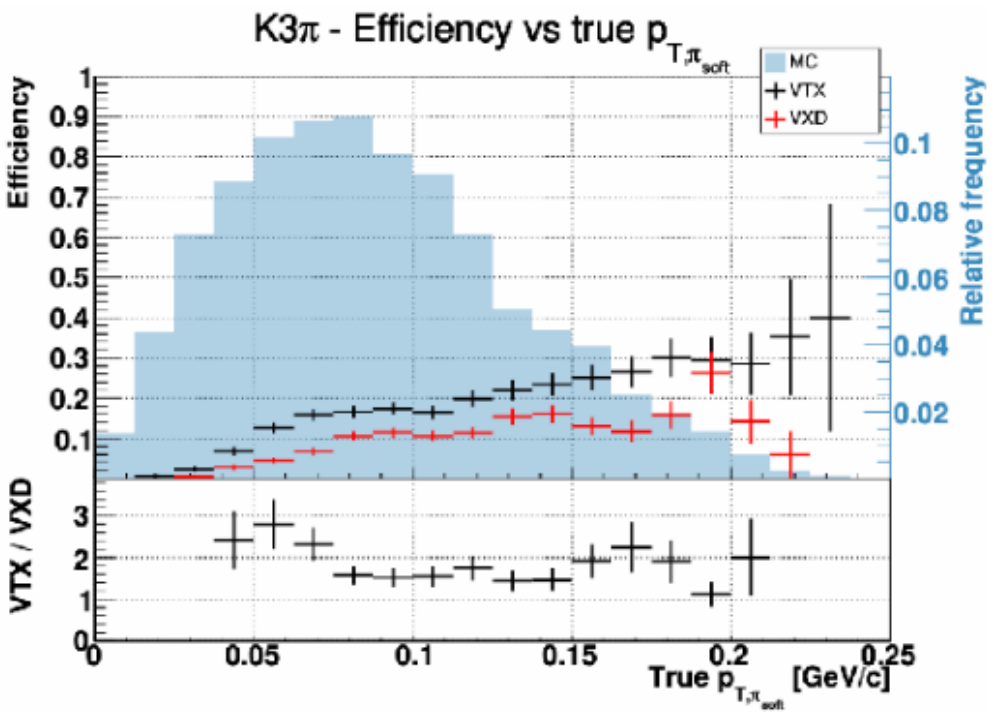
Fe^{55} Spectrum



VTX Performance Simulation

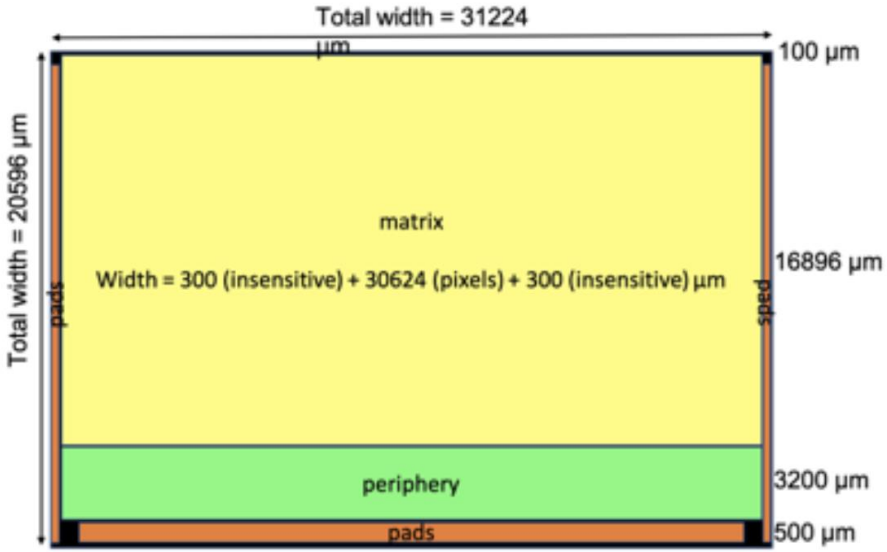
- Results from TJ-Monopix1 data used
- Reconstruction efficiency increases x1.5 – x1.8
- Lower reconstruction limit from 75 MeV to 50 MeV for p_T

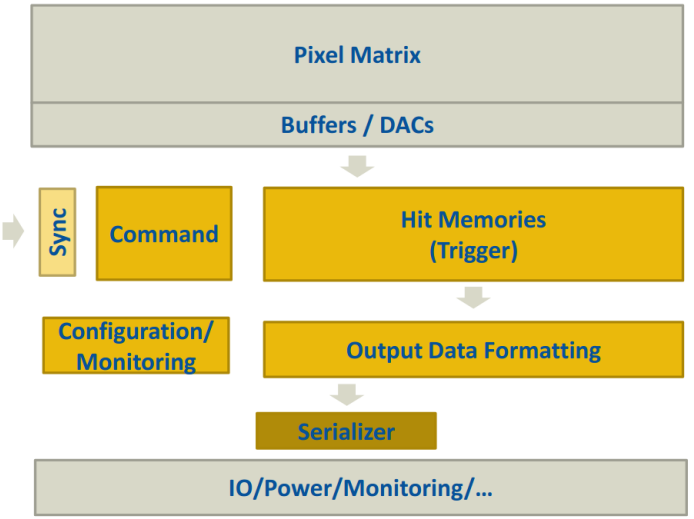




OBELIX

- OBELIX: **O**ptimized **BEL**le II p**IX**el sensor
- Analog matrix taken from TJ-Monopix2
  - Optional tuning when more results
- Analog powering of large-area Matrix
  - Narrow LDOs on both sides of the chip
- OBELIX implements Belle II specific adaptions
  - Hit memory
  - Large trigger latency is required (>5 µs)
  - Trigger synchronisation
  - On-chip clustering (optional)





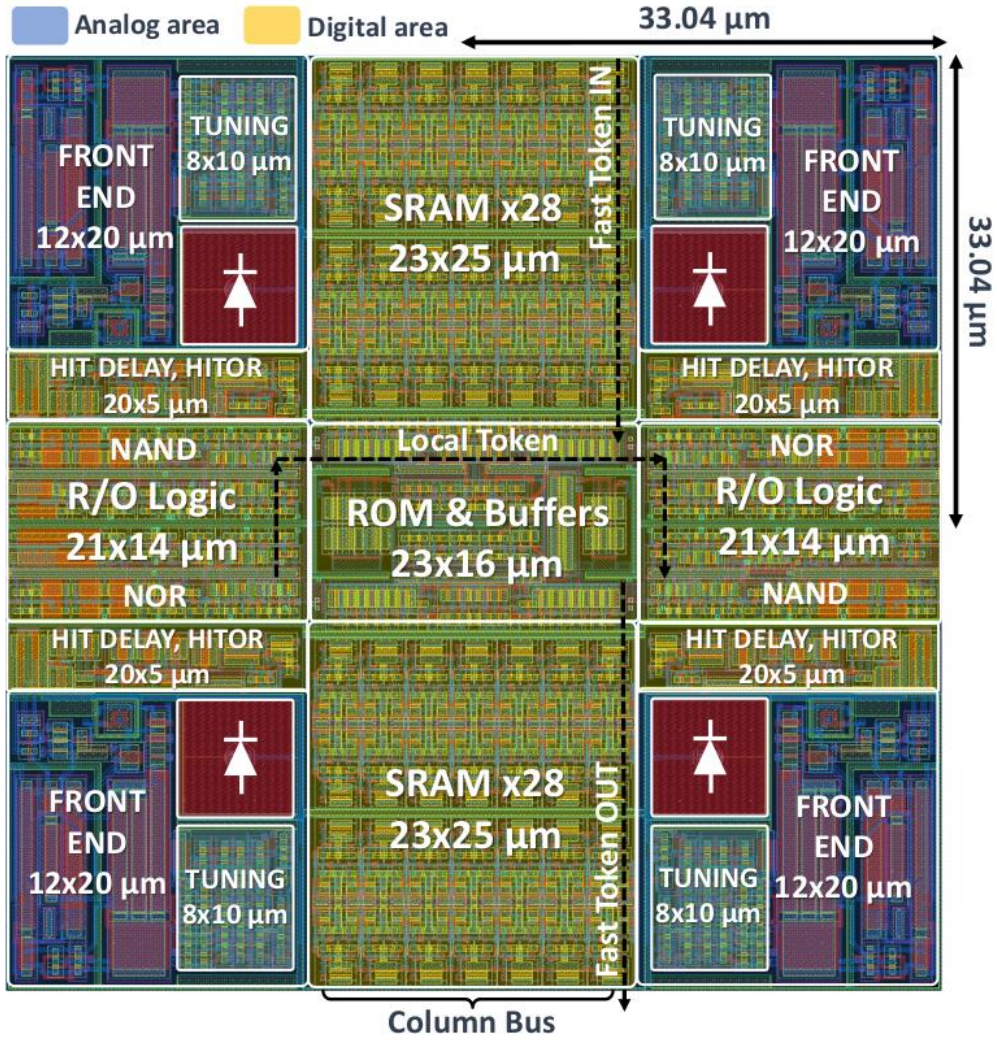
Summary and Outlook

- All pixel detector design improves tracking performance
- DMAPS promising technology for the Belle II upgrade at LS2
- Testing of **TJ-Monopix2** ongoing, first results available
- Deveopment of next version **Obelix** started recently
  - Dedicated for Belle II VTX
  - Additional digital processing for Trigger
  - Improvements of analog circuitry when tests are completed
- VTX design currently prototyped, low material budget

Backup Slides

TJ-Monopix2

- 33 x 33 μm^2 per pixel
- 4 pixels form pixel-cores ➔ area saving
- Pixel cores form double-columns
- 7-bit Timestamp for LE/TE
- Per pixel threshold tuning
- Timestamp delay compensation



TJ-Monopix readout scheme