Front end electronics of the Belle II Aerogel Ring Imaging detector

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Abstract

In the forward end-cap of the Belle II spectrometer, a proximity focusing RICH with aerogel radiator will be used for charged particle identification. The detector, consisting of 4 cm aerogel radiator, 16 cm expansion volume and a photon detector with 420 Hybrid Avalanche Photo Detectors is mounted in a very confined space between central drift chamber and electromagnetic calorimeter, leaving only 5 cm space for the readout electronics. A low power front end read-out board is mounted at the back side of each of the photo sensor. All the boards have been tested before the installation in the spectrometer. In the contribution, the design and first experiences with the boards are presented.

Keywords: Proximity focusing RICH with an aerogel radiator, Hybrid Avalanche Photo Detector, Front End Electronics

1. Introduction

The Belle II experiment in Tsukuba, Japan, will be dedicated to precision measurements of rare decays of B and D mesons and τ leptons to study the possible deviations from the Standard Model [1]. In the forward end cap of the spectrometer, a proximity focusing RICH with aerogel radiator will be installed in the 28 cm space between the Central Drift Chamber and the Electromagnetic Calorimeter. Cherenkov photons, emitted by charged particles in the aerogel radiator, are detected by a photon detector consisting of 420 144-channel Hybrid Avalanche Photodetectors (HAPD) with the front end electronic boards at their back sides [1, 2]. The front end readout board should be able to detect the 35000 e^- high signals which will during 10 years of operation gradually decrease due to irradiation. Because it is positioned in the strong magnetic field the boards do not contain any magnetic materials. $75mm \times 75mm$ big boards are oriented parallel to the HAPD entrance window, since there is only about 5 cm of space available behind the photo sensors for the electronics and the service infrastructure. In addition the readout board also houses a connector supplying four bias and one guard voltage (175 V to 350 V) to the appropriate sensor pins. The digitized signals from up to six front end boards are collected by merger boards mounted approximately 4 cm above the front end boards. The electronics is connected via 30 m long cables to power supplies and common readout electronics positioned outside of the spectrometer.

2. Front end Readout board

The front end readout board consists of 12 layer PCB with a pin grid array connector for the HAPD photo sensor, power supply, bias and data I/O connectors (Fig. 1). Several different operating and reference voltages are generated by the on board low dropout regulators. On the sensor side there are 4 custom ASICs which amplify, shape and digitize 4×36 input signals, protected from the over currents with two ESD protection diode stages. The operation of the ASIC chip is controlled by the internal registers. Its output digital signals are connected to a Xilinx Spartan-6 FPGA clocked by either external or onboard 42 MHz oscillator. The FPGA controls the discriminator level of the ASIC via the on-board DACs, samples the digital signals and at the trigger signal serializes the data and send it through the data connector to a merger board, where the data from up to six front end boards are collected after a trigger sig-

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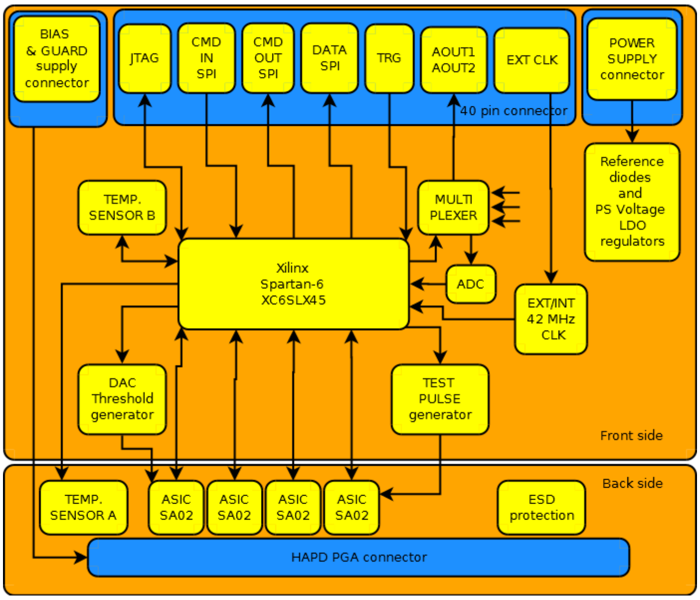

Figure 1: Functional schematic of the Front End Board: 4 custom ASICs positioned on one side of the board digitize the input signals. The digital signals are processed on a Xilinx Spartan-6 FPGA placed on the other side of the board, which is also responsible for the communication and the control of the peripherial devices. The front side of the board houses three connectors: a bias and guard supply, the communication and a power supply connector. From the supply voltages the reference voltage of 1.25 V is generated by a diode and all the other operating voltages by the low dropout regulators (LDO). The ADC chip is used to control different internal voltage levels, which are selected by the multiplexer. The chip discriminator level is set by the digital potentiometer. On the board there is also an internal oscillator to clock the FPGA, replaced by external clock during the operation in the Belle II detector. Two temperature sensors allow temperature monitoring of the front and back side of the board. In addition there is also a test signal generator and electrostatic discharge protection diodes of the signal inputs.

nal and sent through an optical link to an experiment data acquisition card. From the merger board an FPGA firmware can be downloaded via dedicated JTAG lines. The FPGA accepts the instruction commands via receive and responds via transmit lines of the data communication cable. For testing and monitoring purposes (control of the board supply voltages, temperatures and monitoring of analog and digital signals from different stages of ASIC) the board houses two multiplexers, an analog to digital converter and a temperature sensor. For debugging purposes the board provides a test pulse signal, generated and controlled by the FPGA.

2.1. Firmware design

The firmware consists of an 64 bit instruction decoder, data sender, command receiver and response sender. The instructions are received via one way asynchronous "SPI". The response of each command is sent back encoded in a response word through a separate dedicated one way "SPI". The trigger signal starts the data encoder and sends the data through another one way "SPI".

Each hardware peripheral device has a driver triggered by the instruction decoder. In addition a data register is used to control the mode of operation, the sampling and encoder frequencies. The FPGA DNA is used as a unique identifier of the board.

Figure 2: Photo of the front-end board attached to HAPD. There are three connector cables for a data transfer, board and bias power supplies

The front end read-out board should be able to withstand the neutron fluence of 10^{12} 1 MeV n_{eq}/cm^2 and gamma radiation dose of 100 Gy during the expected life time of the Belle II spectrometer. Due to sensitivity of Xilinx Spartan-6 devices to neutrons, the firmware core includes a Xilinx software SEU mitigation controller which corrects the SEUs and signals the unrecoverable errors through a separate heartbit line in the data bus. The signal enables the reload of the firmware and the operational parameters to the board from the safe environment.

3. Production

For the Belle II aerogel RICH detector 440 front end boards have been produced. Their production was smooth with some minor difficulties in the placement of the 152 pin surface-mount custom HAPD connector, which has several through hole pins to gain mechanical stability during the possible service sensor detachments. Each board has been first tested before and then after the HAPD sensor attachment. The tests consisted of several consecutive firmware downloads and verifications of the operating voltage levels and of the temperature sensors. The operating parameters were loaded and read back from the ASIC registers. We also checked the response of the front end board to the noise, test pulses and triggered short green light pulses for different levels of the discrimination threshold.

More than 97% of the boards were fully functional. About 1% were not usable, while 2% were potentially usable having one to several unconnected channels.

The boards should have passed several structural and functional tests before being accepted. They were first connected to the power and common bias supply, data and JTAG cable. Then they have been tested by connecting the dummy board with resistance to the ground and bias voltages and the capacitive signal connections to mimic the capacitance final HAPD sensor. Later the boards have been attached with the HV divider board to the HAPDs. Such modules have been tested under the nominal working voltages by measuring their response to a focused triggered laser light (λ = 532 nm).

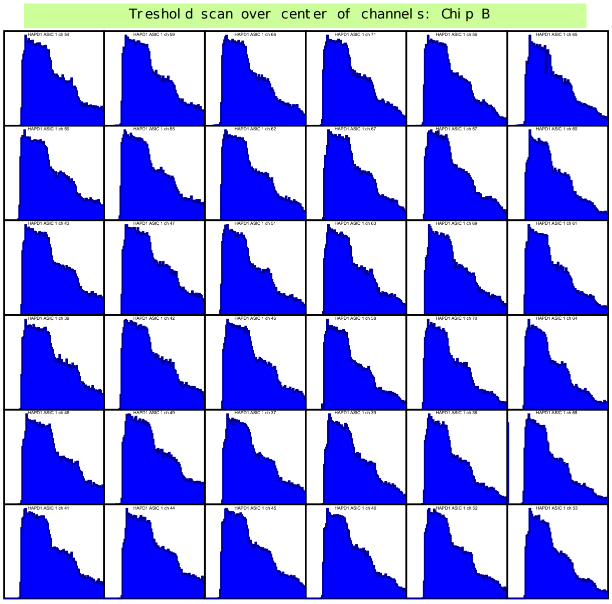

Figure 3: HAPD sensor response to short low intensity light pulses as a function of a discriminator threshold (36 channels of one of the 4 chips are shown). Noise, single and double photoelectron hits can be seen.

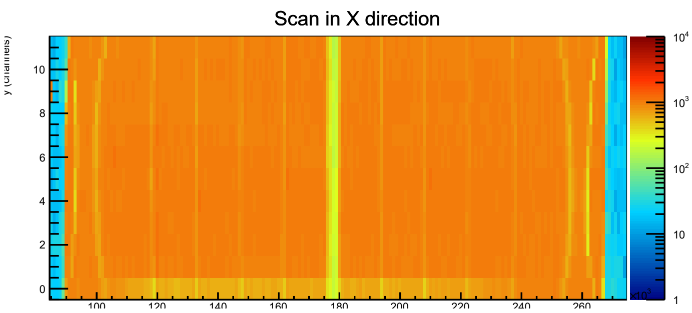

Figure 4: Surface variation of a sensor response to short low intensity light pulses. Due to long measurement time, granularity in x and y direction differ.

By changing the ASIC chip comparator threshold voltage, we scanned the response to several photons (Fig. 3). Note the sharp steps in te threshold scan demonstrating the ability of the ASIC chip to discriminate between hit and non hit channels. By moving th laser spot over the sensor surfaces , we measured very homogeneous response (Fig. 4).

4. Test in the high radiation environment

One of the possible limiting factor in the use of the readout electronics is the use of Spartan-6 FPGA. In Spartan-6 Boron is used as a p-type dopant in production of silicon wafers because it diffuses at a rate that makes junction depths easily controllable. Unlike in other FPGAs the concentration of Boron is high. Thermal neutrons are the main cause of the problems in the integrated circuits due to interactions with the dopant boron

$$^{10}B + n \rightarrow ^{7} Li + \alpha + \gamma\, (94\%) \quad (1)$$

$$\rightarrow ^{7} Li + \alpha\, (6\%) \quad (2)$$

Bit flip	N	t(min)	SEU/h	Belle II extrapolation
$0 \rightarrow 1$	705	17	2488	7.5
$1 \rightarrow 0$	20	17	70.5	0.2

Table 1: Irradiation test of the number of bit changes at neutron fluence of $3.275 \times 10^6 n/s/cm^2$ and γ dose rate of 4.3 Gy/h.

To test the functionality of the FPGA during and after the irradiation, one of the boards has been tested in a TRIGA nuclear reactor, where the energy spectrum of the neutrons in the reactor is similar to the expected one in the Belle II detector [4].

Different tests have been made during several irradiation sessions at rates 700× higher than expected in the Belle II. The cumulative radiation dose and the total neutron fluence exceeded the foreseen values acquired during Belle II lifetime for a factor of 5. During the test the boards were powered and constantly performing different checks: verification of the ASIC chip configuration parameters, monitoring of the threshold voltages and the on-board temperature chip, response of the board to different threshold voltages, test of the communication part, and counting changes in the static part of the firmware (Table 1).

By extrapolating the results to the Belle II, we expect the uncorrectable error resulting in a possible malfunctioning of a single board will happen about 10 times per hour. Since 420 modules will be installed, we plan to reset the unrecoverable errors by uploading the firmware and the parameters during the data taking.

5. Conclusions

420 front end readout boards are used to read out the photosensors of the Belle II Aerogel Ring Imaging detector. After the complex design phase all the components of the photon detector have been manufactured and tested on the bench. The detector was installed in 2016 and 2017 by carefully routing the cables through the available space and finally mounted in the Belle II spectrometer. During the commissioning phase, the complete electronics has been gradually connected to the power supplies and to the data acquisition system. We have confirmed the performance of the front end boards by registering cosmic ray and later also first beam collision events in 2018. We expect an excellent performance of the detector in the coming years.

6. Acknowledgments

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