Study on first-level trigger of the Belle II experiment using upgraded silicon strip detector

(新型シリコンストリップ検出器を用いたBelle II実験初段トリガーの研究)

By

Tomoyuki Shimasaki
島崎 奉文

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Thesis Supervisor: Takeo Higuchi　樋口 岳雄

ABSTRACT

In order to explore new physics beyond the Standard Model, the Belle II experiment plans to accumulate the integrated luminosity of $50\,\mathrm{ab}^{-1}$. The SuperKEKB collider, an accelerator used in the Belle II experiment, is designed to achieve the world's highest luminosity of $6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ so that we can accumulate the target data volume in reasonable time scale of about 15 years. However, the data generated by SuperKEKB with such high luminosity is so large that the data acquisition (DAQ) system cannot store all of it due to the limited bandwidth of the sampling rate and data transfer of each Belle II sub-detector. For this reason, the first-level trigger system is employed, which determines if each event is of interest and selects the data to be stored. For stable operation of the DAQ system, the maximum average Level-1 trigger rate is set to be 30 kHz. However, the trigger rate is expected to exceed the limit at the target luminosity in the future due to harsh beam backgrounds. The major contributor to the background trigger rate is considered to be particles produced outside of the interaction point (IP), which are called Off-IP particles. They cannot be sufficiently rejected by the current Level-1 trigger system due to its low capability to identify particle production positions. Therefore, a new Level-1 trigger system with higher position resolution is desired.

The Silicon Vertex Detector (SVD), which is a type of silicon strip detector and responsible for particle decay vertex reconstruction in cooperation with the Pixel Detector (PXD). It has high position resolution for charged particles, however, has no function for the Level-1 trigger. The Thin Fine-Pitch SVD (TFP-SVD) is being developed as the next generation vertex detector. It will have higher position resolution than the current SVD and have function for the Level-1 trigger. Therefore, we developed new trigger algorithm using the TFP-SVD in simulation to efficiently reject Off-IP particles and suppress the background trigger rate. As a result, we confirmed that the TFP-SVD trigger has sufficient trigger efficiency and Off-IP particle rejection power. Furthermore, fake triggers, which are derived from fake tracks reconstructed by harsh background sensor hits, can be suppressed by the TFP-SVD trigger by combining with the current trigger system. By introducing the TFP-SVD trigger, it is expected that the upper limits of the trigger rate, 30 kHz, can be observed even at the target luminosity. After the simulation study, we implemented the TFP-SVD trigger as firmware and confirmed its feasibility.

Contents

Chapter 1

Introduction

The Standard Model (SM) predicts most of the phenomena in the elementary particle physics at the energy scale up to $\mathcal{O}(1)$ TeV. However, it is not considered to be the ultimate theory because of the large number of parameters, large discrepancies in particles masses and coupling constants, and the existence of dark matter. To search for new theories beyond the SM, experimental measurements with much higher precision are required. B-Factory, which is a type of particle collider experiment designed to produce a large number of B mesons so that their properties and behavior can be measured precisely, has made a significant contribution to our understanding of particle physics. In particular, the Belle experiment [1], which was located in KEK, Tsukuba (Japan), and designed to produce many $B\bar{B}$ pairs as decay products from $\Upsilon(4S)$, observed CP violation in $B\bar{B}$ oscillations and validated the Kobayashi and Maskawa's theory [2].

The Belle II experiment is the successor B-Factory to the Belle experiment. Its center-of mass energy of the asymmetric energy $e^{-}e^{+}$ collider is set to the resonance of $\Upsilon(4S)$ as with the Belle. However, the Belle II experiment aims to measure far more $B\bar{B}$ pairs with the fifty-fold higher integrated luminosity than the Belle experiment and measures the CP asymmetries in the B decays described in Section 1.1 with much more precision to validate the SM. Furthermore, the Belle II experiment can explore the τ physics and dark sector.

Those measurements can be supported by high statistics data. However, since the bandwidth of the sampling rate and data transfer of each Belle II sub-detector is finite, it is not possible to store all of the data generated by such a high luminosity accelerator. For this reason, the Belle II experiment employs the first-level trigger system called "Level-1 trigger" to select data before recording. For stable operation of the data acquisition system, the maximum average Level-1 trigger rate is limited to 30 kHz, and we plans to accumulate the integrated luminosity of $50\,\mathrm{ab}^{-1}$ in about 15 years.

1.1 CKM matrix

The Belle II experiment challenges a wide range of physics. One of the important examples is the measurement of the CKM matrix.

The SM is described by a quantum field theory with the internal gauge symmetries of $\mathrm{SU}(3)_C \times \mathrm{SU}(2)_L \times \mathrm{U}(1)_Y$. It contains the fermion fields, which account for "matter particles", the electroweak boson fields, which are based on the $\mathrm{SU}(2)_L \times \mathrm{U}(1)_Y$ symmetry, the gluon fields, which are based on the $\mathrm{SU}(3)_C$ symmetry, and the Higgs fields. The fermion fields are classified into the quark fields, which are coupled with the gluons, and lepton fields, which are

not coupled with the gluons. Furthermore, quark fields consists of three generations of up-type quarks u_k and down-type quarks d_k where $k = 1,\ 2,\ 3$ denotes the generation index. While the left-handed quark fields (u_{kL} and d_{kL}) form doubles of the $\mathrm{SU}(2)_L$ group, the right-handed quark fields (u_{kR} and d_{kR}) are singlets. The Higgs fields (ϕ^0 and $\phi^\pm$) also form doublet. Their doublets are represented as

$$\Psi_{kL} = \begin{pmatrix} u_k \\ d_k \end{pmatrix}_L, \quad \Phi = \begin{pmatrix} \phi^+ \\ \phi^0 \end{pmatrix}, \quad \Phi^c = \begin{pmatrix} \phi^{0\dagger} \\ -\phi^- \end{pmatrix} \qquad (k = 1,\ 2,\ 3) \tag{1.1}$$

The Lagrangian $\mathscr{L}_I$, in which the quark fields couple with Higgs fields, is represented by

$$-\mathscr{L}_I = \sum_{j,k} \left[M^U_{jk} \overline{\Psi}_{jL} \Phi^c u_{kR} + M^D_{jk} \overline{\Psi}_{jL} \Phi d_{kR} + h.c. \right] \tag{1.2}$$

where $M^{U,D}_{jk}$ are coupling constants between the quark fields and Higgs fields, and $h.c.$ stands for Hermitian conjugate. If the ϕ^0 has nonzero vacuum expectation via spontaneous breaking of the $\mathrm{SU}(2)_L \times \mathrm{U}(1)_Y$ symmetry, the mass terms of the quarks are obtained

$$\begin{aligned} -\mathscr{L}_m &= \frac{v}{\sqrt{2}} \sum_{j,k} \left[M^U_{jk} \overline{u}_{jL} d_{kR} + M^D_{jk} \overline{d}_{kL} d_{kR} + h.c. \right] \\ &= \frac{v}{\sqrt{2}} \left(\overline{U}_L M^U U_R + \overline{D}_L M^D D_R + h.c. \right) \in \mathscr{L}_I \end{aligned} \tag{1.3}$$

where $v/\sqrt{2}$ is a nonzero vacuum expectation value, $U_{L,R} = (u, c, t)_{L,R}$ and $D_{L,R} = (d, s, b)_{L,R}$ are vectors of up-type and down-type quarks respectively, and $M^{U,D}$ are 3×3 complex matrices.

The u, c, t, d, s, and b are weak eigenstates. However, the time evolution of the quark fields are described by their mass eigenstates, which can be obtained by diagonalizing the M^U and M^D as

$$M^U = S^{U\dagger}_L M^U_{\mathrm{diag}} S^U_R, \quad M^D = S^{D\dagger}_L M^U_{\mathrm{diag}} S^D_R \tag{1.4}$$

where $S^{U,D}_{L,R}$ are Unitary matrices, $M^U_{\mathrm{diag}} = \mathrm{diag}(m_u, m_c, m_t)$, and $M^D_{\mathrm{diag}} = \mathrm{diag}(m_d, m_s, m_b)$ are diagonal matrices with quark masses. By substituting these, Eq. (1.3) is rewritten as

$$\begin{aligned} -\mathscr{L}_m &= \frac{v}{\sqrt{2}} \left(\overline{U}'_L M^U_{\mathrm{diag}} U'_R + \overline{D}'_L M^D_{\mathrm{diag}} D'_R + h.c. \right) \\ &= \frac{v}{\sqrt{2}} \sum_{x=u,c,t\ y=d,s,b} \left[m_x \overline{u}'_{xL} u'_{xR} + m_y \overline{d}'_{yL} d'_{yR} + h.c. \right] \end{aligned} \tag{1.5}$$

where $U'_{L,R} \equiv S^U_{L,R} U_{L,R} = (u', c', t')_{L,R}$ and $D'_{L,R} \equiv S^D_{L,R} D_{L,R} = (d', s', b')_{L,R}$ are mass eigenstate vectors of the quarks.

The conversion of the eigenstates gives rise to the generation mixing of the quarks through the charged weak interaction.

$$\begin{aligned} -\mathscr{L}_W &= \frac{g_W}{\sqrt{2}} \left[\overline{U}_L \gamma^\mu D_L W^+_\mu + h.c. \right] \\ &= \frac{g_W}{\sqrt{2}} \left[\overline{U}'_L \gamma^\mu V D'_L W^+_\mu + h.c. \right] \\ &= \frac{g_W}{\sqrt{2}} \sum_{j,k} \left[\overline{u}'_{jL} \gamma^\mu V_{jk} d'_{kL} W^+_\mu + \overline{d}'_{kL} \gamma^\mu V^*_{jk} u'_{jL} W^-_\mu \right] \end{aligned} \tag{1.6}$$

where $W_\mu^\pm$ denotes the W bosons, γ^μ is a gamma matrix, g_W is the coupling constant between the quark fields and the weak bosons, and $V \equiv S_L^U S_L^{D\dagger} = (V_{ij})$ $(i,j = 1,2,3)$ is a 3×3 unitary matrix called the Cabibbo-Kobayashi-Maskawa (CKM) matrix.

$$V = \begin{pmatrix} V_{11} & V_{12} & V_{13} \\ V_{21} & V_{22} & V_{23} \\ V_{31} & V_{32} & V_{33} \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \tag{1.7}$$

There are many conventions to represent the CKM matrix. It is experimentally known that $|V_{ub}|^2 \ll |V_{cb}|^2 \ll |V_{us}|^2$, and the Wolfenstein parameterization is used to exhibit this hierarchy:

$$V = \begin{pmatrix} 1 - \lambda^2/2 & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \lambda^2/2 & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} + \mathcal{O}(\lambda^4) \tag{1.8}$$

where $\lambda \simeq 0.22$, and A, ρ, and η are $\mathcal{O}(1)$.

The unitarity condition of the CKM matrix leads to nine independent equations. The one most relevant to B physics is

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0, \tag{1.9}$$

in which all the terms are order $\mathcal{O}(A\lambda^3)$. Eq. (1.9) is represented as a triangle in the complex plane as shown in Fig. 1.1, which is called the "unitarity triangle" and each angle is given by

$$\begin{aligned} \phi_1 &= \arg\left(-\frac{V_{cd}V_{cb}^*}{V_{td}^*V_{tb}}\right) \\ \phi_2 &= \arg\left(-\frac{V_{td}V_{tb}^*}{V_{ud}^*V_{ub}}\right) \\ \phi_3 &= \arg\left(-\frac{V_{ud}V_{ub}^*}{V_{cd}^*V_{cb}}\right). \end{aligned} \tag{1.10}$$

The independent measurements of these three angles lead to the verification of the SM. This is one of the purpose of the Belle II experiment [3].

The angle ϕ_1 can be determined via the $b \to c\bar{c}s$ transitions. The mode of $B \to J/\psi K_S^0$ is called the "golden mode" for the ϕ_1 determination because it has small theoretical uncertainty and clean experimental signature. The angle ϕ_2 can be determined via the $b \to u\bar{u}d$ transitions. Especially, $B \to \pi\pi$ and $B \to \rho\rho$ decay modes are studied by analyzing the isospin symmetry in these transitions. The angle ϕ_3 is precisely measured via the CP asymmetry in the decay modes of $B \to D^*K^*$ and $B \to D^*\pi$.

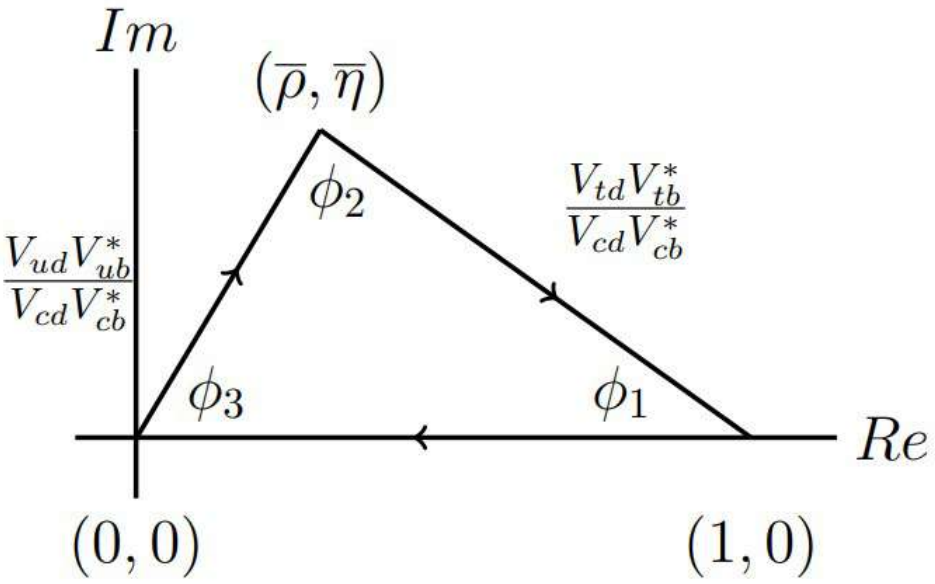

Figure 1.1: Unitarity triangle [3].

1.2 Motivation of a new Level-1 trigger

The SuperKEKB collider, an accelerator used in the Belle II experiment, achieved the instantaneous luminosity of $4.7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in June 2022. For more efficient data taking, we will continue to increase the luminosity by tuning the machine parameters. On the other hand, the increase in the luminosity results in the higher beam background rate. At the target luminosity of $6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the average Level-1 trigger rate is expected to exceed the upper limit of 30 kHz. The major contributor to the background trigger rate is considered to be Off Interaction Point (Off-IP) particles, which are produced outside of the beam interaction point. The Off-IP particles are expected to be rejected by selecting their production positions. The current main trigger system is the Central Drift Chamber (CDC) trigger, which reconstructs the particle trajectories and identifies the particle production positions. However, as described in Section 3.1, the CDC trigger cannot sufficiently reject the Off-IP particles due to its limited position resolution. Therefore, a new Level-1 trigger system with better position resolution is desired. Fake triggers, which are derived from fake tracks reconstructed by harsh background sensor hits, also contribute to the background trigger rate. However, the new trigger with high position resolution is expected to suppress the fake trigger.

The Silicon Vertex Detector (SVD), which is a type of silicon strip detector and responsible for particle decay vertex reconstruction in cooperation with the Pixel Detector (PXD), has high position resolution of a few tens of micrometers for charged particles. However, it has no function for the Level-1 trigger. The Thin Fine-Pitch SVD (TFP-SVD), which is being developed as the next generation vertex detector, will have higher position resolution than the current SVD and have the ability to output signals that can be used for the Level-1 trigger. With the aim of developing a new trigger system that can reject Off-IP particles efficiently and suppress the background trigger rate, this thesis develops the trigger algorithm using the TFP-SVD detector by simulation and reports the results of its performance evaluations. Furthermore, the feasibility of the TFP-SVD trigger system as firmware is also verified after

the simulation study.

This thesis consists of 8 chapters including this introduction. Chapter 2 explains the configuration and features of the Belle II experiment. Chapter 3 evaluates the future Level-1 trigger rate and proposes a new sub-trigger system using the TFP-SVD. The trigger algorithm developed in simulation is described in Chapter 4. In order to evaluate the performance of the algorithm, Chapter 5 considers the test cases and Chapter 6 shows the results. Chapter 7 confirms the feasibility of its implementation. In Chapter 8, we summarize this thesis with description of our achievements.

Chapter 2

The Belle II experiment

In this chapter, the accelerator and the sub-detectors of the Belle II experiment are described, emphasizing important features. In particular, the Silicon Vertex Detector (SVD), beam background, and the Level-1 trigger system are elaborated since they are closely related to our study. Furthermore, the ongoing TFP-SVD plan, which aims to upgrade the SVD, is also described.

2.1 SuperKEKB

The SuperKEKB collider shown in Fig. 2.1 is an accelerator using electron and positron beams. The center-of-mass energy $\sqrt{s}$ is set to 10.58 GeV, which is the $\Upsilon(4S)$ resonance energy, to study $B\bar{B}$ pairs produced by the $\Upsilon(4S)$ decays. SuperKEKB consists of the linear accelerator (linac), the positron damping ring, and the two main storage rings (electron and positron rings). The ring for the 7 GeV electron beam is called the High Energy Ring (HER), while the ring for the 4 GeV positron beam is called the Low Energy Ring (LER). The asymmetric beam energies result in the Lorentz boost of the e^+e^- center-of-mass system with the boost factor of $\beta\gamma = 0.28$. The radio frequency (RF) of the accelerating cavities in the linac alternately generates phases that accelerate and decelerate particles. Therefore, particles in the beam locally gather and form "bunches". Dipole and quadrupole magnets are installed in the main ring to control the orbits and emittances of the electron and positron beams. In particular, the magnets for the final beam focusing are called QCS. The electron and positron beams circulate in the main rings and collide at one interaction point (IP), which is surrounded by the Belle II detector.

The luminosity $\mathcal{L}$ of the beam crossing in a collider is given by the following formula, assuming flat beams and equal horizontal and vertical beam sizes for two beams at the IP [4]:

$$\mathcal{L} = \frac{\gamma_\pm}{2er_e}\frac{I_\pm\zeta_{y\pm}}{\beta^*_{y\pm}}\frac{R_L}{R_{\zeta_y}} \tag{2.1}$$

where γ, e, and r_e are the Lorentz factor, elementary electric charge, and electron classical radius, respectively, I is the beam current, ζ_y is the vertical beam-beam parameter, β^*_y is the vertical beta function at the IP, and R_L and R_{ζ_y} represent the reduction factors for the luminosity and the vertical beam-beam parameter, which arise from the crossing angle and the hourglass effect. The suffix "$\pm$" specifies the positron(+) or electron($-$). According to Eq. (2.1), if β^*_y becomes smaller, the luminosity becomes higher. However, it is limited by the

length of the bunch σ_z.

$$\beta_y^* > \sigma_z \tag{2.2}$$

SuperKEB adopts the "Nano-Beam" scheme [5]. The basic idea of the scheme is to squeeze the β_y^* by minimizing the longitudinal size of the overlap region of the two beams, which is the effective bunch length d. In the scheme, two bunches collide with large crossing angle of $2\phi = 83\,\mathrm{mrad}$, resulting in a small effective length. Fig. 2.2 shows a schematic of the beam collision in the Nano-Beam scheme. In this case, the lower limit of the β_y^* is given by

$$\beta_y^* > d \approx \frac{\sigma_x^*}{\phi} \tag{2.3}$$

where σ_x^* is the horizontal beam size at the IP, and becomes much smaller than the actual bunch length σ_z. The design machine parameters of the SuperKEKB collider are shown in Table 2.1.

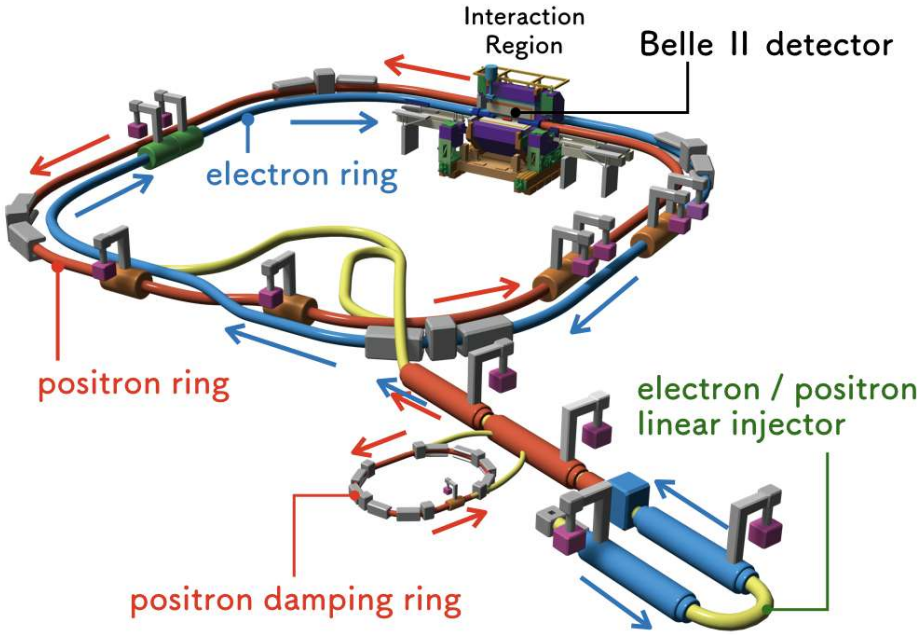

Figure 2.1: The SuperKEKB collider

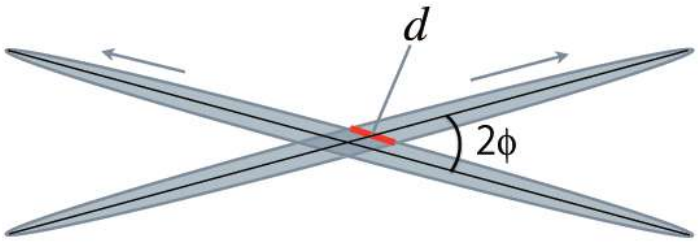

Figure 2.2: Schematic of the Nano-Beam scheme

Table 2.1: Design machine parameters of the SuperKEKB collider [6]

	LER (e^+)	HER (e^-)
Beam energy [GeV]	4	7
Beam current I [A]	3.60	2.62
Number of bunches	2500	2500
Vertical beam-beam parameter ζ_y	0.0881	0.0807
Vertical beta function β_y^* [mm]	0.27	0.30
Bunch length σ_z [mm]	6.0	5.0
Luminosity [$\mathrm{cm^{-2}s^{-1}}$]	8×10^{35}	

At first, SuperKEKB is designed to achieve the luminosity of $8.0 \times 10^{35}\,\mathrm{cm^{-2}s^{-1}}$ to accumulate the integrated luminosity of $50\,\mathrm{ab^{-1}}$ in about 15 years. However, after the operation of the accelerator for several years, the recent target luminosity is set to $6.0 \times 10^{35}\,\mathrm{cm^{-2}s^{-1}}$ maintaining the target integrated luminosity of $50\,\mathrm{ab^{-1}}$. The luminosity projection of SuperKEKB is shown in Fig. 2.3.

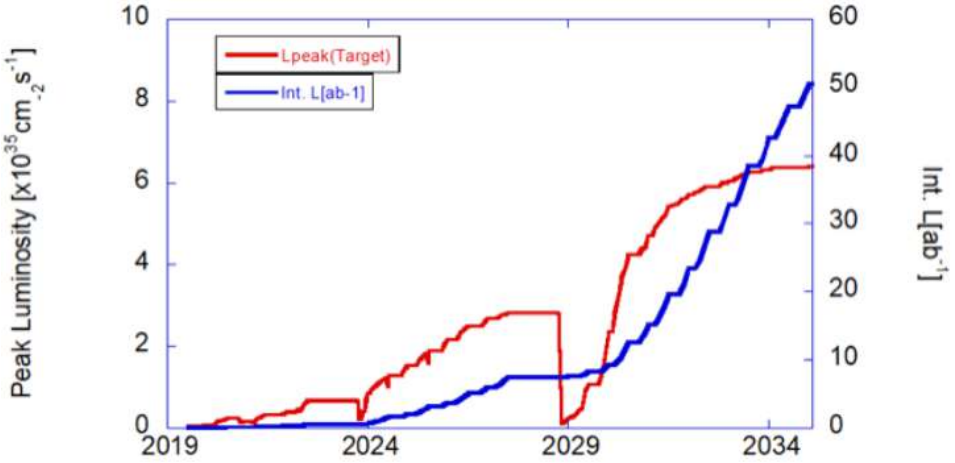

Figure 2.3: Luminosity projection of SuperKEKB [7]. The blue line represents the integrated luminosity, and the red line represents the instantaneous luminosity.

2.2 Belle II detector

As shown in Fig. 2.4, the Belle II detector [4] surrounds the IP and consists of seven sub-detectors: Pixel Detector (PXD), Silicon Vertex Detector (SVD), Central Drift Chamber (CDC), Time of Propagation counter (TOP), Aerogel Ring Imaging Cherenkov counter (ARICH), Electromagnetic Calorimeter (ECL), and K_L^0 and μ detector (KLM). Each sub-detector detects particles produced by the e^-e^+ collisions and measures their various properties. A superconducting solenoid magnet is placed between the ECL and KLM, generating a 1.5 T magnetic field along the beam axis. The magnetic field bends trajectories of charged particles, allowing the measurement of their momenta and signs of charge.

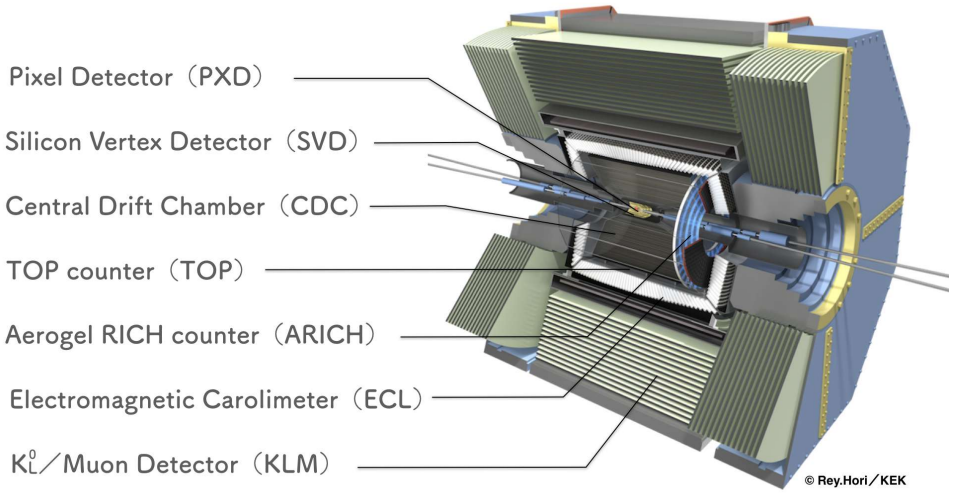

Figure 2.4: The Belle II detector

The global coordinate system of the Belle II detector is set as a right-handed Cartesian system with the origin at the IP. As shown in Fig. 2.5, z-axis points toward the angle bisector of the outgoing HER beam and incoming LER beam. The radius r, polar angle θ, and azimuthal angle ϕ are defined as

$$\begin{aligned} r &= \sqrt{x^2 + y^2} \\ \theta &= \arccos\left(z/\sqrt{x^2 + y^2 + z^2}\right) \\ \phi &= \arctan\left(y/x\right). \end{aligned} \tag{2.4}$$

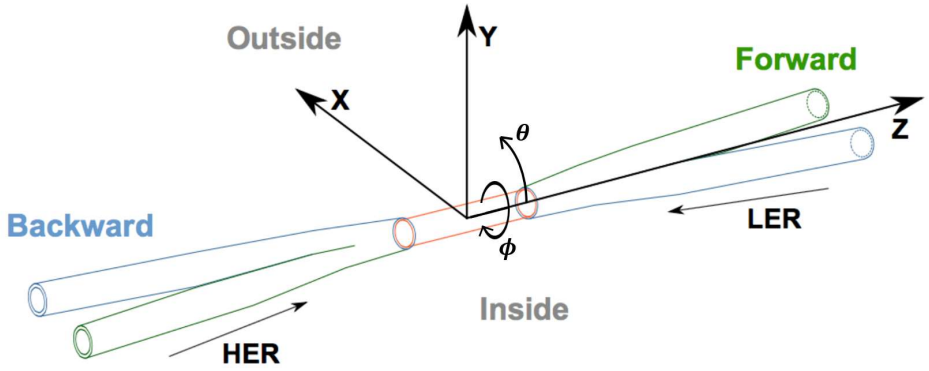

Figure 2.5: The global coordinate system of the Belle II detector

Each sub-detector is introduced below. The SVD is explained in detail in Section 2.3.

PXD The PXD is the innermost sub-detector of the Belle II detector and constitutes the Vertex Detector (VXD) together with the SVD. It consists of two layers of silicon pixel sensors, whose radii are 14 mm and 22 mm. The sensors are fabricated based on the Depleted P-channel Filed Effect Transistor (DEPFET) technology, which is a semiconductor detector concept that combines the signal detection and amplification within one device, allowing for very thin (50 μm) sensors. The size of each pixel is $50 \times 55\,\mu\mathrm{m}^2$ for inner layer and $50 \times 75\,\mu\mathrm{m}^2$ for outer layer.

CDC The CDC mainly plays two important roles. First, it reconstructs charged particle trajectories and measures their momenta precisely. Second, it provides particle identification measuring energy loss within its detector volume. Low momentum particles which do not reach the outer particle identification detectors (the TOP or ARICH) can be identified using the CDC. The CDC has more than 56,000 wires basically stretched in the z direction, filled with the gas mixture of 50 % He and 50 % C_2H_6. A high voltage ($> 30\,\mathrm{kV/cm}$) is applied to those wires: the anode wires are called the "sense wire"s and the cathode wires are called the "field wire"s. The CDC has 14,336 sense wires and 42,240 field wires. If charged particles interact with and ionize the gas, ionized electrons are accelerated toward the sense wires by the electric field impressed between the sense wires and field wires. The accelerated electrons ionize other atoms, and the secondary electrons further ionize other atoms, resulting in an electron avalanche. The avalanche induces current in the wires and the front-end electronics detect the signals. The ionized location due to the incident particle is detected by measuring the drift time from the ionized location to the sense wires, which is basically proportional to the distance between the two locations.

Fig. 2.6 shows the cross-sectional view of the CDC on the $r - z$ plane. The CDC has 56 layers of sense wires, each layer has 160 – 384 sense wires. The 56 layers are divided into 9 "Super Layer (SL)"s: the innermost SL has 8 layers and each of the outer 8 SLs has 6 layers. The SLs are numbered from inner to outer as SL0, SL1, $\cdots$, SL8. In the even-numbered SLs represented by solid line in Fig. 2.6, all wires are strung exactly along the z-axis to reconstruct the 2-dimensional tracks (2D tracks). These SLs and their wires are called the "axial" layers

and "axial" wires. In the odd-numbered SLs represented by dashed line in the figure, all wires slightly deviate from z-axis to reconstruct the 3-dimensional tracks (3D tracks) by combining them with axial wires. These SLs and their wires are called the "stereo" layers and "stereo" wires. Moreover, the concept of "cell" is defined as a set of each sense wire and 8 field wires surrounding that sense wire. As shown in Fig. 2.7, the field wires are shared by adjacent cells. The smaller the cell size is, the shorter the maximum drift time and the lower the beam background influence. Since the innermost super layer (SL0) is exposed to an intense beam background, the cell size in the SL0 is about half of that in the outer SLs.

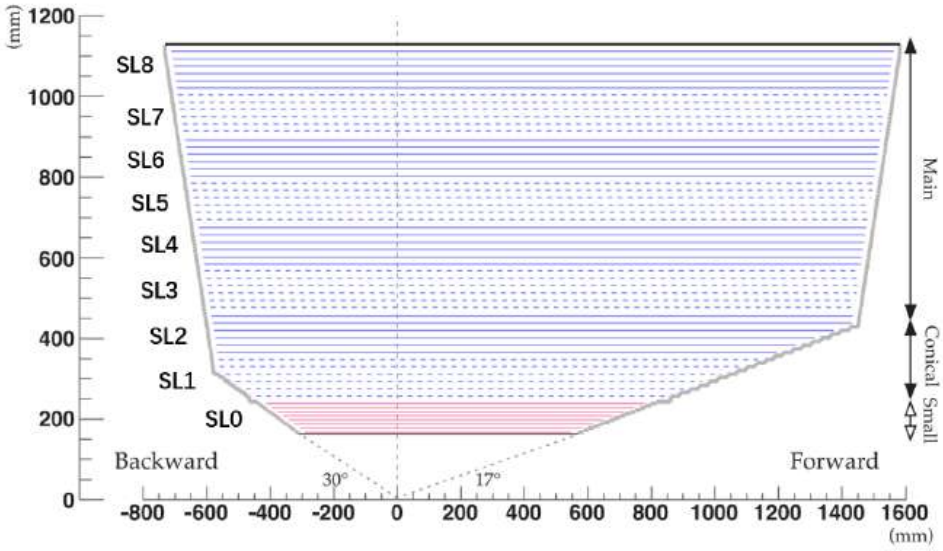

Figure 2.6: Cross-sectional view of the CDC on the $r-z$ plane. The solid lines represent axial layers and the dashed lines represent stereo layers.

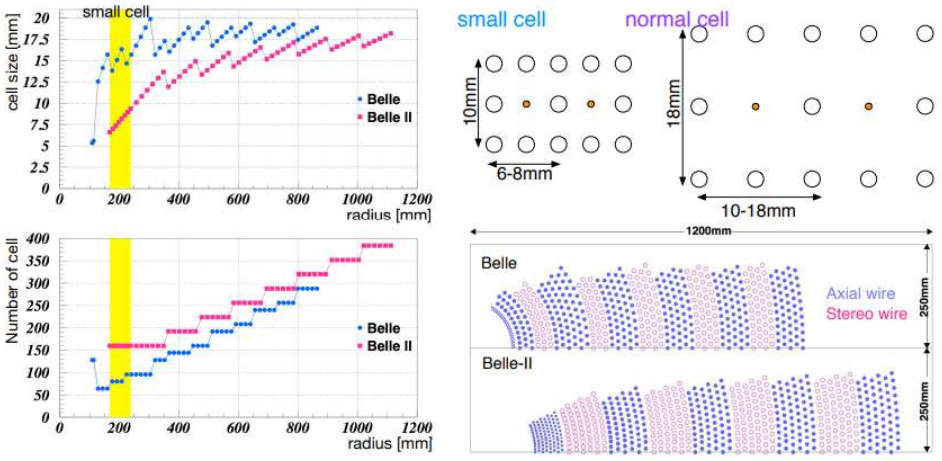

Figure 2.7: The cell size (upper left), the number of cells (lower left), and the structure of the cells on the $x-y$ plane (right) are shown [8]. In the upper right figure, sense wires are represented by orange points and field wires are represented by white circles.

TOP The TOP is placed in the barrel region outside of the CDC and responsible for particle identification of $K^{\pm}$ and $\pi^{\pm}$. The TOP measures the time of propagation of the Cherenkov photons internally reflected inside a quartz radiator. The micro-channel plate photomultiplier tubes (MCP-PMTs), installed at the end surfaces of the quartz, reconstructs the Cherenkov image from the 3-dimensional information provided by the two-diensional local coordinate (x, y) and precise timing. The time information with high resolution better than 50 ps provided by the MCP-PMTs is also used as good timing trigger at the Level-1 trigger system.

ARICH The ARICH is placed in the foward end-cap and responsible for particle identification of $K^{\pm}$ and $\pi^{\pm}$ as well as the TOP. In the ARICH, a charged particle passing through a silica aerogel radiator produces the Cherenkov photons. The Hybrid Avalanch Photo Detector (HAPD) reconstructs the Cherenkov ring image and separates $K^{\pm}$ from $\pi^{\pm}$ by the difference in the Cherenkov angles.

ECL The ECL consists of 6624 CsI(Tl) crystals placed in barrel section with an inner radius of 1.25 m, and 2112 CsI(Tl) crystals placed in end-caps at $z = 1.96$ m (forward) and $z = -1.02$ m (backward). The PIN photo-diodes detect the scintillation light which determines energies and angular coordinates of electrons and photons.

KLM The KLM consists of an alternating sandwich of iron plates and active detector elements, which are located outside of the superconducting solenoid. It has 15 detector layers and 14 iron plates in the barrel region, and 14 detector layers and 14 iron plates in each end-cap. The iron plates serve as the magnetic flux return for the solenoid. Muons traverse the KLM along nearly straight lines, while hadrons cause nuclear interactions in the iron plates. The detectors, which consist of Resistive Plate Chambers (RPCs) and plastic scintillators, detect the difference in the trajectories of the particles and identify the muons. On the other hand, K^0_L mesons are identified by detecting hadronic showers induced by the nuclear interactions.

2.3 Silicon Vertex Detector (SVD)

The SVD [9] constitutes the outer four layers of the VXD and contributes to inner tracking, estimation of the region-of-interest (RoI) on the PXD sensors, and particle identification by energy loss measurements. The whole VXD structure is shown in Fig. 2.8. In the VXD, the inner two layers named as layer 1 and 2 are the PXD and the outer four layers named as layer 3 – 6 are the SVD. Each SVD layer consists of 7 – 16 "ladder"s, and 2 – 5 sensors are mounted on each ladder. As shown in Fig. 2.9, the ladders are located cylindrically and their radii are 39 mm, 80 mm, 104 mm, and 135 mm, respectively. These ladders are numbered counterclockwise when viewed from the LER beam axis. Fig. 2.10 shows the cross-section of the SVD. The sensors are named FW, +Z, CE, -Z, and BW according to their positions on the ladders.

In order to minimize the multiple scattering for high precision reconstruction of particle tracks, the number of layers is reduced by orthogonally implanting strips on both sides of the sensor. The sensor based on this technology is called the Double-sided Silicon Strip Detector (DSSD) sensor. In addition, to suppress the electrical noise level, a "chip-on-sensor" concept is employed to implement the front-end readout electronics. They are explained in the following sections.

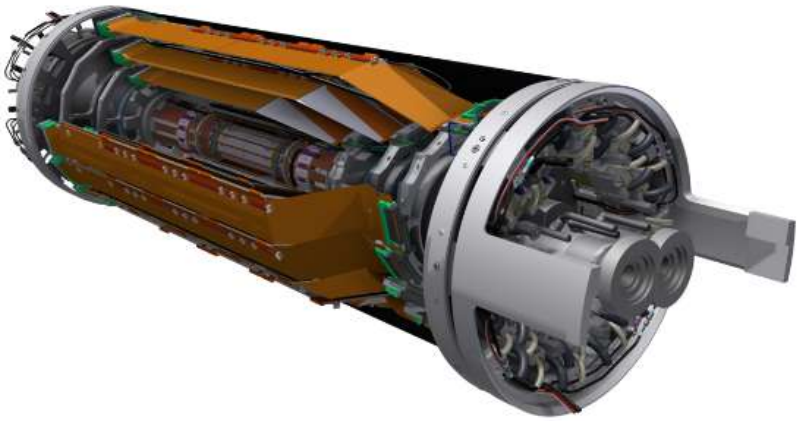

Figure 2.8: Vertex Detector (VXD)

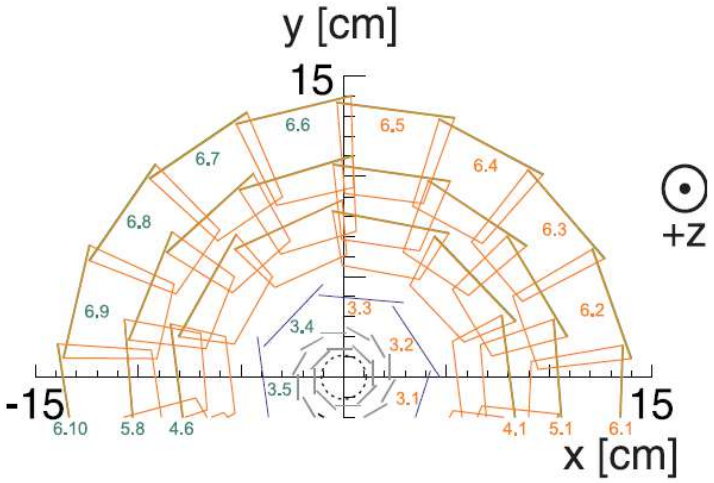

Figure 2.9: Cross-section of the VXD on the $x - y$ plane. The layer 1 – 2 are the PXD and the layer 3 – 6 are the SVD

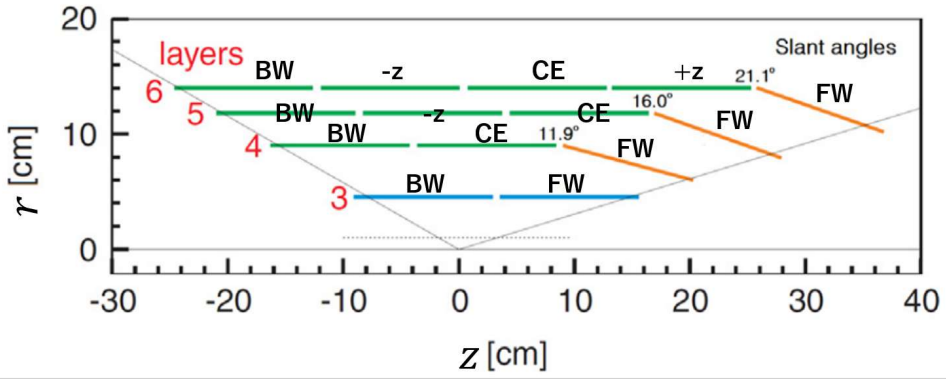

Figure 2.10: Cross-section of the SVD on the $r - z$ plane

2.3.1 Double-sided Silicon Strip Detector (DSSD)

The structure of the DSSD is shown in Fig. 2.11. The DSSD sensor used in the SVD is made of the n-type silicon substrate, on which more deeply doped strips on the top and bottom sides of the sensor bulk are implanted perpendicular to each other. The p^+-strips are called the P-strips and the n^+-strips are called the N-strips. It is known that an electron accumulation layer is created under the bulk-SiO_2 interface. It reduces the interstrip resistance between N-strips and results in the charge sharing among those strips [10]. Therefore, p^+-strips, called p-stops, are implanted between N-strips to insulate them and avoid the charge sharing in the N-strips. The readout aluminum (Al) electrodes are placed on every other strips. The strips on which the readout electrodes are not placed are called floating strips. The thickness of the DSSD sensor is 300 μm and 320 μm. The material budget per layer corresponds to approximately 0.7 % of the radiation length. The geometrical details of the DSSD are shown in Table 2.2.

An inverse bias voltage of 100 V is applied between P-strips and N-strips of the DSSD to fully deplete the bulk in the SVD operation. When a particle passes through the sensor, electron-hole pairs are produced along the particle trajectory. The electrons and holes drift toward N-strips and P-strips respectively by the impressed bias voltage, and then the current induced in the strips by the carrier migration is read out by the Al electrodes. The signals induced in the floating strips are read out by the neighboring readout electrodes. P-strips provide ϕ information and N-strips provide z information, offering the 2-dimensional particle positions.

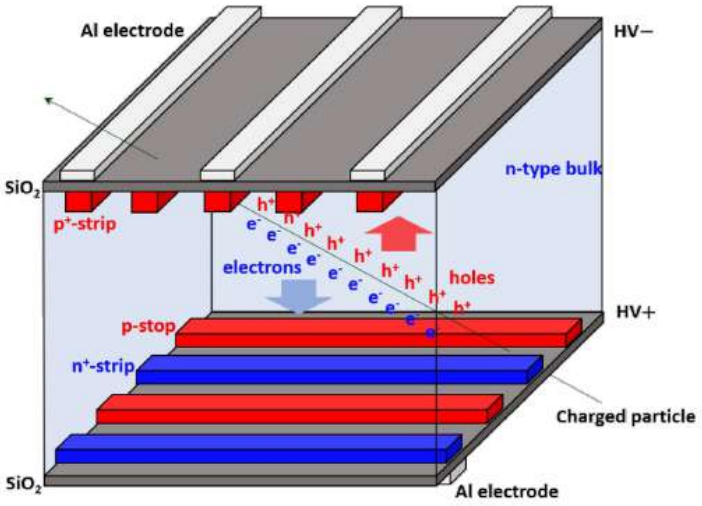

Figure 2.11: Structure of the DSSD sensor

Table 2.2: Geometrical details of the DSSD sensors used in the SVD

	Small rectangular	Large rectangular	Trapezoidal
Location	Layer 3	Layer 4–6 (except FW)	Layer 4–6 (FW)
Active area [mm^2]	122.90×38.55	122.90×57.72	$122.76 \times (38.42–57.59)$
Thickness	$320\,\mu$m	$320\,\mu$m	$300\,\mu$m
Number of readout P-strips	768	768	768
Number of readout N-strips	768	512	512
Pitch b/w readout P-strips	$50\,\mu$m	$75\,\mu$m	$50–75\,\mu$m
Pitch b/w readout N-strips	$160\,\mu$m	$240\,\mu$m	$240\,\mu$m

2.3.2 Front-end readout electronics: APV25

The signal generated in the strips of the DSSD is read out by APV25, which is a front-end ASIC (Application Specific Integrated Circuit) of the SVD [11]. APV25 is a low-noise charge sensitive amplifier chip designed with the 250 nm CMOS technology, and it is characterized by fast signal shaping time, good time resolution, and strong radiation tolerance. However, faster shaping time causes larger noise. In order to suppress the noise to an acceptable level, readout chips should be placed as close to the sensor as possible. For this reason, APV25 is located on a flexible circuit placed on top of the sensor. There is a layer of foam between the flexible circuit and the sensor for electrical and thermal insulation.

APV25 has 128 input channels. The internal circuit of each channel is shown in Fig. 2.12. A Minimum Ionising Particle (MIP) generates about 25,000 electron-hole pairs in the DSSD volume. First, the charge signal induced by them is amplified by a pre-amplifier (preamp). Depending on the type of the carrier (electron or hole), opposite signal polarities arrive at the input of the preamp. In order to reduce power supply range while maintaining the capability to handle both signal polarities, an optional inverter is introduced after the preamp, by which signal polarity is always positive at the subsequent circuit. The following block is a CR-RC shaper to shape the amplified signal. The shaper output is stored to the pipeline of 192 analog cell memories at a frequency of 31.8 MHz, 1/16 of the SuperKEKB RF clock of 509 MHz. The pipeline serves as a ring buffer memory, in which the stored samples are held until readout due to the arrival of the trigger signal or overwritten by new samples. If a sample is read out, its voltage is converted into a current at APSP (Analog Pulse Shape Processor). The samples from all 128 channels are serialized at the MUX (Multiplexer), then output with 12-bit digital header (3 start bits, 8 bits for readout cell address, and one error bit). Fig. 2.13 shows the output from one APV25, which consists of 12-bit and sequential 128 analog values.

There are two data taking modes: 6-sample mode and 3-sample mode. In the 6(3)-sample mode, six(three) cells of data are read out in one event. For the 6(3)-sample mode, when the Level-1 trigger signal (Section 2.6) arrives, the 6(3) cells that are requested for output are protected in order not to be overwritten before the readout is completed. The addresses of the protected cells are recorded in 32-depth FIFO (First-In First-out). If other trigger arrives before the previous readout processing is completed, additional other 6(3) cells are protected. The maximum number of protected cells is 32 due to the depth of the FIFO. Thus, the maximum available pipeline depth to wait for the Level-1 trigger arrival is 160 ($= 192 - 32$), which leads the maximum trigger latency time of $5.0\,\mu$s ($\approx 160 \times 1/31.8\,$MHz).

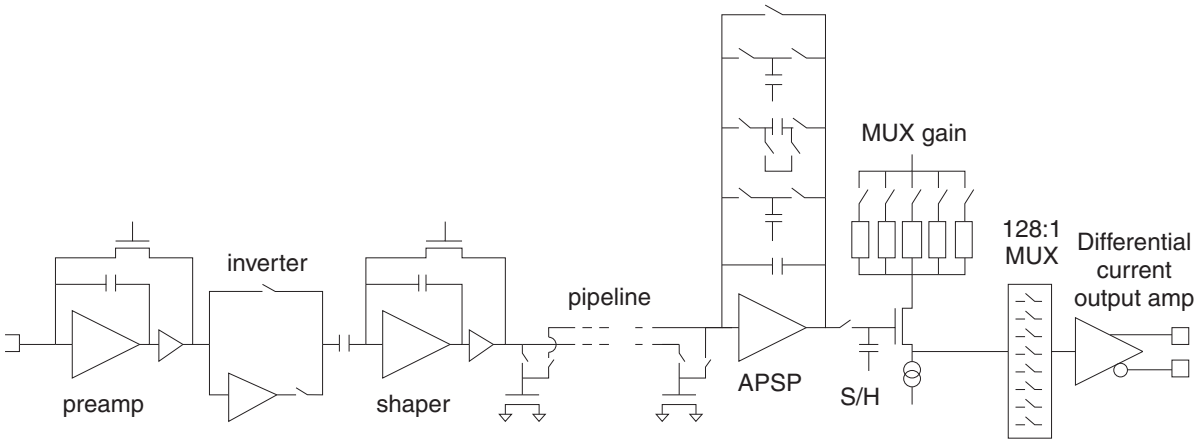

Figure 2.12: Block diagram of one channel in APV25

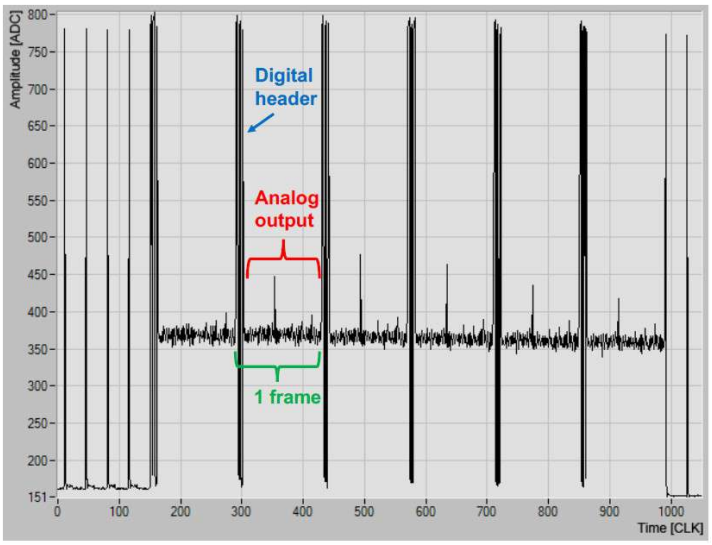

Figure 2.13: Output data from APV25 [12]. The horizontal axis shows time counted by the clock of 31.8 MHz.

2.3.3 Readout chain of the SVD data

The main elements of the SVD readout chain are shown in Fig. 2.14. APV25 outputs are sent to the junction boards located in the DOCKs, which are space reserved for interconnections of cables and services, close to the CDC end-plates. The junction boards are also connected to power supply required for the sensor bias and the APV25 power. After the junction boards, the outputs are sent to the FADC (Flash Analog to Digital Converter) boards located on top of the Belle II detector, in which the analog data is digitized. In the digitization process, an online "zero-supression" processing is performed. In this process, the strip signal is converted in the unit of the electrical noise on the strip, called signal-to-noise ratio (SNR), and the

strip is classified into a "fired" strip when either of samples in the strip signal exceeds a given threshold, otherwise classified into an "unfired" strip. Only the fired strips are transferred to the subsequent pipeline toward the Data-Acquisition (DAQ) system (Section 2.5). The electrical noise is evaluated for each strip as the root mean square (RMS) of the pedestal signals. The SNR threshold is common for all of the strips, and the current value for the online zero-suppression is 3.0 SNR.

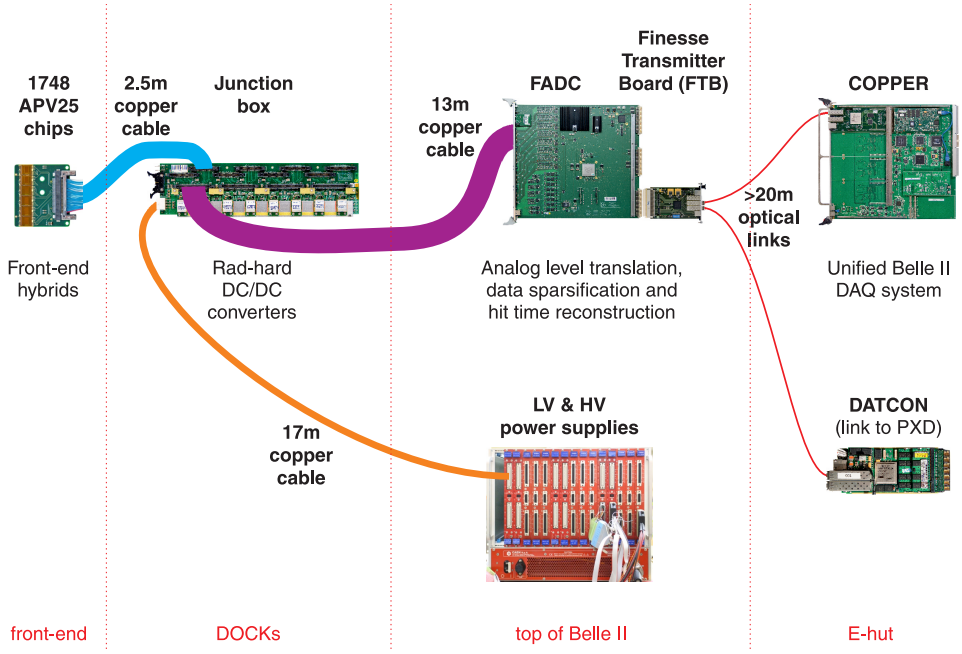

Figure 2.14: Readout chain of the SVD data

2.4 Beam background

The purpose of the Belle II detector is to detect particles produced by the electron-positron beam collision at the IP. However, the beam particles sometimes deviate their design orbits and hit the beam pipe, generating electromagnetic showers. The particles produced by the showers can intrude into the detector volume and make noise signals in the sensors. They are called beam background particles. The beam background can cause serious problems such as radiation damage in sensors, bad reconstruction purity, high fake trigger rate, and DAQ throughput saturation.

2.4.1 Beam background sources

Depending on its production process, beam background can be divided into single-beam background and luminosity background. The single-beam background is caused by interactions of the electron or positron beam that can happen even without the opposite beam. On the other hand, the luminosity background is induced by the collision of the electron and positron beams, thus it is also called collision background.

The single beam background is mainly categorized into three components, Touschek scattering, beam-gas scattering, and synchrotron radiation, while the luminosity background is categorized into two components, two-photon process and radiative Bhabha scattering.

Touschek scattering Touschek scattering is a scattering process between particles within a beam bunch. Some of the scattered particles deviate their orbit and hit beam pipe or magnet walls. The amount of Touschek scattering from all bunches is proportional to

$$\frac{I^2}{\sigma_x \sigma_y \sigma_z n_b E^3} \tag{2.5}$$

where I is the beam current, σ_y is the vertical bunch size, n_b is the number of beam bunches, and E is the beam energy [4]. Since the beam size in the nano-beam scheme is very small ($\sigma_y \approx 50\,\mathrm{nm}$), the effect from Touschek scattering is important. Moreover, it is more important for the LER than the HER due to their asymmetric energy.

Beam-gas scattering Beam-gas scattering is an interaction between the beam particles and the molecules of the residual gas in the beam pipe, which changes the beam particle momenta. Beam-gas scattering is caused by Coulomb scattering and Bremsstrahlung process. The coulomb scattering changes particle trajectories directly through electromagnetic interaction. The bremsstrahlung is a higher order effect in a strong electric field, in which charged particles lose their energy with the radiation of photons. The event rate of the bremsstrahlung is low and low-momentum particles are stopped by collimators in the main ring. Hence, the coulomb scattering is the main source of the beam-gas background. The beam-gas scattering effect is proportional to the beam current I and the vacuum pressure P inside the beam pipe. The P has linear dependency on the I. Therefore, the beam-gas scattering is almost proportional to the square of the I similarly to the Touschek scattering.

Synchrotron radiation Synchrotron radiation (SR) is a electromagnetic radiation emitted when relativistic charged particles are accelerated by a magnetic field. Since the SR power is proportional to the beam energy squared and magnetic field squared, the effect is more important for the HER than the LER. The energy spectrum of the SR photons ranges from a few keV to tens of keV, and its contribution to the detector background is predicted to be negligible [13, 14].

Two-photon process Two-photon process $e^+e^- \to e^+e^-e^+e^-$ produces low-momentum electron-positron pairs. The Feynman diagram of this process is shown in left side of Fig. 2.15. The low-momentum particles spiral inside the SVD volume by the magnetic field and make many hits on the sensors. The two-photon process is the largest component of the luminosity background for the SVD. The rate of the two-photon process is proportional to the luminosity $\mathcal{L}$.

Radiative Bhabha scattering Radiative Bhabha process $e^+e^- \to e^+e^-\gamma$ produces photons through the process shown in the right side of Fig. 2.15. It is the second largest component of the luminosity background on the SVD. The photons from this process fly in the direction of the beam axis and interact with the materials, resulting in electromagnetic showers. In

addition, electrons and positrons losing their energy are bent their trajectories by QCS placed around the interaction region (IR) and hit the walls of magnets, where electromagnetic showers are generated. The rate of the radiative Bhabha scattering is also proportional to the luminosity $\mathcal{L}$.

Radiative Bhabha process is classified according to the scattering angle of electron or positron ($\theta_{e^\pm}$). If one of the $\theta_{e^\pm}$ is larger than 10° and the other is larger than 1°, the event is called "BHWideLargeAngle (BHWide LA)". If the event is not BHWide LA and both of the $\theta_{e^\pm}$ are larger than 0.5°, it is called "BHWide". In other cases, it is called "RBB".

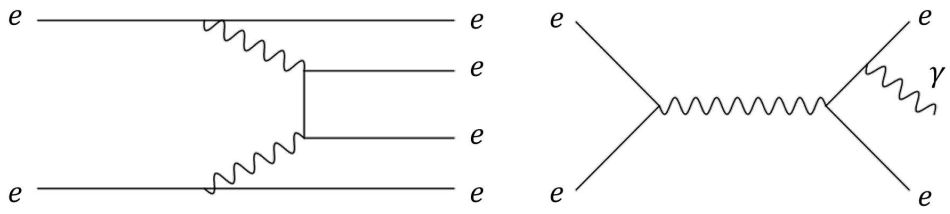

Figure 2.15: Feynman diagrams of the luminosity backgrounds. The left diagram shows two photon process and the right diagram shows radiative Bhabha scattering.

2.4.2 Geometrical distribution of beam background

Spatial distribution of production positions of charged particles was studied in Ref. [15]. In Fig. 2.16, two obvious hot spots can be seen at $z = 0.6\,\mathrm{m}$ and $z = 1.1\,\mathrm{m}$. The location of these spots corresponds to the LER beam pipe. Since the beam size needs to be widened once in QCS located around $z = 1.1\,\mathrm{m}$ in order to be focused at the IP, the diameter of the beam pipe around $z = 1.1\,\mathrm{m}$ is small relative to the beam size. Therefore, background events are expected to be generated there. There is another hot spot around $z = 0.6\,\mathrm{m}$ because no background shields such as tungsten shields are located there. Such particles produced outside of the IP are called the "Off-IP particle"s, which are expected to be the major background source. In contrast to them, the particles produced at the IP are called the "On-IP particle"s.

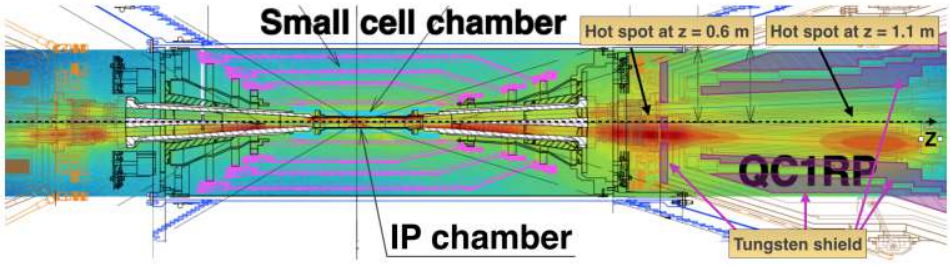

Figure 2.16: Top view of the vertices reconstruction studies in 2019 [15]. Hot spots in the forward region correspond to locations where many background events are generated.

2.4.3 Injection beam background

Regarding the beam injection, SuperKEKB adopts the "continuous injection scheme", in which beams are injected at a frequency of 50 Hz in parallel with the data taking for the efficient data

acquisition. The injected beams are unstable and produce more background in the detectors for a brief interval ($\sim 100\,\mu$s) after each injection. Thus, the events right after the injections, which include more background noise, are vetoed and not sent to the Data-Acquisition system (Section 2.5).

2.5 Data-Acquisition (DAQ) system

The Data-Acquisition (DAQ) system reads out signals from the sub-detectors and records the data. However, the data from the Belle II detector are enormous (of course, background events greatly contribute to it) and all of them cannot be recorded due to the limitation of the storage capacity and the bandwidth of the data transfer. For this reason, the Belle II experiment employs the trigger system to select physics events to be recorded in the DAQ. The trigger system of Belle II has two stages: the Level-1 trigger, described in Section 2.6, performs first selection of the events, and then the High-Level Trigger (HLT), which is the online software trigger, further reduces the data volume.

Fig. 2.17 shows the conceptual design of the Belle II DAQ system. The front-end electronics and digitizers are placed nearby the corresponding sub-detectors. The digitized data of each sub-detector are temporarily stored in its buffer memory. The timing distribution system distributes the 127 MHz clock, Level-1 trigger signal, and other control signals to all the sub-detector readout boards and COPPER (COmmon Pipeline Platform for Electronics Readout) boards through the FTSW (Frontend-Timing-SWitch) modules.

After receiving the Level-1 trigger signal, the data stored in the local memory of each sub-detector except for the PXD are transferred into COPPER boards through optical fibers using the Belle2Link, a homemade data transfer protocol. The data are then formatted by the on-board CPU and sent to the readout PCs via the GbE (Gigabit Ethernet) links. After the preliminary event reconstruction in Event Builder 1, the full event reconstruction is performed in the HLT servers, where high-level trigger decision is made. The selected data are sent to Event Builder 2 [16]. The data from the PXD are so large that it waits for the reconstructed information from the HLT. By using the RoI information from the HLT, the PXD data of about 1 MB are reduced by a factor of 10. Finally, the reduced PXD data are merged with the HLT processed data and recorded in the storage of the DAQ. The maximum record rate of the fully reconstructed data is designed to be 1.8 GB/s. The designed performance for the DAQ is summarized in Table 2.3.

Table 2.3: Designed performance for the DAQ [17]

	Maximum value
Level-1 trigger rate	30 kHz
Event size except the PXD	1 MB
Data flow after Level-1	30 GB/s
PXD data reduction rate	1/10
HLT rate reduction rate	1/3 - 1/6
Data record rate	1.8 GB/s

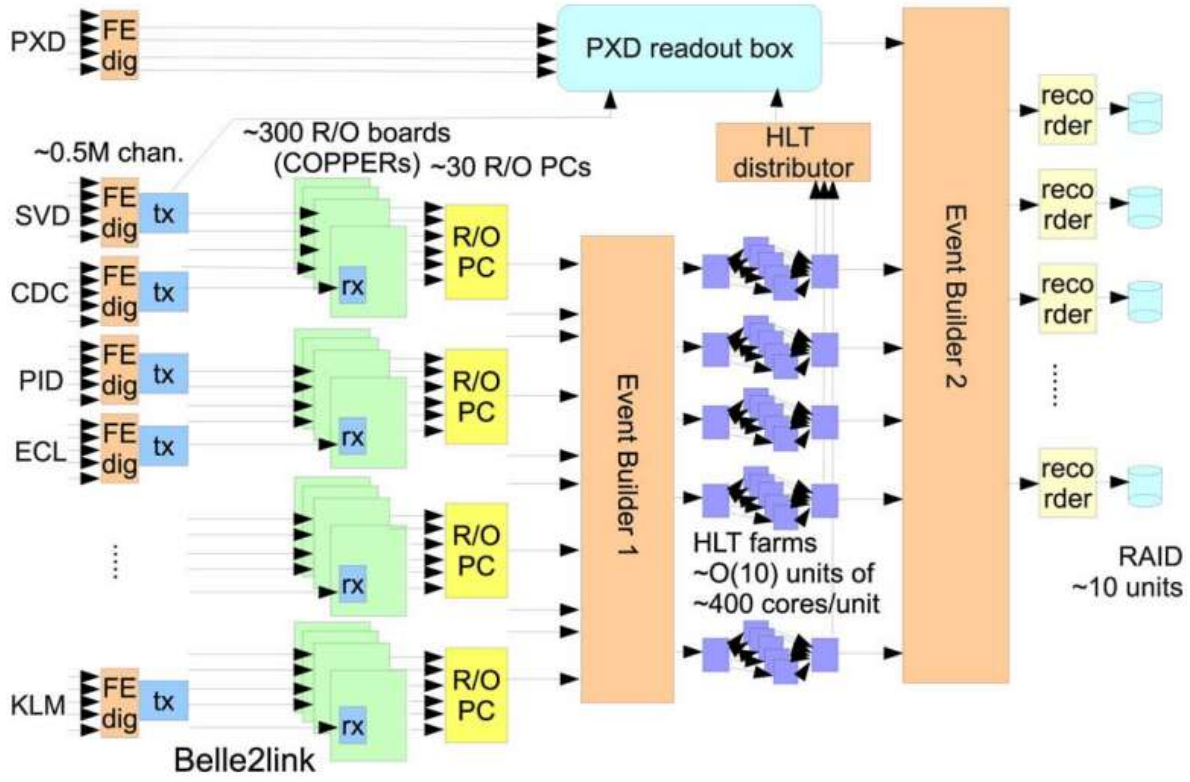

Figure 2.17: Conceptual design of the Belle II DAQ system [16]

2.6 Level-1 trigger system

The Level-1 trigger is the first-level trigger system of the Belle II experiment. The requirements are summarized in Table 2.4. The total cross sections at $\sqrt{s} = 10.58\,\text{GeV}$ and trigger rates at the designed luminosity of $8.0 \times 10^{35}\,\text{cm}^{-2}\text{s}^{-1}$ for physics events of interest are listed in Table 2.5. Since the trigger rate due to physics events of interest is estimated to be 15 kHz, the trigger rate due to background events must be less than 15 kHz to meet the limit of the trigger rate of 30 kHz.

Table 2.4: Requirements for the Level-1 trigger [4]

	Requirement
Maximum average trigger rate	30 kHz
Fixed latency	4.2 μs
Minimum two-event separation	200 ns

Table 2.5: Cross sections $\sqrt{s} = 10.58\,\mathrm{GeV}$ and trigger rates at the designed luminosity [18]. The rates of Bhabha scattering and $\gamma\gamma$ event are pre-scaled by a factor of 100 because of their large cross sections.

	σ [nb]	Level-1 trigger rate [Hz]
$\Upsilon(4S)$	1.2	960
Hadron production from continuum	2.8	2200
$\mu^+\mu^-$	0.8	640
$\tau^+\tau^-$	0.8	640
Bhabha	44	350 (prescaled by 100)
$\gamma\gamma$	2.4	19 (prescaled by 100)
Two photon	~ 80	~ 10000
Total	67	~ 15000

2.6.1 Structure of the Level-1 trigger system

The Level-1 trigger system [4, 18] consists of four sub-trigger systems, Global Reconstruction Logic (GRL), and Global Decision Logic (GDL). The schematic overview of the system is shown in Fig. 2.18. The clock frequency used for the Level-1 trigger system is 127 MHz, which is one-forth of the RF frequency of SuperKEKB of 509 MHz. In the first step of the trigger system, several sub-triggers are generated by individual sub-detectors: the CDC sub-trigger, ECL sub-trigger, TOP sub-trigger, and KLM sub-trigger. The CDC trigger is also called "track trigger", which provides the charged track information on momentum, position, charge, and multiplicity. The details are described in Section 2.6.3. The event rate of the $B\bar{B}$ including photons in the final state is about 50 % of the total $B\bar{B}$ production. Therefore, as well as the CDC track trigger, the ECL trigger that is sensitive to the photons is also helpful to find the $B\bar{B}$ events. It provides the position, energy, and size of the ECL clusters. The trigger decision is made mainly by the CDC trigger and ECL trigger. The TOP trigger is used to precisely determine the event occurrence timing. The KLM trigger is used to identify muons, and its information is combined with the CDC and ECL triggers at the GRL, which performs particle identification for electron, photon, and other hadrons by combining the information from sub-triggers. The matching information from the GRL is expected to make the discrimination between low-multiplicity events and background events more efficient[*1]. The GDL receives signals from sub-triggers and from the GRL, and makes the final Level-1 trigger decision. The trigger signals of the different sub-triggers from the same event are generated at different timing. The GDL performs a timing adjustment to compensate for the different latencies before matching the sub-triggers and making the trigger decision. In the GDL, multiple trigger conditions called "trigger bit"s are set for various decay modes (Section 3.1): if either of the conditions is satisfied, the corresponding trigger bit is asserted and the Level-1 trigger signal is issued. The Level-1 trigger signal is designed to be output to the FTSW exactly 4.2 μs after the beam collision.

[*1] The decay event of τ or dark sector particle, which includes a small number of visible particles in the final state, are often confused with Bhabha event (elastic scattering between electron and positron without γ).

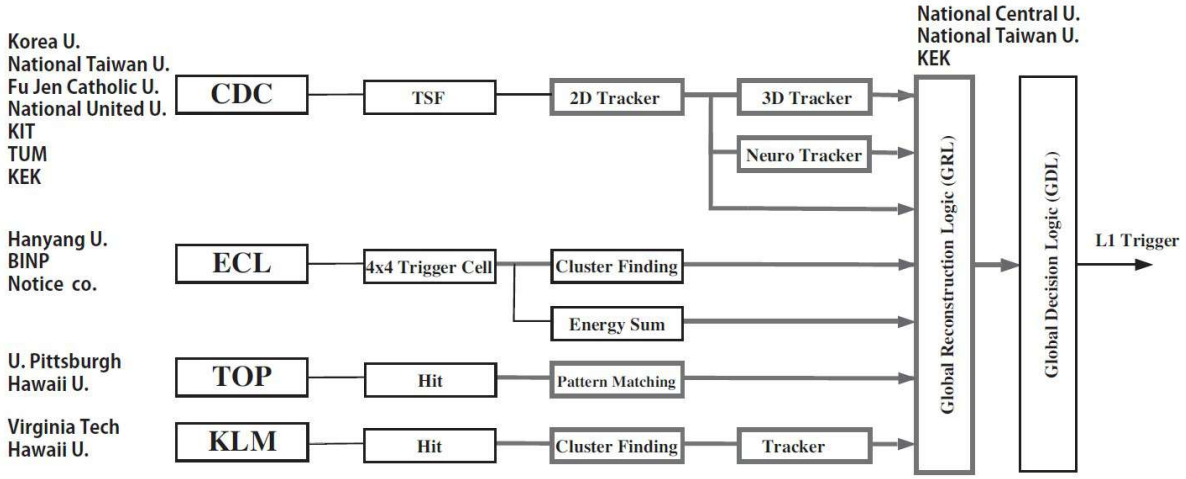

Figure 2.18: Schematic overview of the Level-1 trigger system

2.6.2 Universal Trigger board

The Universal Trigger (UT) board is developed to realize the following features required by the Level-1 trigger system [18].

1. FPGA (Field Programmable Gate Array) is introduced into the Level-1 trigger system so that the trigger logic can be changed to accommodate future situations without replacing hardware.

2. High-speed serial communication is used. In Belle, the data transfer between modules is performed using differential emmiter-coupled logic, which needs two signal lines per channel. The change of the communication method enables 100 times faster data transfer and reduces the number of signal lines by a factor of 10.

The current available UT boards are the UT3 (third generation of UT board), which was produced in 2012, and the UT4 (4th generation of UT board), which was produced in 2016. The specifications of the UT3 and UT4 are shown in Table 2.6. In the table, GTH, GTX, and GHY are protocols for the high-speed serial communication provided by Intel. Fig. 2.19 is a photograph of the UT4 board. Moreover, the development plan of the UT5, 5th generation of the UT board, is ongoing.

2.6.3 CDC sub-trigger

The CDC trigger [18, 17] is the main sub-trigger system and has the highest trigger rate among all the sub-triggers. Therefore, the CDC trigger impacts the performance of the Level-1 trigger system significantly. The configuration of the CDC trigger is shown in Fig. 2.20. The CDC trigger has two types of tracking systems: the 2D track trigger and 3D track trigger. Using the axial wires, the 2D track trigger measures the the number of charged particles, charge, transverse momentum[*2] p_{T}, and azimuthal angle ϕ. In addition to these information, by using

[*2]Transverse momentum is the component of three-dimensional momentum perpendicular to the z-axis

Table 2.6: Specifications of the UT3 and UT4

	UT3	UT4
model of FPGA	Xilinx Virtex6 XC6VHX380 / 565T	Xilinx Virtex Ultrascale XCVU080 / 160
The number of logic gates	382k / 580k	975k / 2026k
Band width of Opt module	530 Gbps	1300 Gbps
IO	GTH 11.18 Gbps × 24 lanes GTX 6.6 Gbps × 40 lanes	GTY 25 Gbps × 32 lanes GTH 15 Gbps × 32 lanes
Sub FPGA	-	Artix 7 XC7A15T (16k gates)

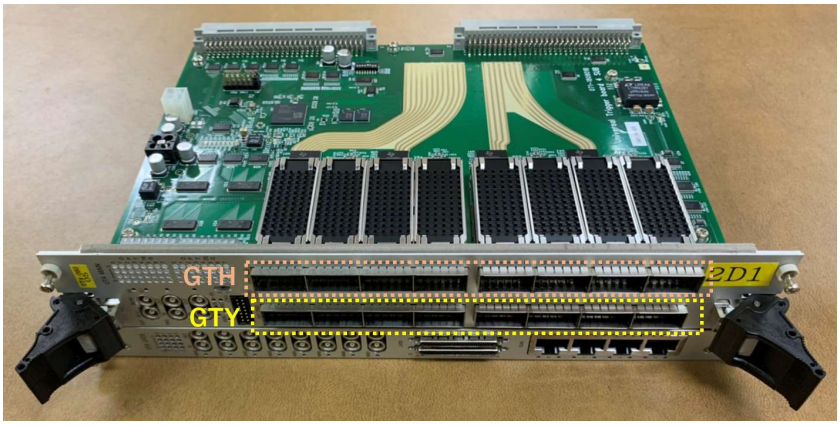

Figure 2.19: The photograph of the UT4 board

the stereo wires, the 3D track trigger measures the production z-positions of the particles, it is a very powerful tool to reject the Off-IP particles.

The CDC has 302 front-end electronics, each of which reads out the 48 sense wires. For the CDC trigger, 292 front-ends are used due to the high background rate in the inner most 3 layers. The clock frequency of the front-ends for the sub-trigger system is 31.75 MHz, one-fourth of 127 MHz. The Merger board merges the data from four CDC front-ends and sends the merged data to the Track Segment Finder (TSF) module.

By using the hit data from the Merger, "Track Segment" hits are formed by the TSF modules. The structures of TSFs are shown in Fig. 2.21. In the figure, each square represents a CDC cell, described in the CDC part of Section 2.2. Each TSF contains five layers. The TSF on the SL0 is shaped to be sensitive to the track from the IP. On the other hand, the TSFs on the other SLs is shaped to accommodate the curved track due to the magnetic field. The total number of TSFs is 2,336. Adjacent TSFs are located on the next cells, thus sharing the 10(6) same cells with each other for SL0(other SLs). The TSF is classified as a "track segment" if at least four out of the five layers have hits. The red cells represent the first priority cells, and the orange cells represent the second priority cells. If the first priority cell has a hit, the hit is called "priority hit". The information on the position and hit timing of the TSF is assumed to be that of its priority hit, and only the information of the priority hit is sent to

the subsequent tracking processing. If the first priority cell does not have hit, the hits of the second priority cells provide the information. If there is no hit on the first priority cell and the second priority cells, the information of TSFs is ignored. The overall arrangement of TSFs is shown in Fig. 2.22. TSFs are designed to reconstruct the track of charged particles with $p_{\mathrm{T}} > 0.3\,\mathrm{GeV}$.

Using the information from the 1,312 TSFs on the axial SLs, the 2D tracker module reconstruct the 2-dimensional track (2D track). Since a charged particle curves on the $x - y$ plane passing through the IP in the magnetic field, its track can be determined by identifying r and ϕ where r is the radius and ϕ is the azimuthal angle of the center of the circle. The information on the r and ϕ is determined from the track segment hits using "Hough Transformation" method [19]. Furthermore, 3-dimensional tracks (3D tracks) are reconstructed using 2D tracks and track segment hits of TSFs on the stereo SLs. In this calculation, the hit timing information is also used. After the 3D track trigger, the information on the full momentum including the z-component p_z and the production z position of the track Δz can be obtained, which is sent to the GRL for matching with the information from other sub-trigger systems.

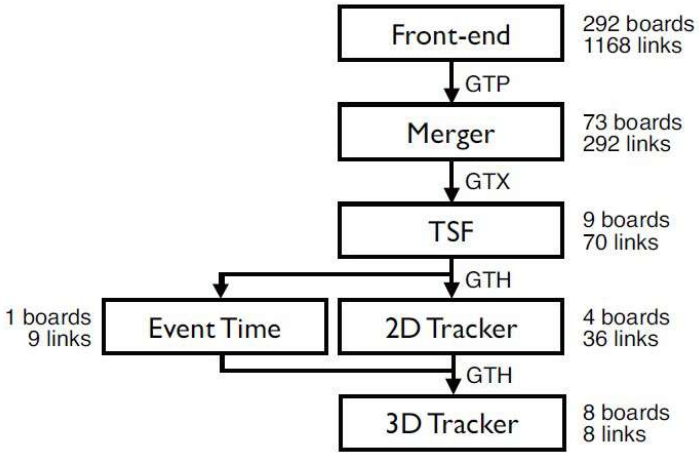

Figure 2.20: The overall configuration of the CDC trigger. GTP, GTY, and GTH are represent the protocols for the high-speed serial communication.

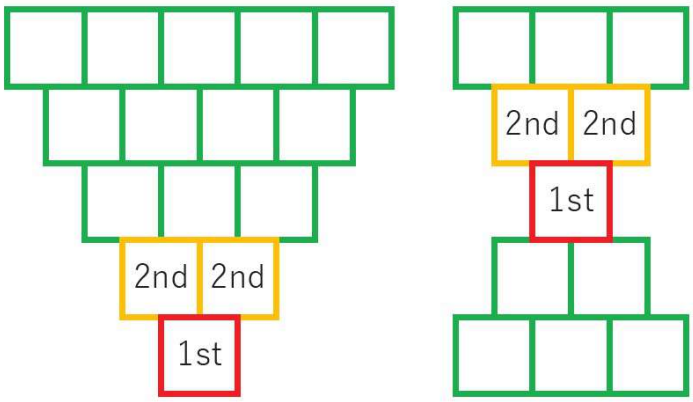

Figure 2.21: The structure of TSFs on the SL0 (left) and the other SLs (right). Each square represents a CDC cell. The red cell is the first priority cell and the two orange cells are the second priority cells.

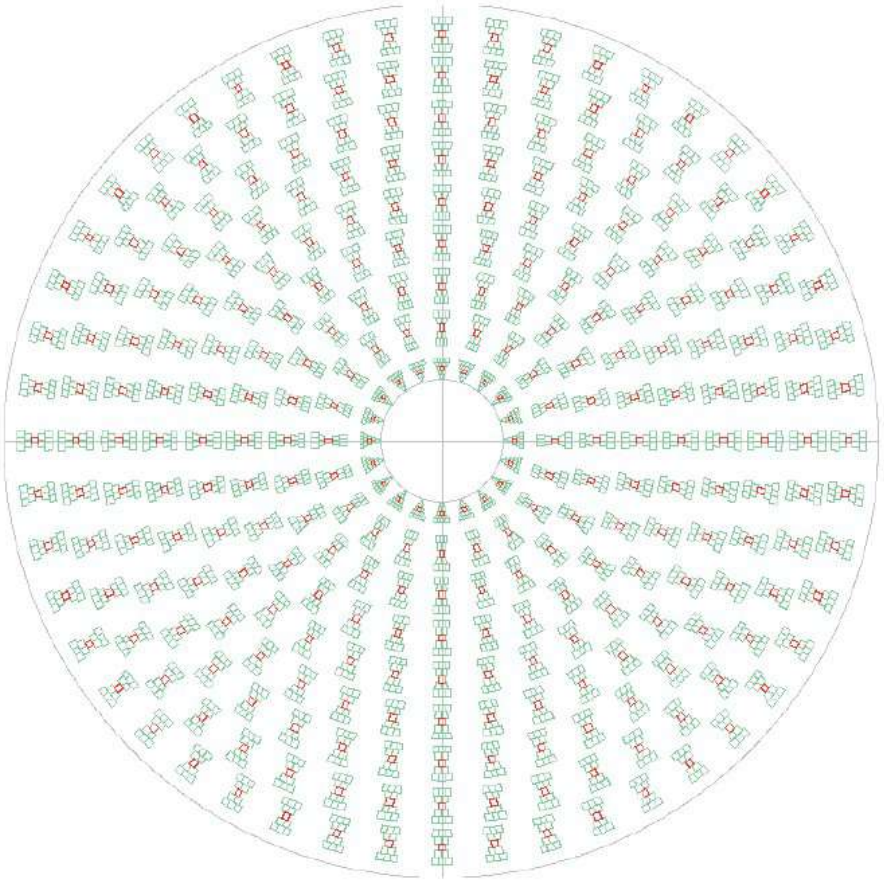

Figure 2.22: Cross-section of the CDC on the $x - y$ plane. Only 1/8 of all TSFs are shown.

2.7 Thin Fine-Pitch SVD (TFP-SVD)

As described below, we are now having several concerns in the operation of the current SVD coming from the harsh beam background. Furthermore, as discussed in Section 3.1, the Level-1 trigger rate is in a severe situation against the limit of 30 kHz. For these reason, the development plan of a new DSSD with thinner thickness and finer strip pitches compared with the current SVD is under discussion [20]. The new SVD is named "Thin Fine-Pitch SVD (TFP-SVD)". The TFP-SVD is intended as a replacement for the current SVD to improve the beam background tolerance, the reconstruction performance, and the Level-1 trigger performance. Moreover, a more ambitious target is to replace the inner part of the CDC layers with the TFP-SVD for higher beam background tolerance in that region.

Radiation damage Long-term irradiation to the silicon sensor causes radiation damage to the surface and bulk of the sensor, degrading its performance. The radiation damage can be evaluated by the total ionizing dose (TID) and the non-ionizing energy loss (NIEL). In the TID, incident particles ionize atoms in the sensor and change the surface states. The NIEL causes displacement of atoms in the sensor bulk region. The NIEL effect mainly leads to an increase in leakage current and a change in doping concentration. In particular, the latter causes a change in the full depletion voltage and requires higher power supply, making the operation of the silicon sensor more difficult. The expected radiation tolerance of the current SVD sensor is about 10 Mrad for the TID, and about 10^{13} neq/cm^2 for the NIEL where neq is a unit represented as an equivalent to NIEL of 1 MeV neutrons. The beam background rate at the design luminosity ($\mathcal{L} = 8.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$) is estimated by the simulation based on the beam background study in November 2020. The results, which are re-scaled using Data/MC ratios to compensate the gaps between simulation and data, are shown in Table 2.7. The detail of the simulation technique is described in Section 5.3. The safety factors derived as ratios of limits to expectations are also shown in the table. While the safety factor is above 1, the simulation can be optimistic because it assumes a perfect configuration of the collimators ignoring the beam injection efficiency, and it does not take the injection beam background into account. Therefore, a larger safety factor of about 5 is desirable by extending the limitation.

Table 2.7: Expectations and limits for the radiation damage of the SVD. Expectations are calculated by multiplying the expectation per single year [9] by the operating period of SuperKEKB.

	Expectation	Limit	Safety factor
TID	2.2 Mrad (10 years)	10 Mrad	4.5
NIEL	5.2×10^{12} neq/cm^2 (10 years)	10^{13} neq/cm^2	1.9

Reconstruction performance A vertex of a particle which decays in the SVD volume and leaves no hit signals in the PXD must be reconstructed using the SVD hit signals. An important example is K_S, which is essential for the indirect CP violation measurement, e.g. $B \to K_S\pi^0$, $B \to K_S K_S K_S$, and $B \to K_S\pi^0\gamma$. The vertex resolution for such decay modes is largely degraded by the multiple scattering in the material of the DSSD sensor. The effect of the multiple scattering is also critical for the low-momentum track reconstruction. The current

material budget per SVD layer corresponds to 0.7 % of the radiation length, however, smaller material budget is desirable.

Hit signals of background particles and those due to physics particles of interest are sometimes indistinguishable. Therefore, the large number of hit signals due to beam background events also degrades the reconstruction performance because of so many fake tracks. This effect is evaluated by the "hit occupancy", which is defined as the average fraction of the number of fired strips to the total number of strips. It is required that the hit occupancy of the innermost layer (layer 3) should be less than 5 % [21]. The expectation at the designed luminosity is shown in Table 2.8. The safety factor of 1.7 is obtained, which is not sufficient for the same reason described above.

Table 2.8: Expectations and limits for the hit occupancy of the SVD. The assumption of the simulation is the same as the Table 2.7.

	Expectation	Limit	Safety factor
Hit occupancy (layer 3)	about 3 %	5 %	1.7

Background tolerance on the CDC The influence of the beam background on the wire hit rate is biggest issue for the CDC. An increase in the wire hit rate changes electrical field around the wires due to the space charge effect and degrades the signal gain. The limit on the wire hit rate is roughly estimated to be about 200 kHz. The estimation of the wire hit rate at the target luminosity is done by the simulation based on the beam background study in May 2020. Fig. 2.23 shows the result of the CDC hit rates per sense wire of 56 layers. In the simulation, the 55th layer is masked due to malfunction. It is found that the average hit rates of the inner layers exceed the limitation of 200 kHz.

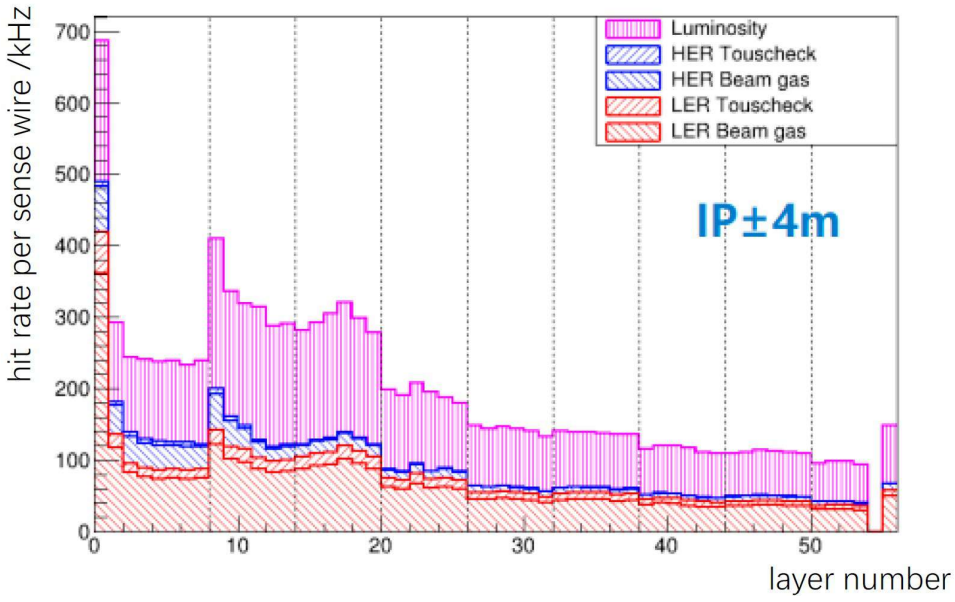

Figure 2.23: Expectation of the CDC hit rate [22]

2.7.1 Specification of the TFP-DSSD sensor

A new DSSD sensor, called "TFP-DSSD" sensor, is being developed to be used in the TFP-SVD. To obtain a safety factor of 5, the target beam background tolerances are set as

- Hit rate: $10\,\mathrm{MHz/cm^2}$
- TID: 11 Mrad (10 year)
- NIEL: $2.6 \times 10^{13}\,\mathrm{neq/cm^2}$

For these target, the TFP-DSSD plans to have the sensor thickness of about $140\,\mu$m and strip pitches of $100\,\mu$m or less. The thinner thickness compared to the current thickness of $300 - 320\,\mu$m has two benefits. One is the smaller material budget corresponding to 0.19 % of the radiation length, which will improve the K_S vertex reconstruction resolution and low-momentum track resolution. The other is the smaller change in full depletion voltage after radiation damages. The full depletion voltage V_FD is given by

$$V_\mathrm{FD} = \frac{d^2}{2\epsilon_\mathrm{Si}\rho\mu_e} \tag{2.6}$$

where d is the sensor thickness, ϵ_Si is the permittivity in silicon, ρ is the silicon resistivity, and μ_e is the electron mobility [23]. According to this equation, the full depletion voltage is proportional to the square of the sensor thickness. Fig. 2.24 shows the relation between the full depletion voltage and the NIEL damage in a silicon sensor with $300\,\mu$m thickness. Considering the target NIEL tolerance of $2.6 \times 10^{13}\,\mathrm{neq/cm^2}$, it needs power supply of about 150 V to fully deplete the sensor bulk. If other parameters are fixed, full depletion voltage of the TFP-DSSD is 37.5 V, which can be applied by a usual power supply.

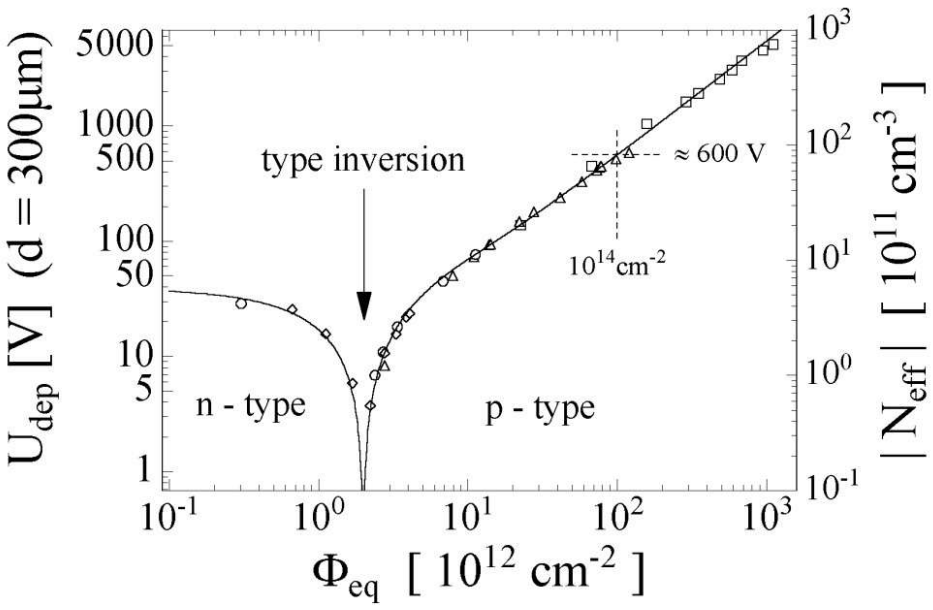

Figure 2.24: The observed change of the full depletion voltage as a function of the irradiated 1 MeV-neutron equivalence flux [24]

The first prototype of the TFP-DSSD sensor was fabricated by Micron Semiconductor in England and delivered to KEK by the end of May 2021. Its specification is summarized in Table 2.9. The thinner the sensor and the smaller the strip pitch, the smaller the charge induced in each strip. In order to concentrate the charge on each strip, all the floating strips were removed in the prototype. This prototype has the size of 52.6 mm × 59.0 mm, which is too small to cover the whole detector volume. Therefore, a lager TFP-DSSD sensor is under development. However, in the larger sensor, the strip length becomes longer and the detector capacitance becomes larger. This can cause the degradation of the signal-to-noise ratio (SNR). It may be critical especially for tracks with large incident angles, which have short pass lengths L (= strip-pitch/ $\sin\theta$ where θ is the incident angle). To assure enough SNR, larger strip pitch is being considered in the next prototype.

Table 2.9: Specification of the first prototype of the TFP-DSSD sensor

	Value
Size	52.6 mm × 59.0 mm
Active area	51.2 mm × 57.6 mm
Thickness	140 μm
Number of P-strips	1024
Number of N-strips	768
Pitch b/w P-strips	50 μm
Pitch b/w N-strips	75 μm
Floating strip	No
Full depletion voltage	< 15 V

2.7.2 Front-end readout electronics: SNAP128

New front-end readout electronics for the TFP-DSSD is also under development to meet the requirements for the TFP-SVD. It is named "SNAP128". SNAP128, developed in 180 nm CMOS technology, has 128 input channels and digitizes the analog signals internally. The development is being done by the electrical system group in KEK, based on the SliT128 readout ASIC for KEK g-2 experiment [25].

The internal structure of one channel is shown in Fig. 2.25. The diagram consists of the analog part and the digital part. In the analog part, similarly to APV25, an input analog signal is amplified and shaped at the CSA (Charge Sensitive Amplifier) and the CR-RC shaper. In the comparator, the shaper output is compared with a threshold voltage and converted into binary data. The threshold is given by the external input voltage and internal 8-bit DAC (Digital-to-Analog Converter). The comparator has two selectable polarities so that the chip can read out the signal from either side of the sensor. In the example shown in Fig. 2.26, the comparator outputs logic-high when the negative signal is below the threshold. The comparator outputs are sampled at the frequency of 127 MHz and stored in the ring buffer. Each clock that reads out samples is named "frame". The depth of the ring buffer is 2048, therefore, the maximum trigger latency is about 16 μs ($\approx 2048 \times 1/127$ MHz). For the suppression of the hit occupancy and hit rate, the hit time information with the resolution of 7.87 ns ($\approx 1/127$ MHz) is enough to distinguish the physics particle hits and the beam background hits.

When the Level-1 trigger signal arrives, the samples at the requested address in the ring

buffer of all the 128 channels are read out and recorded in a 128-channel × 1024-depth FIFO. After that, the samples of the 128 channels are serialized and output via the line of D_FPGA_D (Fig. 2.25). Fig. 2.27 shows the structure of the binary output data. In the output data, the header bits (3 start bits, 1 bit error flag, and 10 bits for readout address) are followed by the hit information bits in order of frame.

The first prototype SNAP128 named "SNAP128A" was produced by SilTerra in Malaysia and delivered to KEK in April 2021. Its performance was evaluated in detail and the results will be fed back into the next design [12].

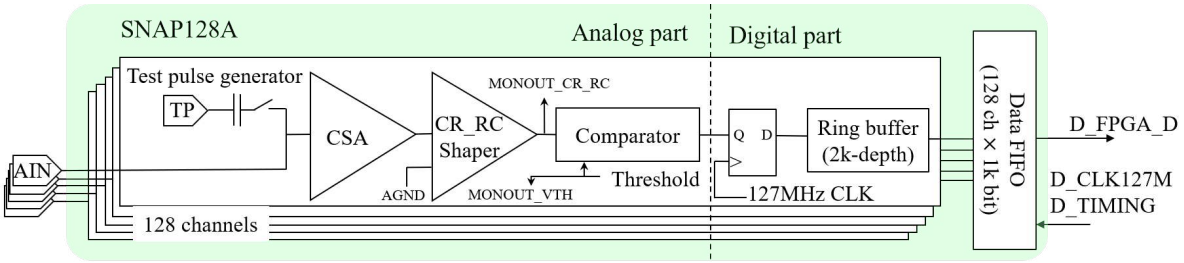

Figure 2.25: Block diagram of one channel in the SNAP128

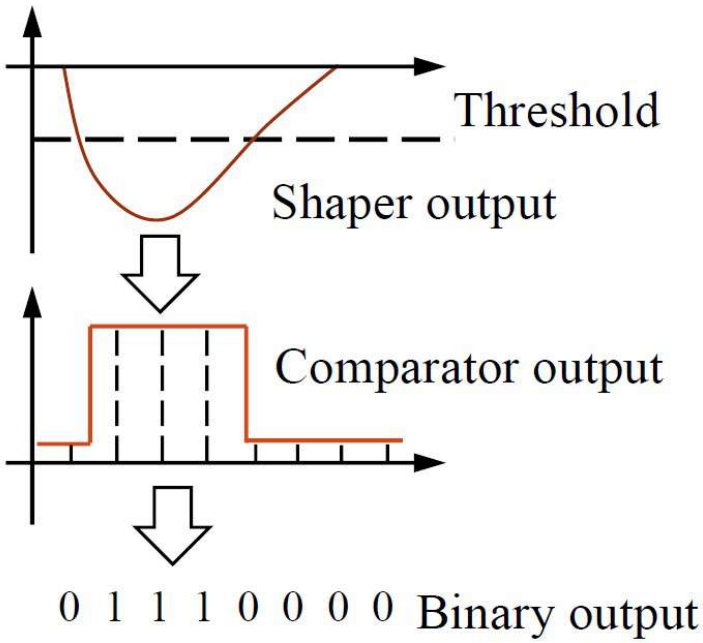

Figure 2.26: Schematic for binary output [12]. In this example, the comparator is set to negative polarity and output 1 when the shaper output is below the comparator threshold.

Delimiter 3'b110	Error flag (1 bit)	Ring buffer address (10 bit)	Hit data (frame 0) ch. 127~ch.0 (128 bit)	Hit data (frame 1) ch. 127~ch.0 (128 bit)	.....

Figure 2.27: Structure of the binary output from SNAP128 [12]

2.7.3 Self trigger signal output of SNAP128

The TFP-SVD is planed to participate in the Level-1 trigger system as a sub-trigger in order to suppress the trigger rate under future harsh background environment. It is described in more detail in Chapter 3. For use in the sub-trigger system, SNAP128 is also designed to output a signal, which is the logic OR of the hit signals from several channels, in a different path from the D_FPGA_D (Fig. 2.25) without waiting for the arrival of the Level-1 trigger signal. The more detailed block diagram of the digital part of SNAP128 is shown in Fig. 2.28. In this figure, SNAP_SMPs read out the digitized data from the comparator and write them into the ring buffer. For the sub-trigger system, the hit signals are extracted from the SNAP_SMPs of all the 128 channels. The lower limit (SELFTRG_LOWER) and upper limit (SELFTRG_UPPER) can be set for the duration of the logic-high of the hit signals. Furthermore, a waiting time (SELFTFG_TIME) can also be set. When at least one channel has a signal with duration between the lower and upper limits, the output from the D_SELFTRG becomes logic-high for one frame after the waiting time. The clock of the D_SELFTRG is synchronized with the sampling rate of the SNAP_SMP of 127 MHz.

The filtering process of the output signals using the duration is called "Duration Cut" in this thesis. An example of the Duration Cut is shown in Fig. 2.29. In simulation, the duration of logic-high of the background signal tends to be longer than that of the physics signal. Therefore, it is expected to roughly select the physics signals by the Duration Cut. The optimization of the lower and upper limits, and the waiting time is a next task, however, the contribution of the latency generated by Duration Cut to the trigger latency should be taken into account.

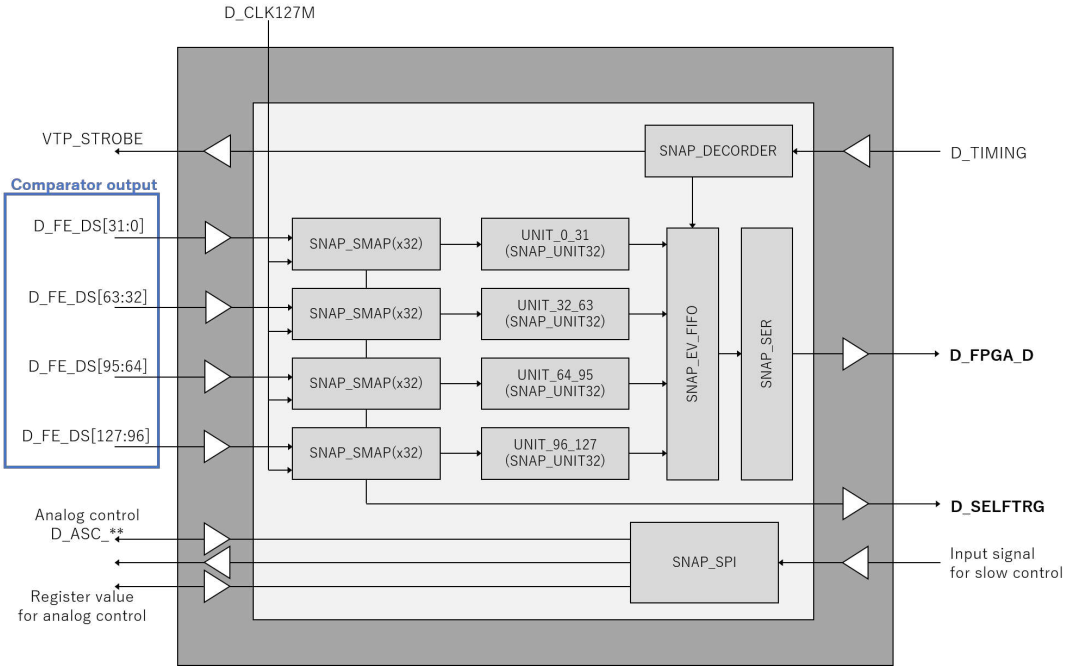

Figure 2.28: Block diagram of the digital part in SNAP128.

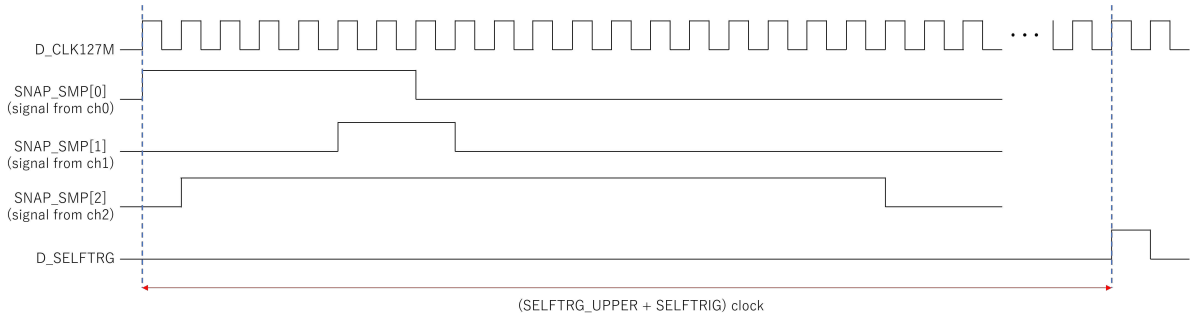

Figure 2.29: Output timing of D_SELFTRG. In this example, the SELFTRG_LOWER is set to be 5 and the SELFTRG_UPEER is set to be 10. Since the duration of the logic-high of the channel 0 is 7, the D_SELFTRG becomes logic-high for one clock after waiting the clocks of the SELFTRG_UPPER and SELFTRIG_TIME from the rise of the channel 0.

Chapter 3

TFP-SVD sub-trigger

The Level-1 trigger is required to suppress its maximum average rate less than 30 kHz. However, at the current luminosity of $4.7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in June 2022, which is 1/10 of the target luminosity of $6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the current trigger rate has reached about 8 kHz. Therefore, the future trigger rate is expected to exceed the limit. The trigger rate projection based on the current situation is discussed in Section 3.1. The main contributor to the background rate is also described in the section. To suppress the background rate and meet the upper limit of the trigger rate, we develop the trigger algorithm using the TFP-SVD detector. Section 3.2 explains the basic strategy of the TFP-SVD trigger, then Section 3.3 determines the requirements for its performance.

3.1 Projection of the Level-1 trigger rate at the target luminosity

The Level-1 trigger system has several trigger conditions called "trigger bit"s for various physics purposes. Table 3.1 shows the trigger conditions of "$B\bar{B}$ CDCTRG", which is the CDC trigger bit for $B\bar{B}$ events, "$B\bar{B}$ ECLTRG", which is the ECL trigger bit for $B\bar{B}$ events, and "Low-multi CDCTRG", which is the CDC trigger bit for low-multiplicity events. More than 99 % of the $B\bar{B}$ events are triggered by the $B\bar{B}$ CDCTRG and $B\bar{B}$ ECLTRG [26]. There are several other trigger bits besides these three trigger bits in the current Level-1 trigger, however, it is expected to be difficult to maintain all the trigger bits at the target luminosity. Considering the purpose of the Belle II experiment, it is important to maintain the trigger bits of the $B\bar{B}$ CDCTRG and $B\bar{B}$ ECLTRG. In addition to this, the Low-multi CDCTRG should be also maintained for the τ and dark sector physics.

Based on the current trigger rate, the future trigger rate is projected by scaling with the luminosity. The current trigger rates and projected trigger rates are shown in Table 3.2. The "Total CDCTRG" bit is the integrated trigger bit of the $B\bar{B}$ CDCTRG and Low-multi CDCTRG. The sum of the rates of multiple trigger bits overestimates the integrated trigger rate because the multiple trigger bits can satisfy their trigger conditions for the same event. Hence, in order to calculate the Total CDCTRG rate, the "exclusive rate" is introduced. In the calculation of the exclusive rates, trigger bits are prioritized and the raw rates are distributed to them according to their priority to avoid double-counting. In the calculation of the Total CDCTRG rate, the $B\bar{B}$ CDCTRG is prioritized over the Low-multi CDCTRG, and the trigger of the Low-multi CDCTRG is ignored if the $B\bar{B}$ CDCTRG issues its trigger for the same event.

Since the CDC and ECL triggers also correlate somewhat each other, their rate cannot be

Table 3.1: Trigger conditions of each trigger bit. All trigger bits reject the injection beam background. The Bhabha event is identified as an event that meets the conditions showed in the bottom row, and the Bhabha veto rejects the Bhabha events.

Trigger bit	Trigger condition
$B\bar{B}$ CDCTRG	{CDC 2D track ≥ 3 AND CDC 3D track ≥ 1} OR {CDC 2D track ≥ 2 AND CDC 3D track ≥ 1 AND Angle between CDC tracks $\geq 90^\circ$ AND Bhabha veto}
$B\bar{B}$ ECLTRG	{ECL cluster ≥ 3 AND Bhabha veto at the end-cap} OR {ECL energy $\geq 1\,\mathrm{GeV}$ AND Bhabha veto}
Low-multi CDCTRG	CDC 3D track ≥ 1 AND Momentum $\geq 0.7\,\mathrm{GeV}/c$ AND Bhabha veto
Bhabha event	$\left\{165^\circ < \sum \theta_{\mathrm{CM}} < 190^\circ\right\}$ AND $\left\{160^\circ < \Delta\phi_{\mathrm{CM}} < 200^\circ\right\}$ AND $\left\{E^0_{\mathrm{CM}} > 3\,\mathrm{GeV}\right\}$ AND $\left\{E^1_{\mathrm{CM}} > 3\,\mathrm{GeV}\right\}$ AND $\left\{E^0_{\mathrm{CM}} > 4.5\,\mathrm{GeV}\ \mathrm{OR}\ E^1_{\mathrm{CM}} > 4.5\,\mathrm{GeV}\right\}$ where $\sum \theta_{\mathrm{CM}}$ is the sum of the polar angles of two ECL clusters, $\Delta\phi_{\mathrm{CM}}$ is the difference of the azimuthal angles of two ECL clusters, and E^0_{CM} and E^1_{CM} are the energies of the ECL clusters in the center-of-mass system.

simply summed. The CDC trigger accounts for the highest trigger rate, therefore, this thesis focuses on the reduction of the CDC background trigger rate. Therefore, instead of considering the limit of 30 kHz for the total trigger bits, we consider the individual upper limit of 20 kHz for the Total CDCTRG by trisecting the total limit and distributing them to those three trigger bits ($B\bar{B}$ CDCTRG, Low-multi CDCTRG, and $B\bar{B}$ ECLTRG). In the Table 3.2, it can be seen that the future rate of the Total CDCTRG is above the upper limit of 20 kHz.

Table 3.2: Projected rates of each trigger bit. The current raw rate and current luminosity are as of June 18, 2022. In the calculation of the exclusive rates, the priorities are set as $B\bar{B}$ CDCTRG > Low-multi CDCTRG. The Total CDCTRG and $B\bar{B}$ ECLTRG are above their upper limits of 20 kHz and 10 kHz, respectively.

Trigger bit	Current raw rate	Current exclusive rate	Future exclusive rate
Luminosity $[\mathrm{cm}^{-2}\mathrm{s}^{-1}]$	4×10^{34}	4×10^{34}	6×10^{35}
$B\bar{B}$ CDCTRG	1.9 kHz	1.9 kHz	28.7 kHz
Low-multi CDCTRG	2.6 kHz	1.7 kHz	25.3 kHz
Total CDCTRG	–	3.6 kHz	54.0 kHz
$B\bar{B}$ ECLTRG	1.1 kHz	1.1 kHz	17.1 kHz

As a breakdown of each trigger rate, the ratio of physics rate and background rate is assumed to be the ratio of events selected and not selected by the HLT. Based on the data in June 2022, the physics rates and background rates for each trigger bit are calculated. The results are shown in Table 3.3. To meet upper limit while maintaining the physics trigger rate,

the Total CDCTRG must reduce its background rate by about 83 %.

Table 3.3: Breakdown of the future exclusive rates of each trigger bit at $\mathcal{L} = 6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

Trigger bit	Total rate [kHz]	Physics rate [kHz]	Background rate [kHz]
$B\bar{B}$ CDCTRG	28.7	7.0(24 %)	21.7(76 %)
Low-multi CDCTRG	25.3	5.7(23 %)	19.6(78 %)
Total CDCTRG	54.0	12.7(24 %)	41.3(76 %)
$B\bar{B}$ ECL	17.1	9.6(56 %)	7.5(44 %)

As discussed in Section 2.4.2, one of the main contributor to the background rate is considered to be Off-IP particles. They are expected to be rejected by selecting the production z-positions of the particles. The current condition of the CDC trigger to select the particle production position is $|z| < 15\,\mathrm{cm}$ to assure enough trigger efficiency for the physics events of interest. Figure 3.1 shows the relation between the production z-positions of the particles in the 3D track trigger reconstruction and in the offline reconstruction. It can be seen that many production positions determined to have large $|z|$ in the offline reconstruction are determined to be close to the origin in the CDC trigger. Thus, Off-IP particles with $|z| > 15\,\mathrm{cm}$ are expected to remain even after the selection by the CDC trigger.

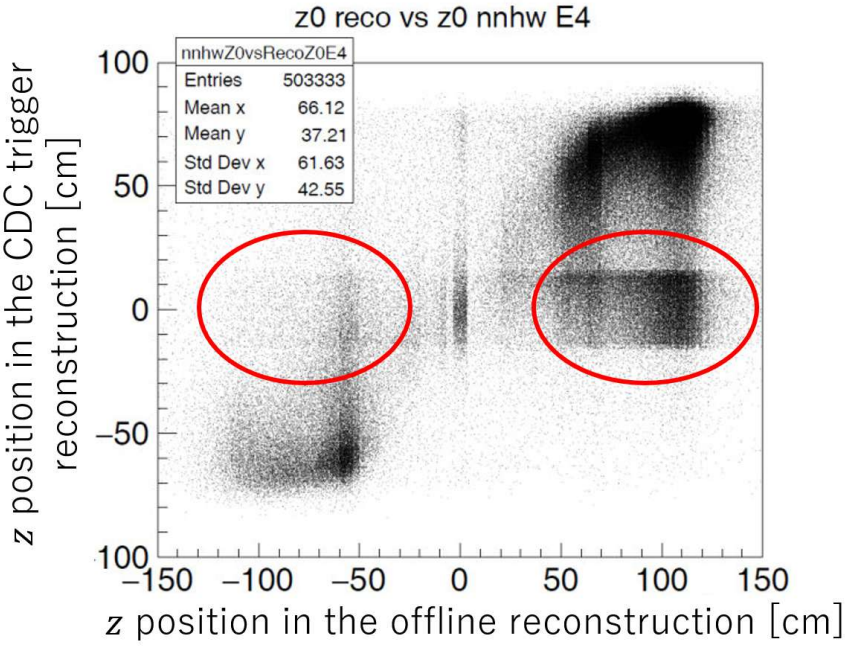

Figure 3.1: Relation between z production positions in 3D track trigger reconstruction and those in the offline reconstruction [27]. In this study, the data in March 2021 was used. The plots indicated by the red circle are the particles, which are determined to be Off-IP particles in the offline reconstruction and to be particles near the IP in the CDC trigger.

The beam background and electrical noise in the readout electronics increase the hit occupancy due to the background noise hits. Even if there is no On-IP particle, the noise hits

can accidentally satisfy the trigger condition of the CDC trigger bit, resulting in fake triggers. Another main contributor to the background rate is considered to be the fake triggers.

3.2 Basic strategy of the TFP-SVD trigger

The TFP-SVD trigger is a track trigger which selects only tracks from the IP. It reconstructs particle trajectories using the hit signals from the D_SELFTRG of the SNAP128 chips. While the concrete design of the TFP-SVD is not determined yet, the performance evaluation of the new trigger system using simulation software and development of the trigger algorithm require to assume some reasonable detector configuration. Thus, the geometry of the TFP-SVD for the studies is developed based on the current SVD geometry as described in Section 3.2.1. The TFP-SVD trigger is planned to be used with the CDC trigger to help it to reject beam background particles which cannot be rejected by the CDC trigger alone.

3.2.1 Assumptions on the TFP-SVD detector design for the studies in this thesis

TFP-DSSD sensor

All the current sensors (small rectangular, large rectangular, and trapezoidal) are replaced with the TFP-DSSD sensors. The size of the sensor active area is assumed to be the same as the current DSSD sensor shown in Table 2.2. The number of P-strips and the pitch between them are also assumed to be the same as the current sensor. The pitch of N-strips is changed to 80 μm, just by dividing the N-strip pitch of the current DSSD sensor by two for the layer-3 sensors and by three for the layer-4, 5, and 6 sensors. Therefore, one TFP-DSSD sensor has two or three times larger number of N-strips than the current DSSD sensor. No floating strips are placed and all the strips are read out by SNAP128. The assumption on the TFP-DSSD sensor geometry is summarized in Table 3.4. The target of the TFP-SVD sensor geometry has the thickness of 140 μm and the strip pitches of 75 μm for P-strips and 85 μm for N-strips. The assumed sensor thickness and strip pitches in Table 3.4 are almost consistent with the target value, and the realistic performance can be evaluated using the assumption.

Table 3.4: Assumption on the TFP-DSSD sensor geometry for the studies in this thesis

	Current DSSD	TFP-DSSD
Thickness	300 – 320 μm	140 μm
Number of P-strips	768	768
Number of N-strips	512 – 768	1536
Pitch b/w P-strips	50 – 75 μm	50 – 75 μm
Pitch b/w N-strips	160 – 240 μm	80 μm
Floating strip	Yes	No

The sensor locations are assumed to be the same as the locations of the current SVD sensors. Thus, the assumed geometry of the TFP-SVD consists of four cylindrical layers located at 39 mm, 80 mm, 104 mm, and 135 mm from the z-axis, respectively. There are 7 ladders in layer 3, 10 ladders in layer 4, 12 ladders in layer 5, and 16 ladders in layer 6. Fig. 3.2 shows the TFP-SVD geometry formed by strips of the TFP-DSSD sensors. In the TFP-SVD, IDs are assigned to each ladder and each sensor as shown in Fig. 3.3.

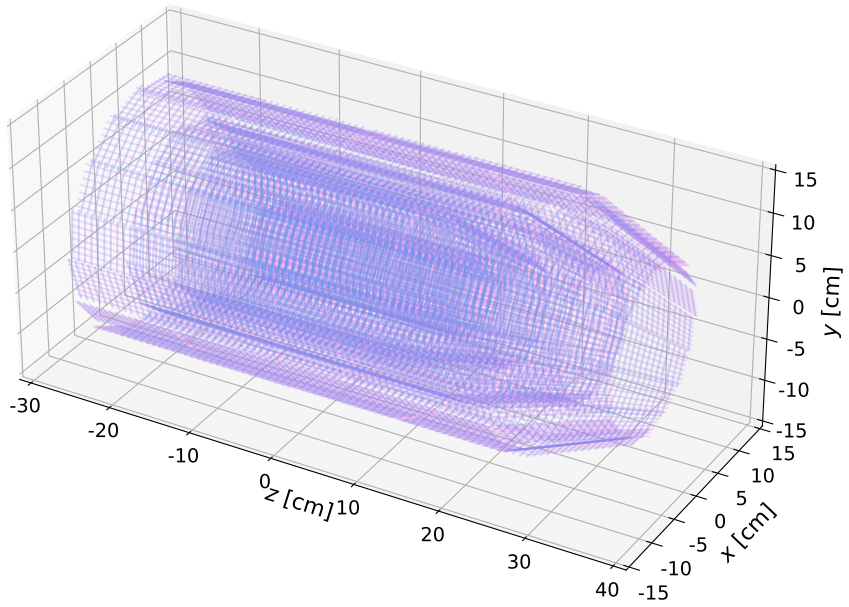

Figure 3.2: Geometry of the TFP-SVD formed by strips of the TFP-DSSD sensors. The blue(red) line segments represent the N(P)-strips.

SNAP128

For the TFP-SVD trigger, the binary output from the D_SELFTRG at 127 MHz is used. Since the tracking performance deteriorates if the hit occupancy exceeds $\mathcal{O}(1\,\%)$, it is desirable to aim for an hit occupancy of $\mathcal{O}(0.1\,\%)$ or less [9]. It is known that if the SNR (signal-to-noise ratio) is set to more than 4, the hit occupancy due to the electrical noise becomes less than $\mathcal{O}(0.1\,\%)$ [28]. Hence, the threshold of SNR > 4 is applied to the comparator in SNAP128, which is the digitization processing described in Section 2.7.2.

The output signal from the D_SELFTRG of SNAP128 is the logic OR of the hit signals in multiple strips. The set of the multiple strips is named "cell" in this thesis. The cell of P-strips is called P-cell, and that of N-strips is called N-cell. If the number of OR'ed strips contained in each cell is n, the cell is called n-cell. In this study, two types of n-cells are examined: 128-cell and 64-cell. When at least one strip of the cell is fired, the cell is also fired, however, it cannot determine which strip is fired. Therefore, the position resolution depends on the width of the cell. Considering the strip pitches (50–80 μm), the cell width is about 0.6 – 1.0 cm for 128-cell and 0.3 – 0.5 cm for 64-cell. The schematic of the cell is described in Fig. 3.4, and the 3-dimensional graphic images of the 128-P-cell and 128-N-cell are displayed in Fig. 3.5.

In the overall geometry, the TFP-SVD has 132,096 P-strips and 264,192 N-strips. Therefore, in the case of 128-cell, it has 1032 ($= 132,096/128$) P-cells and 2064 ($= 264,192/128$) N-cells.

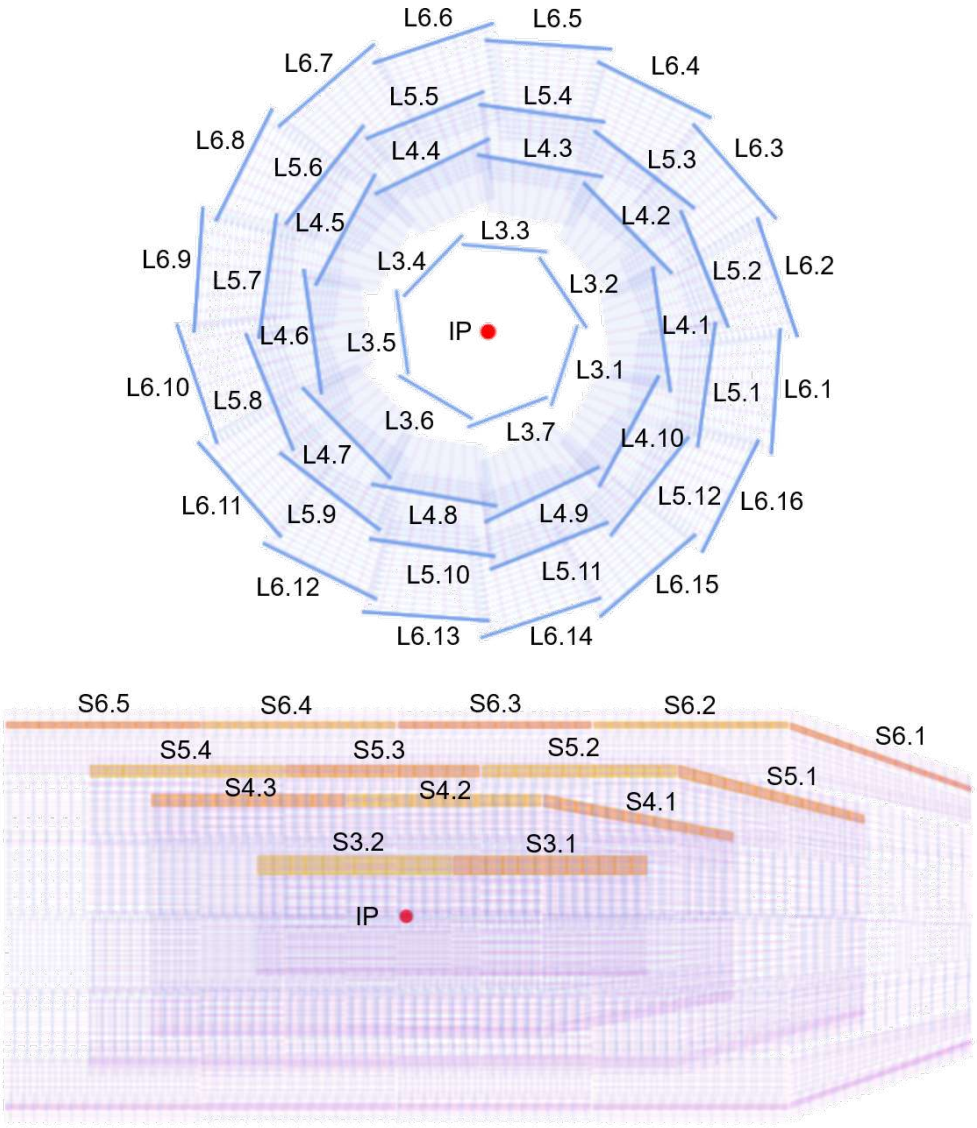

Figure 3.3: TFP-SVD geometry projected on the $x-y$ plane (top) and the $z-x$ plane (bottom)

Similarly, in the case of 64-cells, it has 2064 P-cells and 4128 N-cells. The assumptions on SNAP128 and the cells are shown in Table 3.5.

3.2.2 Matching with the CDC sub-trigger

In order to help the CDC trigger to find On-IP particles correctly, the TFP-SVD trigger tries to find On-IP particles at the same event. These sub-trigger results are sent to the GRL (Global Reconstruction Logic) to take the track matching. If either one sub-trigger cannot find any On-IP particles, the GRL assumes that there is no On-IP particle in the event and the GDL (Global Decision Logic) does not issue the Level-1 trigger signal for that event. By taking the logic AND of the CDC and TFP-SVD trigger results in this way, the background CDC

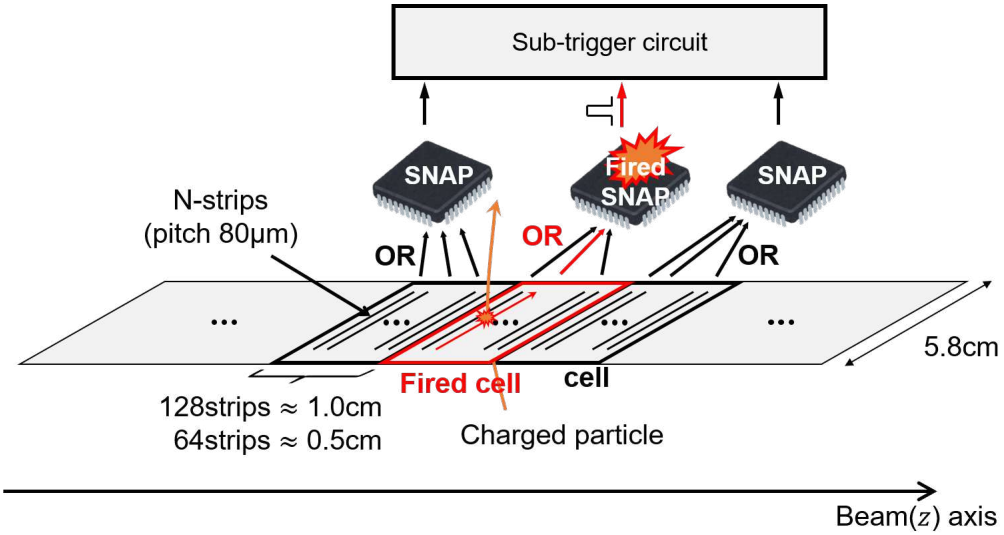

Figure 3.4: Schematic of the cell concept in the case of the N-side of the sensor

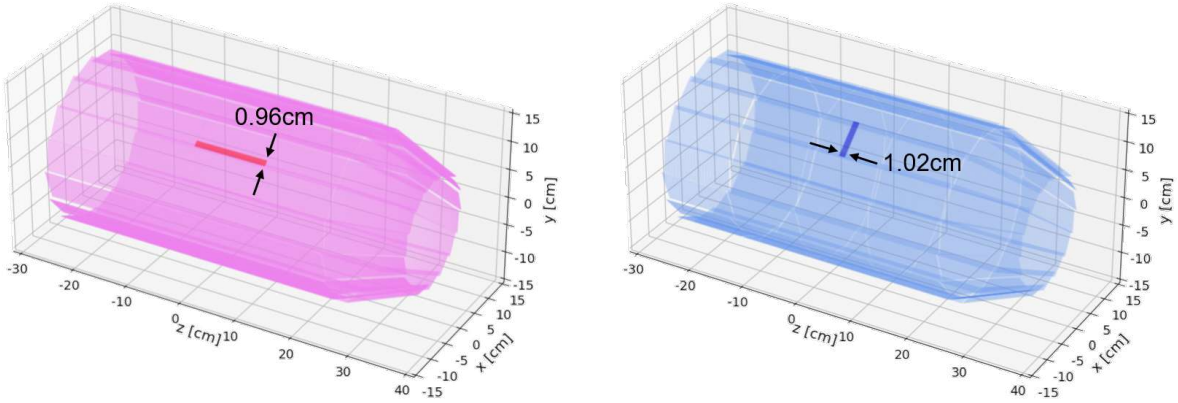

Figure 3.5: Graphical images of the 128-cells. The left(Right) shows a P(N)-cell in sensor S6.3 of ladder L6.7.

sub-triggers can be suppressed.

SNAP128 outputs hit signals at the frequency of 127 MHz. At every frame of the clock frequency (7.87 ns), the TFP-SVD trigger provides the trigger decision results. On the other hand, due to the large variation of the electron drift time in the CDC, the time resolution of the CDC trigger is larger than that of the TFP-SVD trigger. Fig. 3.6 shows the time distribution of the issued CDC trigger at the Bhabha event data. In this plots, the time origin is set to collision time measured by the TOP that has very precise time resolution (TOP T0). The RMS and 3-sigma interval of the time distribution is about 10 ns and 60 ns, respectively. Thus, the CDC trigger signal can be expected to come within 60 ns with a high confidence level. In that time window, the TFP-SVD makes about 8 trigger decisions. In order to find the same

Table 3.5: Assumption on SNAP128 and the cells

	128-cell	64-cell
Output rate	127 MHz	127 MHz
Zero suppression	SNR > 4	SNR > 4
Number of strips to be taken OR	128	64
Number of P-cells	1032	2064
Number of N-cells	2064	4128
Width of P-cell	0.64 – 0.96 cm	0.32 – 0.48 cm
Width of N-cell	1.02 cm	0.51 cm

particle in both detectors, the logic OR of the trigger results in 8 frames of the TFP-SVD trigger must be used. A schematic of the trigger matching structure is shown in Fig. 3.7.

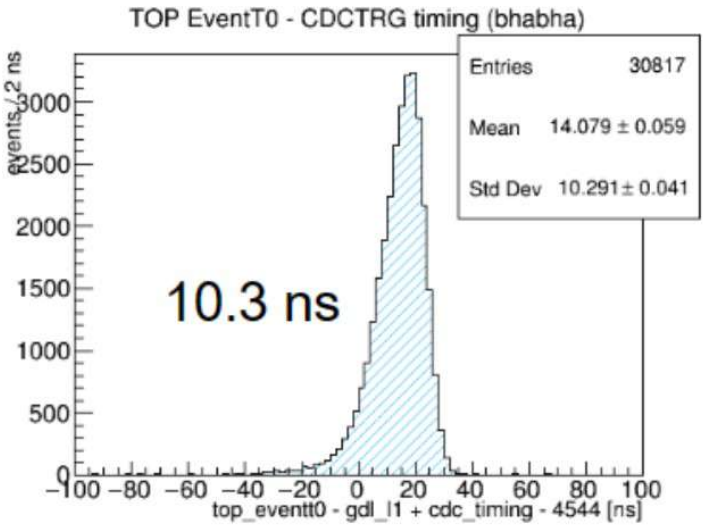

Figure 3.6: Time distribution of the CDC trigger [29]. RMS of the distribution is 10.3 ns. The time origin is set to collision time measured by the TOP.

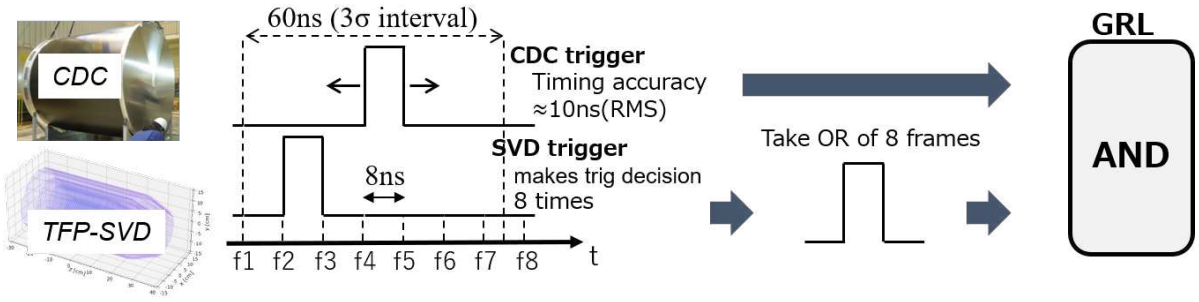

Figure 3.7: Schematic of matching the CDC trigger and TFP-SVD trigger by taking the logic AND of them

3.3 Requirements for TFP-SVD trigger

The performance of the TFP-SVD trigger is characterized by the three criteria: the trigger efficiency, discrimination power for On-IP particles, and fake trigger probability.

Trigger efficiency The TFP-SVD trigger should issue sub-trigger if the event involves the On-IP particles. The trigger efficiency is defined as the probability of finding the events with the On-IP particles:

$$\text{Trigger efficiency} = \frac{\#\text{ triggered events involving the On-IP particles}}{\#\text{ events involving the On-IP particles}} \tag{3.1}$$

where # events means the number of events. The current trigger efficiency of $B\bar{B}$ CDCTRG is about 95 %. To require the same efficiency level as the CDC trigger bit, the target trigger efficiency of the TFP-SVD trigger is set to be 95 % or more.

Discrimination power for On-IP particles On the other hand, in order to discriminate the Off-IP particles, the finding probability of the events with the Off-IP particles should be decreased to zero. The z position range where the trigger probability is above 1 % is defined as a "particle selection area", which represents the z position resolution of the TFP-SVD trigger. As mentioned in Section 3.1, the current CDC trigger requires $|z| < 15\,\text{cm}$ for the particle production position. To improve the resolution, the target of the particle selection area of the TFP-SVD trigger is set to be $|z| < 5\,\text{cm}$, which is 1/3 of the CDC trigger condition.

Fake trigger probability In the TFP-SVD trigger, the effect of the fake trigger, in which the fired cells due to the noise hits can accidentally satisfy the trigger condition of the TFP-SVD trigger, is also important. The fake trigger probability is defined as

$$\text{Fake trigger probability} = \frac{\#\text{ triggered events in which only background particles are produced}}{\#\text{ events in which only background particles are produced}}. \tag{3.2}$$

As long as beam background exists, the TFP-SVD trigger always issues a fake trigger with this probability per frame. Assuming that the TFP-SVD and CDC triggers due to the background noise are independent, the CDC background trigger rate is reduced to the

percentage of the fake trigger probability. As explained above, the logic OR of the TFP-SVD triggers in any continuous 8 frames is used to take the matching with the CDC trigger. In order to reduce the CDC background trigger rate by a factor of 10, our target on the fake trigger probability is set to be less than 10 % for the time window of the 8 frames. In this case, the background trigger rate is reduced by 90 % and, as shown in Table 3.6, the CDC trigger rate can meet the upper limit of 20 kHz.

Table 3.6: Projected exclusive rates of the CDC trigger bits at the target luminosity of $\mathcal{L} = 6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ when taking the matching with the TFP-SVD trigger. The rates when taking the matching are calculated by adding the physics rates to background rates reduced to the target fake trigger probability of 10 %.

Trigger bit		No matching [kHz]	Matching [kHz]
$B\bar{B}$ CDCTRG	Physics rate	7.0	7.0
	Background rate	21.7	2.2
	Total rate	28.7	9.2
Low-multi CDCTRG	Physics rate	5.7	5.7
	Background rate	19.6	2.0
	Total rate	25.3	7.7
Total CDCTRG		54.0	16.8

Our target values on each evaluation index are summarized in Table 3.7.

Table 3.7: Targets on each evaluation index

Index	Target
Trigger efficiency	$> 95\,\%$
Particle selection area	$\lvert z\rvert < 5\,\mathrm{cm}$
Fake trigger probability (8 frames)	$< 10\,\%$

Chapter 4

Development of TFP-SVD trigger algorithm

When a particle passes through the TFP-DSSD sensor, cells(strips) on which the particle passes are fired. Thus, the particle trajectory can be represented by a combination of the fired cells(strips) in the four layers (layer 3 to layer 6), which is called a "cell(strip) pattern". On-IP particles have different cell patterns from Off-IP particles. Ignoring the track bending due to the magnetic field, in the case of On-IP particles, the fired cells in the four layers and the IP should be connected with a straight line. In practical, because of the magnetic field, they are connected with a curved line. On the other hand, it is not necessarily for the case of Off-IP particles. All the possible cell patterns created by On-IP particles are collected by simulation, and they are listed up in a table, called a "cell pattern table". By comparing fired cells with the cell pattern table, it is determined if the pattern of the fired cells is caused by the On-IP track or not, then the decision is sent to the GRL. In this thesis, hit signals and fired strips(cells) under the actual accelerator operation are called "online" hit signals and "online" strips(cells) to distinguish them from the hit signals or strips(cells) obtained in the simulation process to generate the cell pattern tables or test samples (Chapter 5).

The main purpose of the TFP-SVD trigger is to identify the z position of the particle production. The z positions of the particle hits can be obtained by the N-cells. However, if only the N-cells are used, many fake tracks may be reconstructed by hits scattered randomly in the ϕ direction. The P-cells, which provide the ϕ positions of the particle hits, can reduce the possibility of the reconstruction of fake tracks. Therefore, we can consider two different trigger algorithms: the "N-algorithm", which uses only the N-cells, and the "PN-algorithm" which uses both the P-cells and N-cells. The number of cell patterns using only N-cells is less than that using both P-cells and N-cells. Therefore, compared to the PN-algorithm, the N-algorithm is expected to save resources when implemented as firmware due to the smaller size of the cell pattern table. At the same time, we can also consider more two different algorithms using 128-cells or 64-cells. Eventually, there are four possible trigger algorithms as shown in Table 4.1. In this thesis, we study three of the four trigger algorithms except for the N-64 algorithm.

Table 4.1: Possible trigger algorithms. In this thesis, the N-64 algorithm is skipped.

	Only N-cells	Both P-cells and N-cells
128-cells	N-128 algorithm	PN-128 algorithm
64-cells	(N-64 algorithm)	PN-64 algorithm

The purpose of this chapter is to elaborate each trigger algorithm. Section 4.1 describes how to generate the cell pattern tables. The trigger algorithms using their cell pattern tables are explained in Section 4.2. When comparing online hit signals with the cell pattern table, the timing discrepancies in online hit signals of different layers should be considered. Section 4.3 shows the operation to compensate the timing discrepancies.

4.1 Generation of the cell pattern tables

The way to represent the particle trajectory using cells depends on the trigger algorithm. This section describes how to generate the cell pattern table. In order to generate the pattern table, the Monte Carlo (MC) simulation is performed on the basf2 (Belle II Analysis Software Framework) software [30]. In this study, the simulation to collect On-IP particle cell patterns is performed in the following three steps for each event. First, a particle gun generates one charged particle at the IP. Second, Geant4 [31] simulates the behavior of the particle under the magnetic field and the interaction between the particle and the TFP-DSSD sensor. Third, the detector response is emulated from energy depositions in the sensitive sensor volume and hit signals of each strips are generated as a binary data. The array of the strip hits are converted to the array of the cell hits by taking the logic OR to the strip hits in the 128-cell groups or 64-cell groups.

In order to collect all the possible cell patterns of On-IP particle tracks, a large enough number of events are simulated. For the N-128 and PN-128 algorithms, one million events are simulated. Changing from the 128-cells to 64-cells, the number of cell patterns increases by a factor of 10. Hence, for the PN-64 algorithm, twenty million events are simulated. In each event, the parameters of momentum and its direction (θ and ϕ) are randomly determined from uniform distributions within given ranges. The parameters are shown in Table 4.2.

Table 4.2: Parameters of the particle gun for creating the pattern tables. In each event, momentum, polar angle, and azimuthal angle are extracted from uniform distributions within the given ranges.

Parameters	Value
Particle	$\mu^{\pm}$
Production point x	$x = 0\,\mathrm{cm}$
Production point y	$y = 0\,\mathrm{cm}$
Production point z	$z = 0\,\mathrm{cm}$
Range of momentum p	$0.2\,\mathrm{GeV}/c \leq p \leq 3.0\,\mathrm{GeV}/c$
Range of polar angle θ	$0^\circ \leq \theta < 180^\circ$
Range of azimuthal angle ϕ	$0^\circ \leq \phi < 360^\circ$
Number of events	(128-cell) 1,000,000 (64-cell) 20,000,000

After the MC simulation, the following operations extracting the hit patterns are performed on the hit data to construct the cell pattern table.

Extraction of one-way track After flying out the TFP-SVD detector volume, low-momentum tracks with small radius circular trajectories can go into the detector volume again. The re-

turned track also creates the fired cells. However, they are not necessary for the pattern table. In this thesis, the hits created at time $t \leq T/2$ where T is the period of circular motion are called "hits on the way path", while the hits at time $t > T/2$ are called "hits on the way back path". The MC simulation provides T and each hit time (t). Using those information, only hits on the way path are extracted (Fig. 4.1).

Extraction of cell patterns from hit cluster In 95 % events, one particle leaves hits in continuous multiple strips on one side of the sensor. The group of the continuous hits is called a cluster. The cluster shape can change even if the particles are generated with the exactly same kinematics due to the variation of the electrical noise in the readout electronics. In order to cover the possible pattern of the hit cluster, the cell patterns are reconstructed by repeatedly extracting one hit from each layer as shown in Fig. 4.1. Therefore, multiple cell patterns are obtained from one hit cluster, each of which is a subset of the original hit cluster.

Deduplication Since each cell has a width of about 0.3 – 1.0 cm, some particle tracks are converted into the same cell pattern. Thus, the duplicate patterns are deleted. In this step, the initial 1,000,000 or 20,000,000 patterns are significantly reduced. The eventual numbers of patterns are described in Section 4.2.

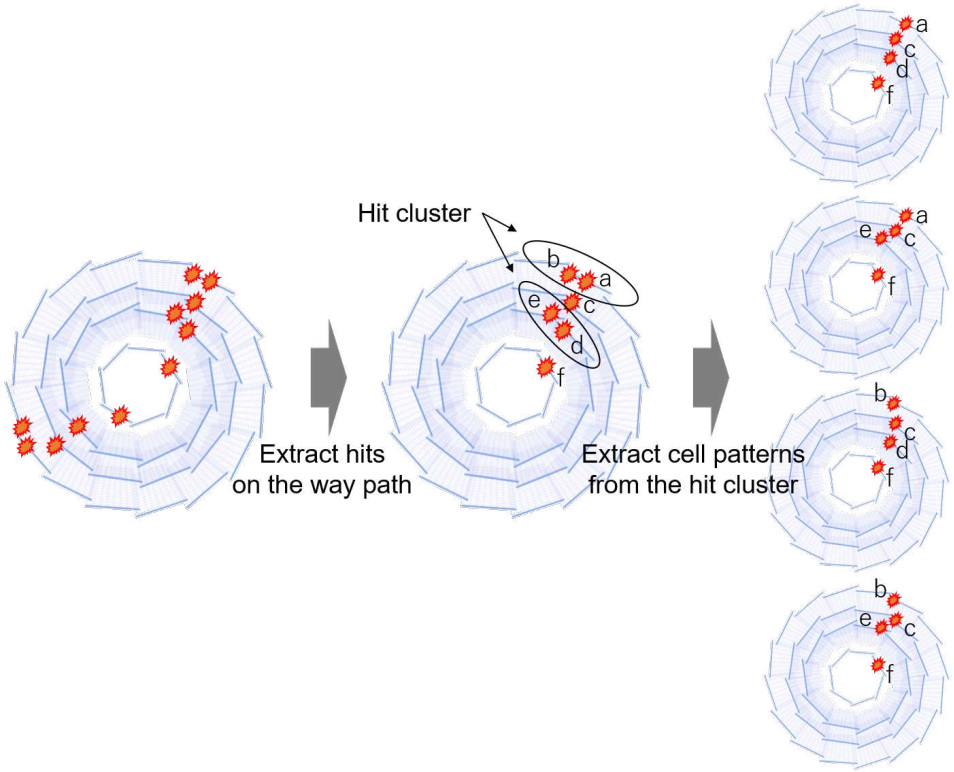

Figure 4.1: Operations of the extraction of hits on the way path and extraction of cell patterns from hit cluster

4.2 Trigger algorithm

Trigger algorithms are developed in the software at first to evaluate the performance using the MC simulation. This section describes details of the trigger algorithms and explains how the algorithms are implemented in software.

4.2.1 N-128 algorithm

The N-128 algorithm introduces a new concept of N-ring-cell, which is a set of N-cells having the same z-coordinate aligned on the circumference of each layer. The graphical image is shown in Fig. 4.2. Layer 3, 4, 5, and 6 have 24, 36, 48, and 60 ring-cells respectively, and there are 168 ring-cells in total. These ring-cells have unique IDs ranging from 0 to 167. In this algorithm, each item in the cell pattern table is represented by a combination of these ring-cell IDs. Since a single particle basically makes one hit cell on the N-side of the sensor in each layer while flying from layer 3 to layer 6, its track can be basically represented by a combination of four ring-cell IDs as shown in Fig. 4.3.

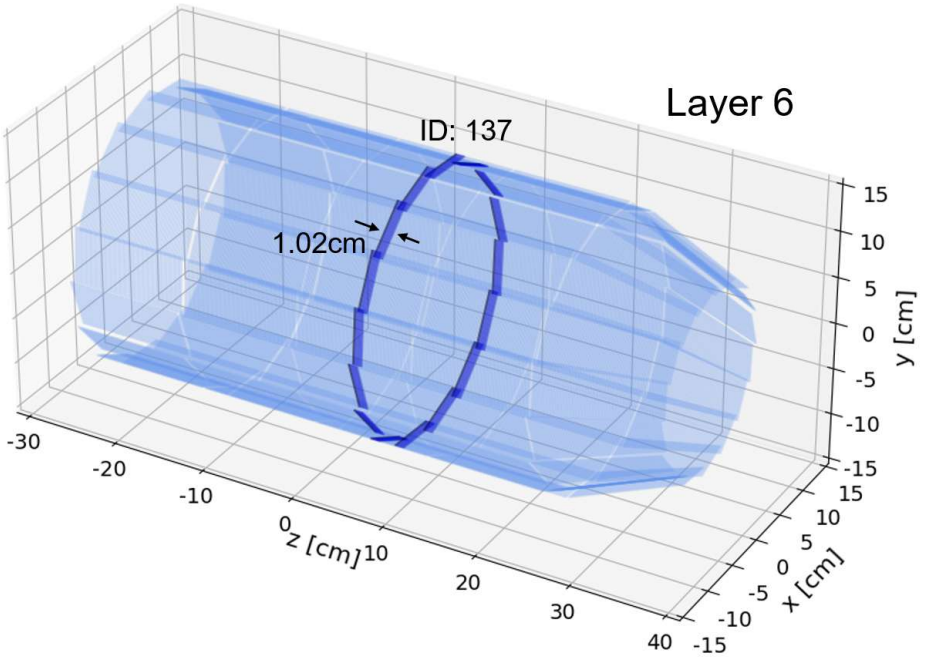

Figure 4.2: Graphical image of an N-ring-cell. As an example, the ring-cell with ID 137 on layer 6 is displayed.

When executing the algorithm in software, a combination of N-ring-cells is encoded into a bit string of 168-width: the ring-cell with ID 0 corresponds to the beginning of the bit string, the ring-cell with ID 1 corresponds to the second bit of the bit string, and so on. Initially, all bits are set to '0', then, when the ring-cell with ID n is fired, the n-th bit changes to '1'. Therefore, each particle track is typically represented by a bit string of 168-width with four '1' bits corresponding to layer 3, 4, 5, and 6 (Fig. 4.3).

The concern about using only the N-ring-cells is they have no ϕ information at all. In the representation using only the N-ring-cells, many fired cell patterns due to beam background or

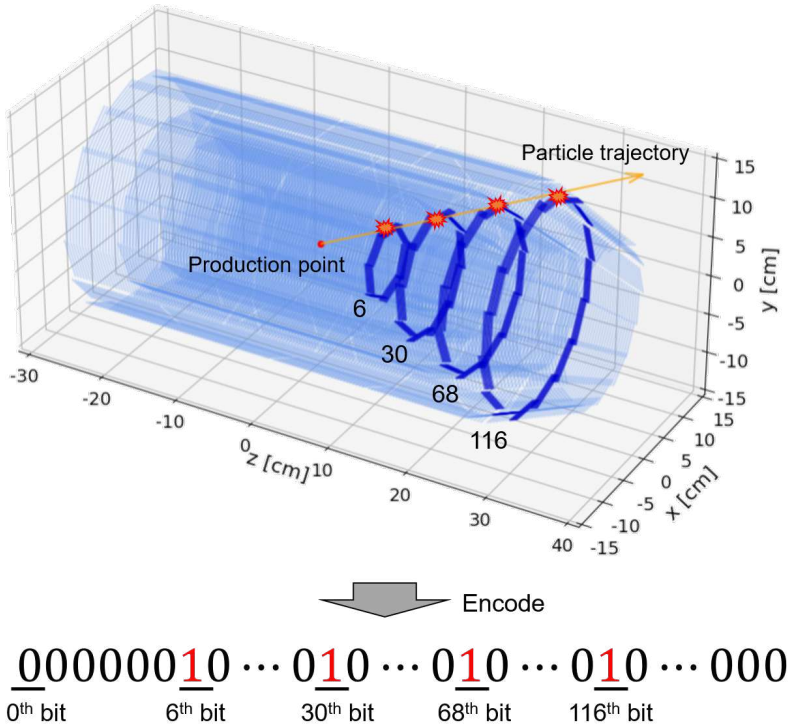

Figure 4.3: An example of fired ring-cells due to a particle passing through sensors. The combination of four fired ring-cells are encoded into a bit string of 168-width.

electrical noise can be indistinguishable from On-IP particle cell patterns. It leads a high fake trigger rate. The 2D track and 3D track of the CDC sub-trigger contain the information of the trajectory direction in ϕ. To suppress the fake trigger at the matching of the TFP-SVD and CDC triggers, the TFP-SVD trigger can also send the track ϕ information and the matching of the two triggers can be taken only if the ϕ of the tracks are consistent. For this purpose, the cell patterns are grouped by the layer-6 ladder containing the fired cell in each pattern. Each group of the patterns is considered as a small cell pattern table, resulting in 16 small cell pattern tables in total (16 is the number of the layer-6 ladders). When collecting the On-IP particle track pattern in Section 4.1, the IDs of the inner ladders (layer-3, 4, and 5 ladders) passed through by particles are also collected and compiled as the "inner ladder list" for each ladder of layer 6. Fig. 4.4 shows the case of making the cell pattern table of ladder L6.1. In this example, particles which are generated at the IP and reach ladder L6.1 possibly pass through the inner ladders of L3.1, L3.2, L4.1, L4.10, L5.1, L5.2, and L5.12. Thus, the inner ladder list for ladder L6.1 holds those ladder IDs. Each of these ladders in the inner ladder list is classified as "in-section" ladder, otherwise, the ladder is classified as "out-section" ladder. Before comparing the online hits with the cell pattern table, the hits of the out-section ladders are truncated and only hits of the in-section ladders are converted into a bit string (Fig. 4.5). After that, the comparison between online hits and the cell pattern table is executed. The same procedure is repeated for each ladder from L6.1 to L6.16 while reclassifying the inner ladders as in-section or out-section.

In this trigger algorithm, each of the 16 cell pattern tables contains approximately 500 patterns. Since each cell pattern is represented by a bit string of 168-width, the size of each table is roughly 10 kB (≈ 168 bits $\times$ 500). It is a small enough data size to be implemented in the FPGA used in Chapter 7.

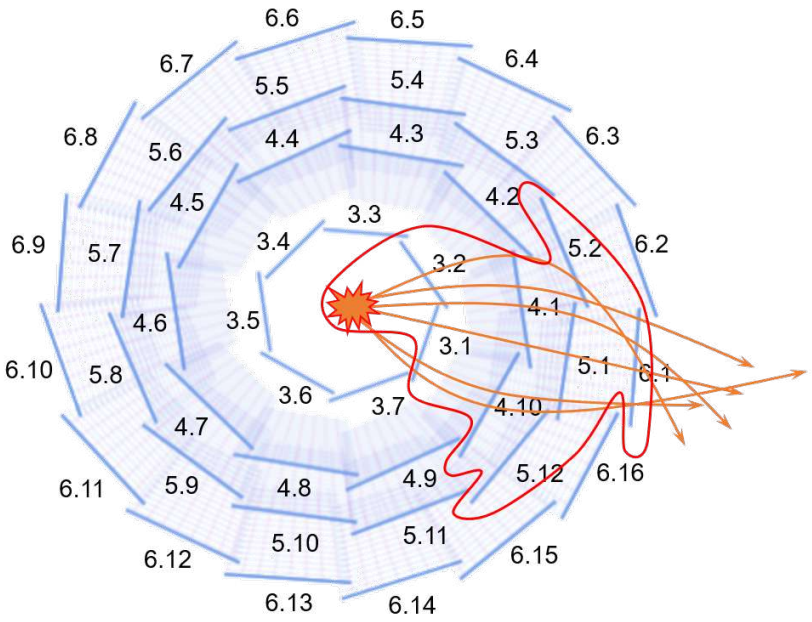

Figure 4.4: Track patterns that can reach the ladder L6.1 in the MC simulation

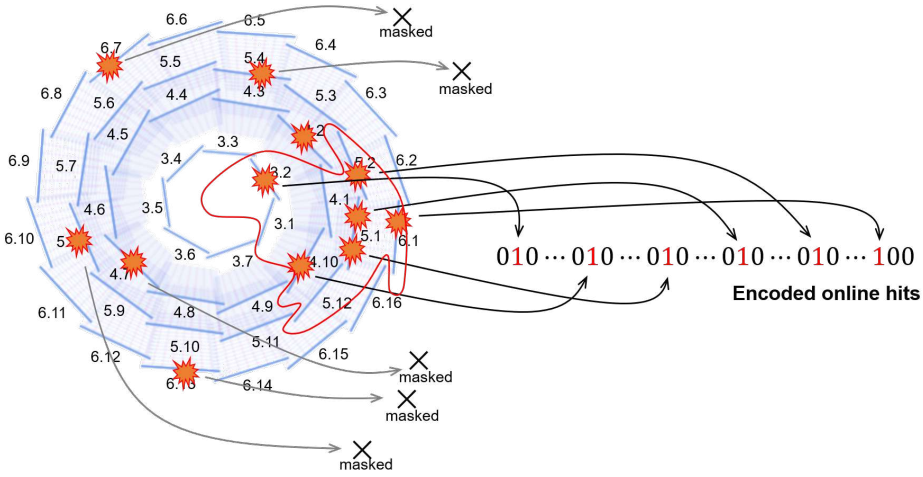

Figure 4.5: Masking the online hits of the out-section ladders in the case of ladder L6.1

Trigger condition

In practical, apart from the hit cells created by the On-IP particles, there are also hit cells randomly due to the beam background and electrical noise. To deal with the additional random hits, the comparison between the online hit pattern and each pattern in the cell pattern table is to be made only on the bits where the pattern in the table has a fired cell '1'. An example is shown in Fig. 4.6.

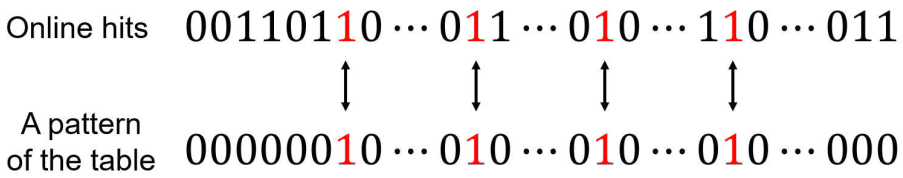

Figure 4.6: Comparison between online hits and a pattern of the table. In this example, the trigger condition is met because the bit string of online hit pattern has four '1's in the same place as the pattern in the table.

This comparison is performed as follows in software so that even if there are several extra '1's in online hit bit string, they are ignored. It is called "trigger condition".

$$\begin{aligned} &\text{if } (\text{bits}^{\text{online}} \text{ AND } \text{bits}_j^{\text{table}}) == \text{bits}_j^{\text{table}} \text{ then} \\ &\qquad \text{sub-trigger } = 1 \\ &\text{else} \\ &\qquad \text{sub-trigger } = 0 \end{aligned} \tag{4.1}$$

where $\text{bits}^{\text{online}}$ is the bit string of online hits and $\text{bits}_j^{\text{table}}$ is the bit string of j-th pattern of the cell pattern table. By taking the logic AND of the online hits and the table before performing the equivalence operation (==), we can ignore the '1's except for the positions in which the pattern of the table has '1's.

In the algorithm, comparison between online hits and the pattern tables starts with ladder L6.1 after masking the hits of out-section ladder for ladder L6.1. If trigger condition is met for at least one pattern of the table, the sub-trigger signal is set to '1' and the trigger algorithm is stopped, otherwise, it moves to comparison in ladder L6.2 after re-truncating the online hits. If no patterns of the table met the trigger condition in the loop, the event is considered to have no On-IP particles and the sub-trigger signal is set to '0'. The flowchart of this algorithm is described in Fig. 4.7.

Relaxed trigger condition

Fig. 4.8 shows the TFP-SVD geometry projected onto the $z - x$ plane. In this figure, sensors placed perpendicularly to the $z - x$ plane ($x > 0$) are colored alternately yellow and orange. The blue circles indicate the sensor insensitive areas at the edges of the sensors. If a particle passes through these insensitive areas, no hit signals are recorded. The relation between the sensor hit efficiency, which is defined as follows, and θ is shown in Fig. 4.9.

$$\text{Sensor hit efficiency} = \frac{\#\text{ events where there is at least one hit on the layer}}{\#\text{ total events}} \tag{4.2}$$

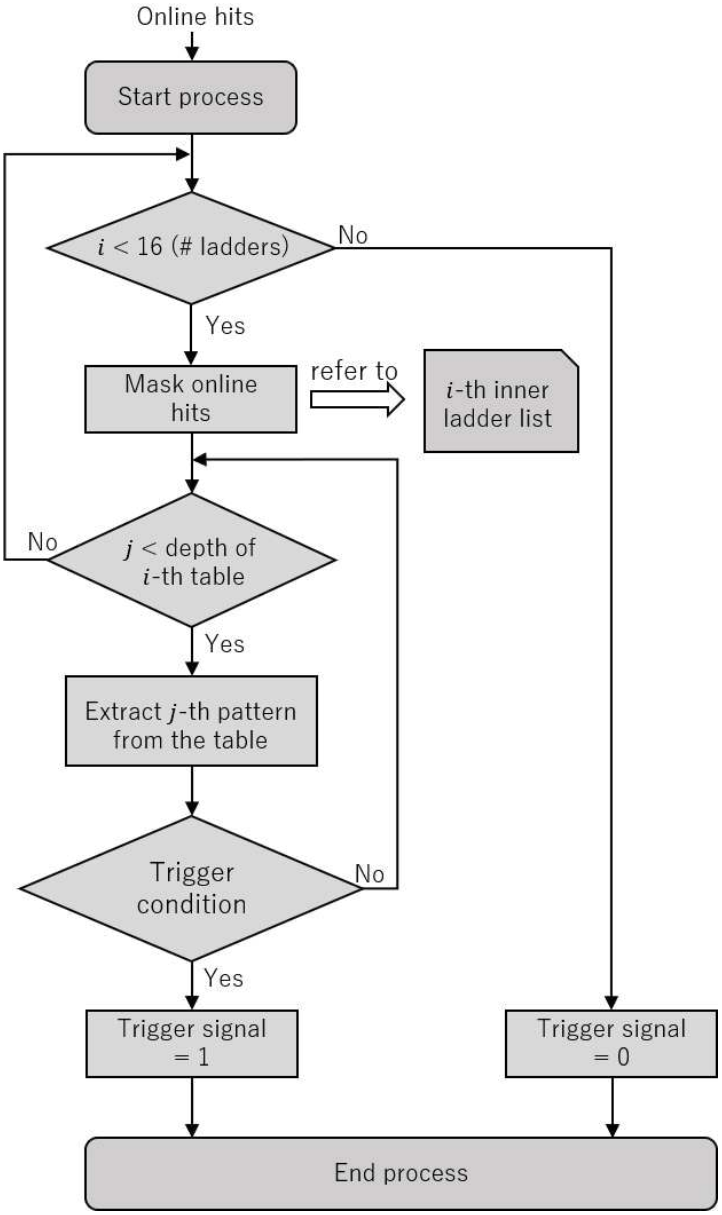

Figure 4.7: Flowchart of the N-128 trigger algorithm

In fact, we can see that hit efficiency drops significantly in the θ regions where the sensor insensitive area is located. The θ regions where insensitive area exists are listed in Table 4.3.

The above trigger condition requires perfect matching using all the four layers. Thus, if online hits of all four layers cannot be obtained, the trigger condition cannot be met, resulting in a low trigger efficiency. For this reason, we consider other two trigger conditions: "3/4-allθ matching" and "3/4-selectedθ matching". Hereafter, the above trigger condition is named "Full matching".

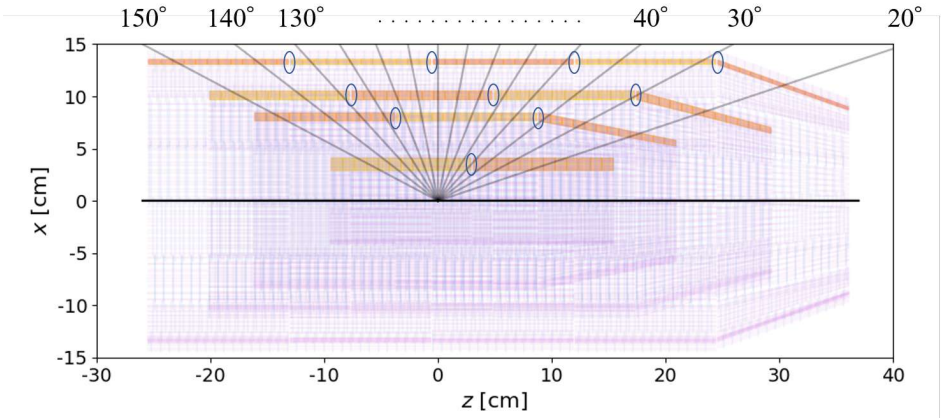

Figure 4.8: TFP-SVD geometry projected onto the $z - x$ plane. Sensor insensitive areas are marked with blue circles.

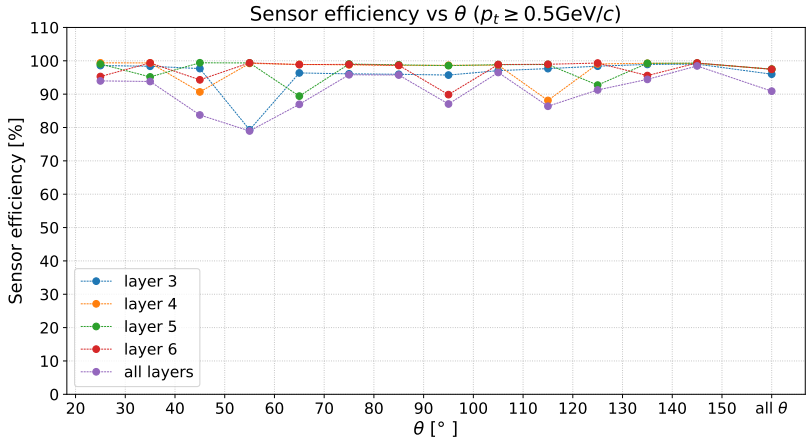

Figure 4.9: Relation between sensor hit efficiency and polar angle θ

3/4-allθ matching Aiming for a high trigger efficiency, the 3/4-allθ matching condition requires matching between online hits and the pattern table using any three out of the four layers. In the comparison using hits of only the layer 4, 5, and 6, online hits and the table can be matched even if the layer 3 has no hits. In this trigger condition, the comparisons without

Table 4.3: Regions of θ where the sensor insensitive areas exist

	Regions of θ
Layer 3	$50^\circ \leq \theta < 60^\circ$
Layer 4	$40^\circ \leq \theta < 50^\circ$, $110^\circ \leq \theta < 120^\circ$
Layer 5	$30^\circ \leq \theta < 40^\circ$, $60^\circ \leq \theta < 70^\circ$, $120^\circ \leq \theta < 130^\circ$
Layer 6	$20^\circ \leq \theta < 30^\circ$, $40^\circ \leq \theta < 50^\circ$, $90^\circ \leq \theta < 100^\circ$, $130^\circ \leq \theta < 140^\circ$

the layer 3, 4, 5, or 6 are performed independently. If the trigger condition is met in the at least one comparison, the sub-trigger is issued. The trigger condition of the 3/4-allθ matching is represented by

$$
\begin{aligned}
\text{if } & \left\{ (\ \text{bits\_wo3}^{\text{online}} \ \text{ AND } \ \text{bits\_wo3}_j^{\text{table}}\ ) \ == \ \text{bits\_wo3}_j^{\text{table}} \right\} \\
& \text{OR } \left\{ (\ \text{bits\_wo4}^{\text{online}} \ \text{ AND } \ \text{bits\_wo4}_j^{\text{table}}\ ) \ == \ \text{bits\_wo4}_j^{\text{table}} \right\} \\
& \text{OR } \left\{ (\ \text{bits\_wo5}^{\text{online}} \ \text{ AND } \ \text{bits\_wo5}_j^{\text{table}}\ ) \ == \ \text{bits\_wo5}_j^{\text{table}} \right\} \\
& \text{OR } \left\{ (\ \text{bits\_wo6}^{\text{online}} \ \text{ AND } \ \text{bits\_wo6}_j^{\text{table}}\ ) \ == \ \text{bits\_wo6}_j^{\text{table}} \right\} \ \text{ then} \\
& \quad \text{sub-trigger } = \ 1 \\
& \text{else} \\
& \quad \text{sub-trigger } = \ 0
\end{aligned}
\tag{4.3}
$$

where bits_wo$n$ is the bit string except of the layer n ($n = 3, 4, 5, 6$).

3/4-selectedθ matching While the 3/4-allθ matching condition is expected to increase the trigger efficiency, it is also expected to increase the fake trigger probability with its relaxed condition. Another strategy is to limit the θ regions to which the matching condition using three layers is applied. From Fig. 4.9, we can select the θ regions where the sensor hit efficiency is lower than 90 % as shown in Table 4.4. The θ regions listed in this table is named "low-efficiency θ region". We can estimate the particle ejection angle θ by the position of the fired cells of layer 6 or 5. In the 3/4-selectedθ matching condition, the matching condition using three layers except for the corresponding layer is applied if the particle ejection angle θ is in the low-efficiency θ region, otherwise, the Eq. (4.1) is applied. The trigger condition of the 3/4-selectedθ matching is represented as follows.

$$
\begin{aligned}
& \text{if } \ \theta \in \text{Low-efficiency } \theta \text{ region of layer } n \ \text{ then} \\
& \quad \text{if } \ (\ \text{bits\_won}^{\text{online}} \ \text{ AND } \ \text{bits\_won}_j^{\text{table}}\ ) \ == \ \text{bits\_won}_j^{\text{table}} \ \text{ then} \\
& \qquad \text{sub-trigger } = \ 1 \\
& \quad \text{else} \\
& \qquad \text{sub-trigger } = \ 0 \\
& \text{else} \\
& \quad \text{Full matching condition Eq. (4.1)}
\end{aligned}
\tag{4.4}
$$

4.2.2 PN-128 and PN-64 algorithms

The PN-128 and PN-64 algorithms use both the P-cells and N-cells. The number of cells in each layer is shown in Table 4.5. These 128(64)-cells are assigned unique IDs from 0 to 3096(6192). Since a single particle basically makes one hit on each side of the sensor of each layer while flying from layer 3 to layer 6, its track can be basically represented by a combination of eight cell IDs: four N-cell IDs and four P-cell IDs. Fig. 4.10 shows the case of the PN-128 algorithm.

Table 4.4: Low-efficiency θ region. In these regions, the sensor hit efficiency is lower than 90 %. In this table, θ regions are chosen at 5° intervals

	Regions of θ
Layer 3	$50^\circ \leq \theta < 55^\circ$
Layer 4	$40^\circ \leq \theta < 45^\circ$, $110^\circ \leq \theta < 120^\circ$
Layer 5	$65^\circ \leq \theta < 70^\circ$, $125^\circ \leq \theta < 130^\circ$
Layer 6	$45^\circ \leq \theta < 50^\circ$, $90^\circ \leq \theta < 95^\circ$

As with the N-128 algorithm, the combination of the P-cells and N-cells is encoded into a bit string of 3096(6192)-width in the case of the PN-128(64) algorithm (Fig. 4.10).

In the case of the PN-128 and PN-64 algorithms, all track patterns for all ladders of layer 6 are included in one table because there is no need to distinguish ladders to obtain the ϕ information. After the processing for generating the cell pattern tables, described in Section 4.1, 88,553 patterns remain for the PN-128 algorithm and 793,764 patterns remain for the PN-64 algorithm. For the PN-128 algorithm, since each pattern is represented by a bit string of 3096-width, the table size is about 33 MB ($\approx 3096\,\text{bits} \times 88,553$). For the PN-64 algorithm, since each pattern is represented by a bit string of 6192-width, the table size is about 586 MB. These sizes are much larger than that of the N-128 algorithm. Their feasibility of the implementation as firmware are discussed in Chapter 7.

Table 4.5: Number of cells in each layer

	128-cell	64-cell
Layer 3 P-cell	84	168
Layer 3 N-cell	168	336
Layer 4 P-cell	180	360
Layer 4 N-cell	360	720
Layer 5 P-cell	288	576
Layer 5 N-cell	576	1152
Layer 6 P-cell	480	960
Layer 6 N-cell	960	1920
Total	3096	6192

As with the N-128 algorithm, the trigger conditions of the Full matching, 3/4-allθ matching, and 3/4-selectedθ matching are applied by these two algorithms. The flowchart of these algorithms is represented in Fig. 4.11. The difference between N-algorithm and PN-algorithm in the flowchart is that the PN-algorithm has all patterns in one table, therefore, there is no loop for the ladder in layer 6.

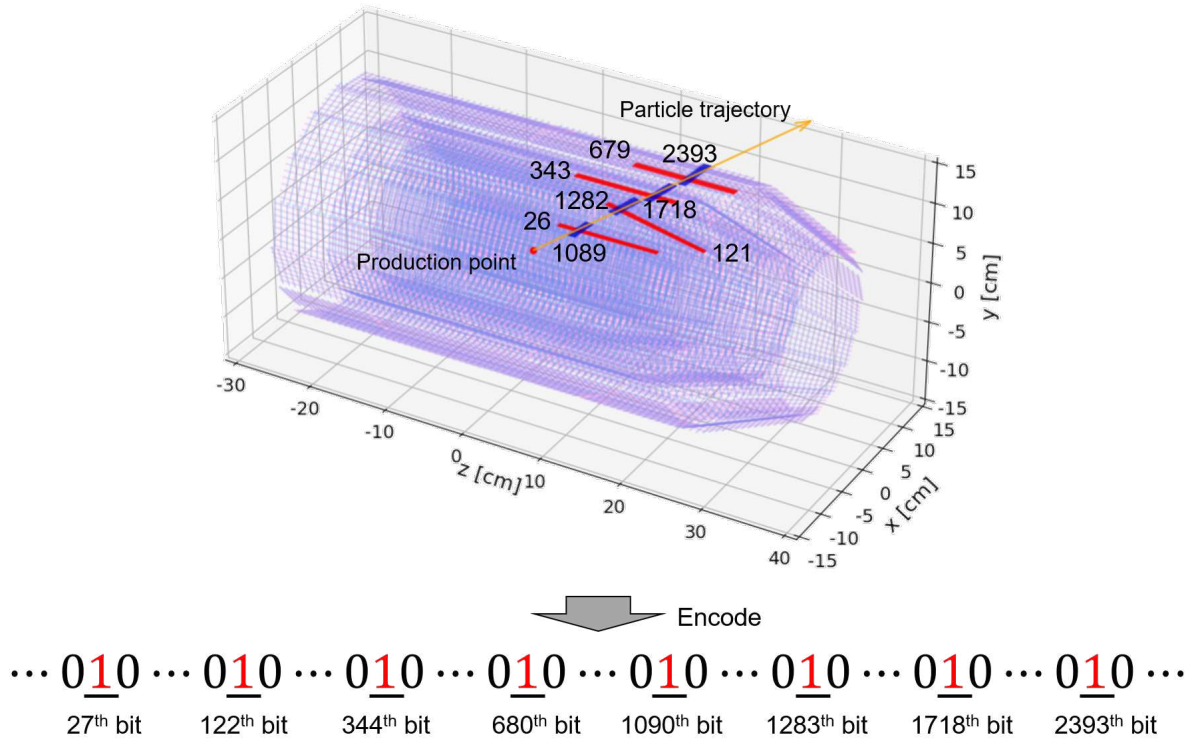

Figure 4.10: Fired cells due to a particle passing through sensors in the case of the PN-128 algorithm. Red(Blue) rectangles represent fired P(N)-cells. The combination of eight fired cells are encoded into a bit string of 3096-width.

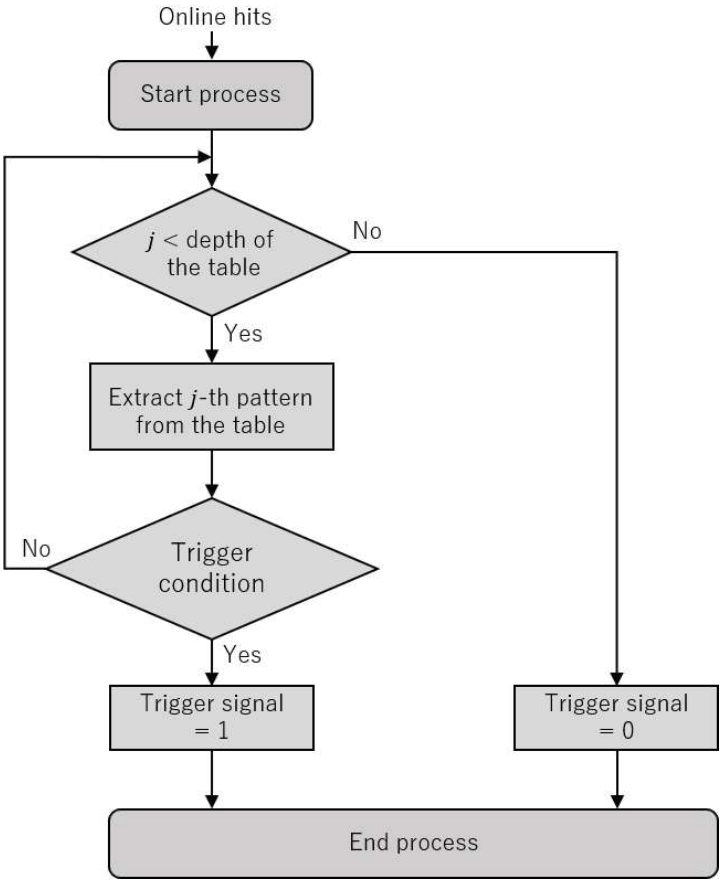

Figure 4.11: Flowchart of the PN-128 and -64 trigger algorithm

4.3 Latching of online hit signal

Since the sampling rate of SNAP128 is 127 MHz, the time window for one frame is about 7.87 ns. The typical momentum of particles produced at SuperKEKB (center-of-mass energy $\sqrt{s} = 10.58\,\mathrm{GeV}$) and recorded by the Belle II detector ranges from several ten MeV/c to several thousand MeV/c. With such momentum, the time for a particle to pass through the TFP-SVD volume from the IP to the layer 6 is estimated to be about $1 - 5$ ns, which is within the time window of one frame of SNAP128. Therefore, basically, it is expected that cells fired in the same frame can be attributed to the same particle, while cells fired at different frames can be attributed to different particles.

However, we must consider that physics events do not occur in sync with the SNAP128 clock. In addition, the time it takes for the voltage of the strip signal to rise and exceed the comparator threshold is not constant. Therefore, all the cells are not always fired in the same frame by a single particle.

Furthermore, this fluctuation is expected to be more pronounced between P-cells and N-cells due to other mechanism. The collected charges on the P-strip are carried by holes, while those on the N-strips are carried by electrons. When a particle passes through a sensor, electrons and holes are produced simultaneously and begin to drift in the sensor bulk under the combined effect of the electric and magnetic fields. However, the effective masses of electrons and holes are different in silicon crystals, resulting in a systematic differences in their drift times [23]. In the MC simulation, the drift velocity of carriers are calculated by

$$\boldsymbol{v}(\boldsymbol{E}, \boldsymbol{B}) = \frac{\mu\boldsymbol{E} + \mu\mu_H \boldsymbol{E} \times \boldsymbol{B} + \mu\mu_H^2 \boldsymbol{B}(\boldsymbol{E} \cdot \boldsymbol{B})}{1 + \mu_H^2 |\boldsymbol{B}|^2} \tag{4.5}$$

where $\boldsymbol{E}$ is electric field, $\boldsymbol{B}$ is magnetic field, μ is carrier mobility, $\mu_H = \mu \cdot r_H$ is Hall mobility and r_H is Hall factor [9]. The main factor that creates the difference between electron and hole velocities is the mobility. The mean values of mobility is $1225.8\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for electron and $410.1\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for hole in the MC simulation. The production of a signal in a strip is simulated by a simplified model, which does not take into account the effect of induced signal on the strips due to charge moving in the sensor (Ramo-Shockley theorem [32, 33]), and it occurs when the carriers are collected on the strip. In this model, the signal production time is calculated by

$$t = \frac{1}{2} \cdot \frac{d}{v_z} \tag{4.6}$$

where d is the distance from the location where the carrier is generated to the sensor surface and v_z is the carrier velocity in the z direction. Fig. 4.12 shows histograms of the signal production times due to electrons or holes. This histogram suggests that the signal production by the holes tends to take longer time of a few nanoseconds than that by the electrons. This fact means that the fired timing of the P-cells tends to be later than that of N-cells.

In order to compensate for these timing discrepancies among the cells, the online hit signals from SNAP128 must be latched for several frames. The number of frames to be latched is called "latch frame number" in this thesis. In the simulation, the latch frame numbers are optimised to be 1 for the N-algorithm and 2 for the PN-algorithm. Fig. 4.13 shows an event where a single particle passes through from layer 3 to layer 6. In this example, the bits of the N-cells of all layers rise in frame 0, while the bits of the P-cells of layer 3, 5 and 6 rise one frame later due to the systematic discrepancy between N-cell and P-cell. Furthermore, the bit of the P-cell

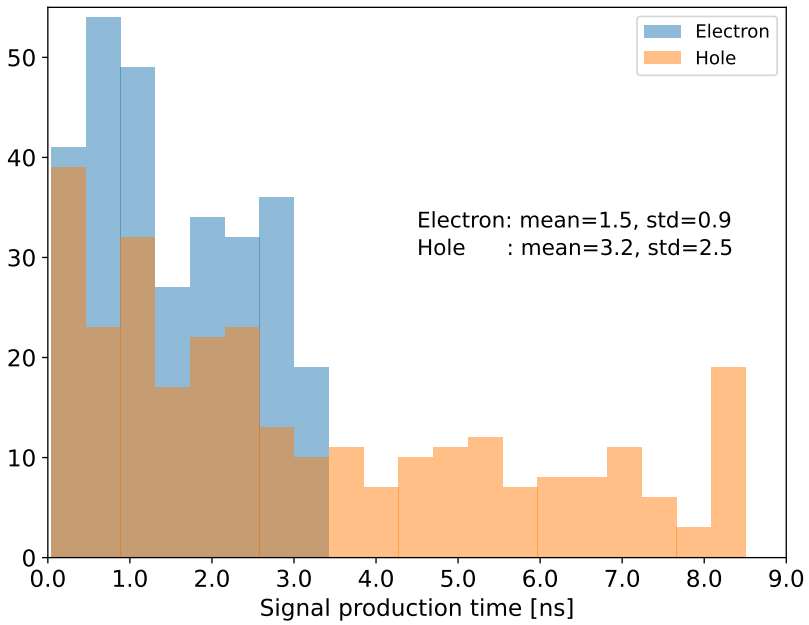

Figure 4.12: Histogram of signal production time. Blue(Orange) represents signal production time due to the electrons(holes).

of layer 4 rises one more frame later due to statistical fluctuation. By latching each signal for two frames, all signals of four layers and both sensor sides are obtained in frame 2.

The operation of latching online hit signal is expected to lead a high fake trigger rate. In real situation, multiple strips are fired and form a cluster when a particle passes through a sensor. Fig. 4.14 shows the time distributions of signal production in the strips of the current SVD. It suggests that the strip at the edge of a cluster has a hit time significantly smaller than that of the central strip [9]. This effect may be explained by the Ramo-Shockley effect, which is not taken into account in the MC simulation. From this fact, the cells in the TFP-SVD may also be fired much faster than in the MC simulation due to the same effect and the time discrepancies among cells may not be as large as observed in the simulation. The optimal latch frame number should be studied using the actual TFP-DSSD sensor in the future.

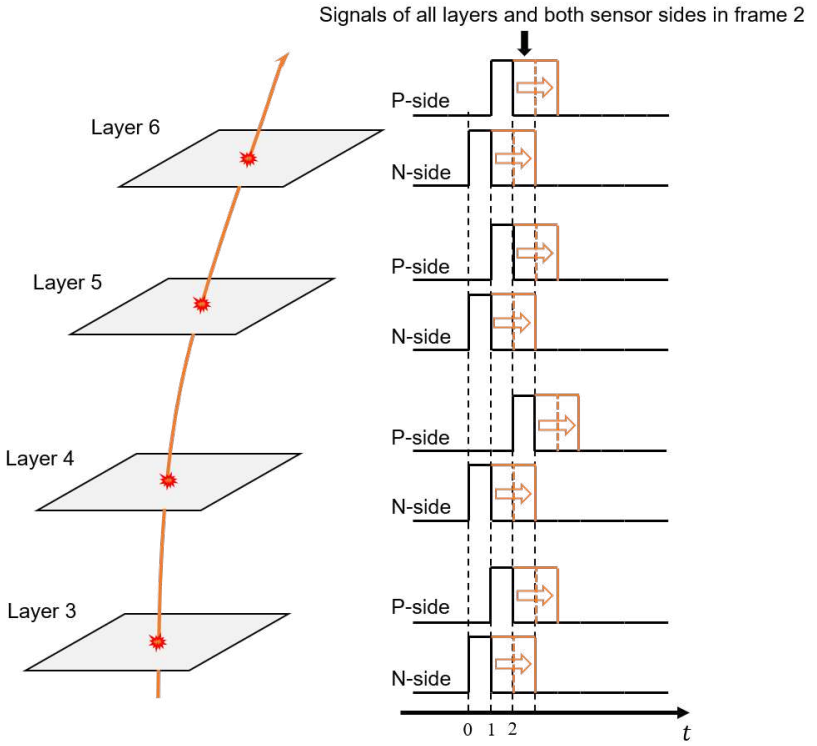

Figure 4.13: The operation to latch the online hit signals for two frames. Black rectangle represents original rising edge of bit. Orange rectangle represents extended bits.

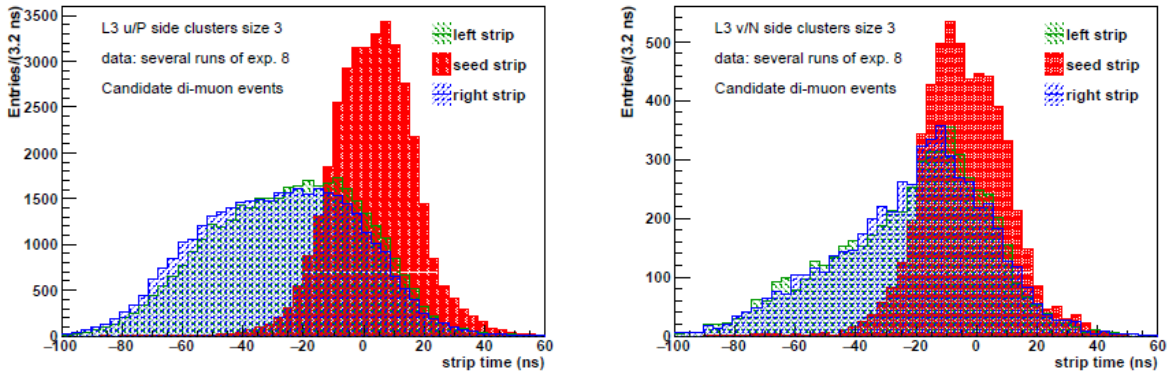

Figure 4.14: Time distributions of the SVD strips belonging to layer 3 clusters of size 3 for perpendicular tracks in di-muon events reconstructed in several runs of 2019 data. The time distribution of central strip is shown in red, while the overlaid time distributions of the left(right) edges strips is shown green(blue) [9]

Chapter 5

Generation of test samples

In order to evaluate the performance of the TFP-SVD trigger, test samples that simulate the online hits assuming the following three types of situations are generated. By applying the trigger algorithms developed in Section 4.2 to these test samples, the evaluation indices discussed in Section 3.3 are investigated.

test case 1 On-IP particle study

test case 2 Off-IP particle study

test case 3 Beam background study

As described in Section 4.1, the MC simulations to generate test samples are performed. The simulated hit signals are sampled for 10 frames in each event. By applying the trigger algorithm to those hit signals of each frame, ten trigger decisions are obtained per event in Chapter 6.

5.1 Test case 1: On-IP particle study

For the evaluation of the trigger efficiency, test samples that simulate the behavior of the On-IP particles are generated as shown in Fig. 5.1 (left). 100,000 events are simulated, and one charged particle is generated at the IP in each event. The range of the parameters of momentum p and its direction (θ and ϕ) are set for the MC simulation as shown in Table 5.1. In each event, p, θ, and ϕ are randomly determined from uniform distributions within the given ranges.

Table 5.1: Parameters for the MC simulation of the On-IP particle study. In each event, momentum, polar angle and azimuthal angle are extracted from uniform distributions within the given ranges.

Parameters	Value
Particle	μ^-
Production point x	$x = 0\,\mathrm{cm}$
Production point y	$y = 0\,\mathrm{cm}$
Production point z	$z = 0\,\mathrm{cm}$
Range of momentum p	$0.1\,\mathrm{GeV}/c \leq p \leq 3.0\,\mathrm{GeV}/c$
Range of polar angle θ	$0^\circ \leq \theta < 180^\circ$
Range of azimuthal angle ϕ	$0^\circ \leq \phi < 360^\circ$
Number of events	100,000

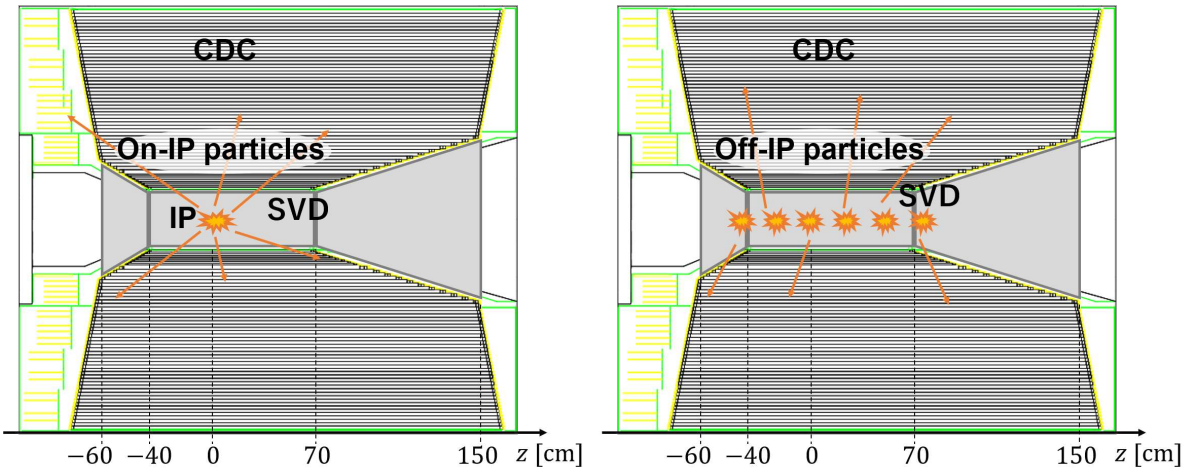

Figure 5.1: Illustration of the MC simulation for the On-IP particle study (left) and for the Off-IP particle study (right)

5.2 Test case 2: Off-IP particle study

For the evaluation of the Off-IP particle rejection power, test samples that simulate the behavior of the Off-IP particles are generated as shown in Fig. 5.1 (right). 100,000 events are simulated, and one charged particle is generated at various points on the z-axis in each event. Similarly to the test case 1, parameters of z, p, θ, and ϕ are randomly determined within the given ranges shown in Table 5.2.

Table 5.2: Parameters for the MC simulation of the Off-IP particle study. At each event, production point, momentum, polar angle and azimuthal angle are extracted from uniform distributions withing the given ranges.

Parameters	Value
Particle	μ^-
Production point x	$x = 0\,\mathrm{cm}$
Production point y	$y = 0\,\mathrm{cm}$
Range of production point z	$-10\,\mathrm{cm} \leq z \leq 10\,\mathrm{cm}$
Range of momentum p	$0.1\,\mathrm{GeV}/c \leq p \leq 3.0\,\mathrm{GeV}/c$
Range of polar angle θ	$0^\circ \leq \theta < 180^\circ$
Range of azimuthal angle ϕ	$0^\circ \leq \phi < 360^\circ$
Number of events	100,000

5.3 Test case 3: Beam background study

In order to evaluate the fake trigger probability, test samples that simulate the behavior of the beam background particles are generated. For this test case, 10,000 events are simulated.

As explained in Section 2.4, the main components of the beam background in SuperKEKB are Touschek effect, Coulomb scattering, Bremsstrahlung, two-photon process, and radiative Bhabha (RBB, BHWide, and BHWide LA). These effects generate many secondary particles, some of which spiral inside the TFP-SVD volume by the magnetic field and make many hits on the sensor. To simulate their generation and behavior, dedicated software of modules are used for each beam background component. For the Touschek, Coulomb scattering, and Bremsstrahlung, SAD (Strategic Accelerator Design) software [34] is used to simulate the propagation and loss of beam particles along the beam ring. AAFH [35] is used for the two-photon events, BBBREM [36] for the RBB, BHWIDE [37] for the BHWide and BHWide LA. The Geant4 is used to simulate the interaction between those particles and sensors as usual. These events are generated at the design luminosity of $\mathcal{L} = 8.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

The background studies [38] have understood background levels in the IR (Interaction Region) and observed discrepancies between the simulation and the measured background. In the studies, data/MC factors which represents the ratio between measured hit occupancy and simulated hit occupancy have been introduced to correct the background simulation. Table 5.3 shows the data/MC factors, which is calculated using the background studies based on the dataset of the 2020 runs and adopted by the SVD group [9].

Since the geometry of the TFP-SVD detector is assumed to be the same as that of the SVD detector, it is expected that the replacement of the SVD with the TFP-SVD does not significantly affect the beam background situation. Therefore, we continue to adopt the above ratios to scale the results of the beam background simulation with the TFP-SVD geometry.

After generating each beam background component, they are mixed and the TFP-SVD hit samples are created at the design luminosity. When creating the TFP-SVD hits, the time of sensor hits and energy depositions in the TFP-SVD are randomized by a dedicated digitizer module. To evaluate the background level, the "cell hit occupancy" is defined as an average fraction of the number of fired cells to the total number of cells. This value depends on the operation of the hit signal latching described in Section 4.3, because the cells fired in the

Table 5.3: Data/MC ratios for each component of beam backgrounds. In the background studies, the design machine parameters are considered at $\mathcal{L} = 8.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

Component	Data/MC ratio
two-photon	1
RBB	1
BHWide	1
BHWide LA	1
HER Brems	3
HER Coulomb	3
HER Touschek	0.2
LER Brems	5
LER Coulomb	5
LER Touschek	4

previous frame contribute to the number of fired cells in the next frame. Table 5.4 and Table 5.5 show the cell hit occupancies in each layer at the design luminosity, and Fig. 5.2 is an event display which shows fired cells by the beam background.

Table 5.4: 128-cell hit occupancy in each layer at the design luminosity of $\mathcal{L} = 8.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

	No latch	Latch for one frame	Latch for two frames
P-cells of layer 3	7.03 %	11.2 %	14.8 %
N-cells of layer 3	2.94 %	4.84 %	6.49 %
P-cells of layer 4	4.32 %	7.54 %	10.5 %
N-cells of layer 4	1.25 %	2.13 %	2.93 %
P-cells of layer 5	4.05 %	7.24 %	10.2 %
N-cells of layer 5	1.07 %	1.84 %	2.55 %
P-cells of layer 6	3.14 %	5.75 %	8.20 %
N-cells of layer 6	0.74 %	1.29 %	1.80 %
P-cells of all layers	3.92 %	6.92 %	9.70 %
N-cells of all layers	1.10 %	1.88 %	2.59 %
Total	2.04 %	3.56 %	4.96 %

Table 5.5: 64-cell hit occupancy in each layer at the design luminosity of $\mathcal{L} = 8.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

	No latch	Latch for one frame	Latch for two frames
P-cells of layer 3	3.92 %	6.37 %	8.49 %
N-cells of layer 3	1.58 %	2.64 %	3.57 %
P-cells of layer 4	2.35 %	4.15 %	5.85 %
N-cells of layer 4	0.66 %	1.13 %	1.57 %
P-cells of layer 5	2.18 %	3.94 %	5.62 %
N-cells of layer 5	0.57 %	0.98 %	1.37 %
P-cells of layer 6	1.66 %	3.07 %	4.41 %
N-cells of layer 6	0.39 %	0.69 %	0.96 %
P-cells of all layers	2.11 %	3.77 %	5.33 %
N-cells of all layers	0.59 %	1.01 %	1.39 %
Total	1.09 %	1.93 %	2.71 %

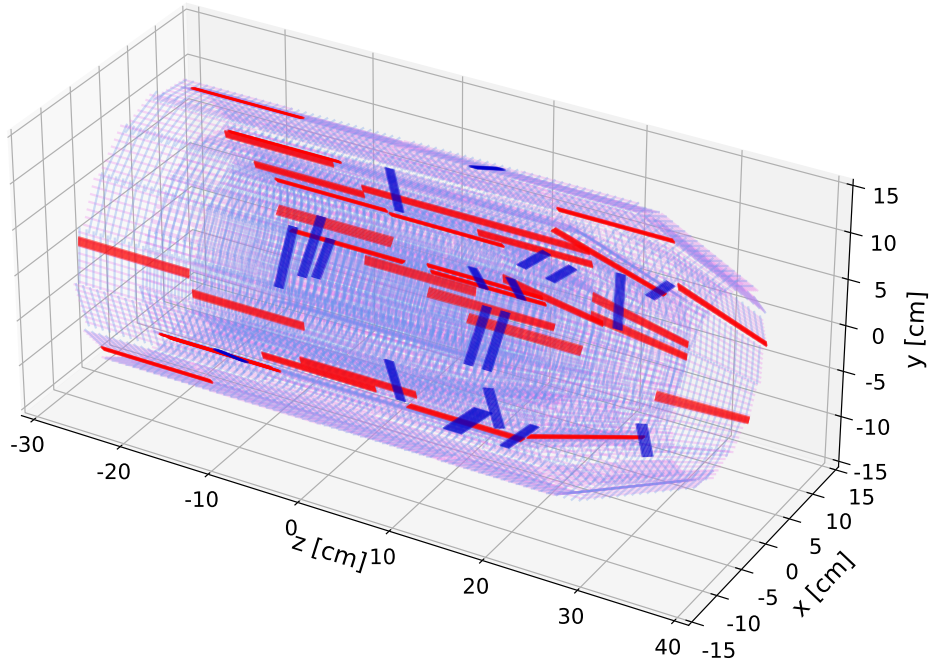

Figure 5.2: Event display of a certain beam background event at the design luminosity of $\mathcal{L} = 8.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Red(Blue) rectangles represent fired 128-P(N)-cells.

Chapter 6

Performance evaluation

In this chapter, the N-128, PN-128, and PN-64 algorithms are applied to each test case generated in Chapter 5 and their performances are evaluated.

6.1 Evaluation of the trigger efficiency

In this section, the trigger algorithms are applied to the test case 1 (On-IP particle study) and their trigger efficiencies are evaluated.

N-128 algorithm First of all, the efficiency of the N-128 algorithm is evaluated. At the same time, the effect of the relaxed trigger conditions of the 3/4-allθ matching and 3/4-selectedθ matching are discussed.

Fig. 6.1 shows the trigger efficiency as a function of the particle transverse momentum p_{T}. The events in which θ is in the range of 17° to 150° are selected for the trigger efficiency calculation. The result of the Full matching condition is represented by the blue plots. This plots shows that the trigger efficiency does not strongly dependent on p_{T}. The average trigger efficiency for the events with $p_{\mathrm{T}} > 0.2\,\mathrm{GeV}/c$ is 90.5 %, which is below the target of 95 %. Fig. 6.2 shows the trigger efficiency as a function of the particle ejection angle θ. The events with p_{T} of larger than $0.5\,\mathrm{GeV}/c$ are selected. The dependency of the trigger efficiency on θ can be seen in this figure. As anticipated in Section 4.2.1, the trigger efficiency drops significantly in the θ regions listed in Table 4.3.

In Fig. 6.1 and Fig. 6.2, the orange plots represent the trigger efficiency of the 3/4-allθ matching condition, and the green plots represent that of the 3/4-selectedθ matching condition. In Fig. 6.1, the average trigger efficiency for the events with $p_{\mathrm{T}} > 0.2\,\mathrm{GeV}/c$ is 98.4 % for the 3/4-allθ matching condition and 95.7 % for the 3/4-selectedθ matching condition. Fig. 6.2 shows that the dependency of trigger efficiency on θ are weakened for these two conditions.

From these facts, the Full matching condition is not useful due to the existence of the sensor insensitive areas. On the other hand, 3/4-allθ matching condition can cover the direction of the low sensor hit efficiency and achieve the high trigger efficiency above the target of 95 %. Even in the case of 3/4-selectedθ matching condition, although the trigger efficiency is lower than the 3/4-allθ matching due to limited application of the relaxed matching condition, it still be above the target.

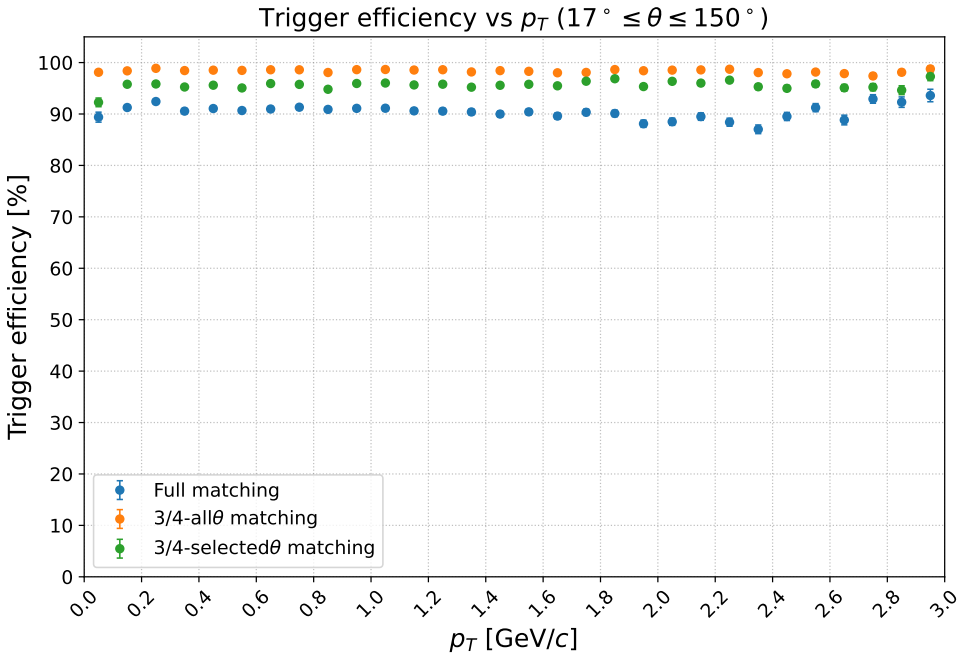

Figure 6.1: Efficiencies of the N-128 algorithm for On-IP particles. The horizontal axis is transverse momentum p_{T}. The blue(orange, green) plots represent the Full(3/4-allθ, 3/4-selectedθ) matching condition.

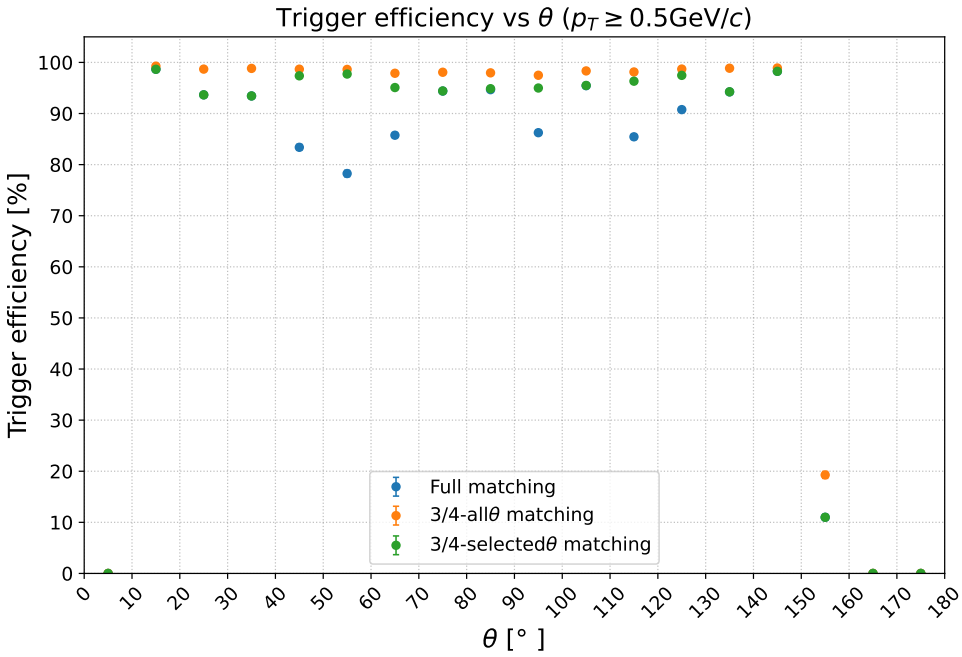

Figure 6.2: Efficiencies of the N-128 algorithm for On-IP particles. The horizontal axis is particle ejection angle θ. The blue(orange, green) plots represent the Full(3/4-allθ, 3/4-selectedθ) matching condition.

PN-128 and PN-64 algorithms The efficiencies of the PN-128 algorithm are shown in Fig. 6.3 and Fig. 6.4. The efficiencies of the PN-64 algorithm are shown in Fig. 6.5 and Fig. 6.6. As with the N-128 algorithm, it can be seen that the trigger efficiencies of the Full matching conditions are low level and have θ dependence, while the 3/4-allθ matching and the 3/4-selectedθ matching condition have high trigger efficiencies. Those results are summarized in Table 6.1. The efficiency of the PN-algorithms are slightly lower than that of the N-algorithm because they require matching using more cells than the N-algorithm. However, from the viewpoint of the trigger efficiency, no significant differences can be seen among these algorithms.

Table 6.1: Trigger efficiencies of each trigger algorithm and each trigger condition. The average value is calculated using the events with $p_{\mathrm{T}} > 0.2\,\mathrm{GeV}/c$

	Full matching	3/4-allθ matching	3/4-selectedθ matching
N-128	90.5 %	98.4 %	95.7 %
PN-128	89.8 %	97.9 %	94.8 %
PN-64	89.9 %	97.3 %	94.2 %

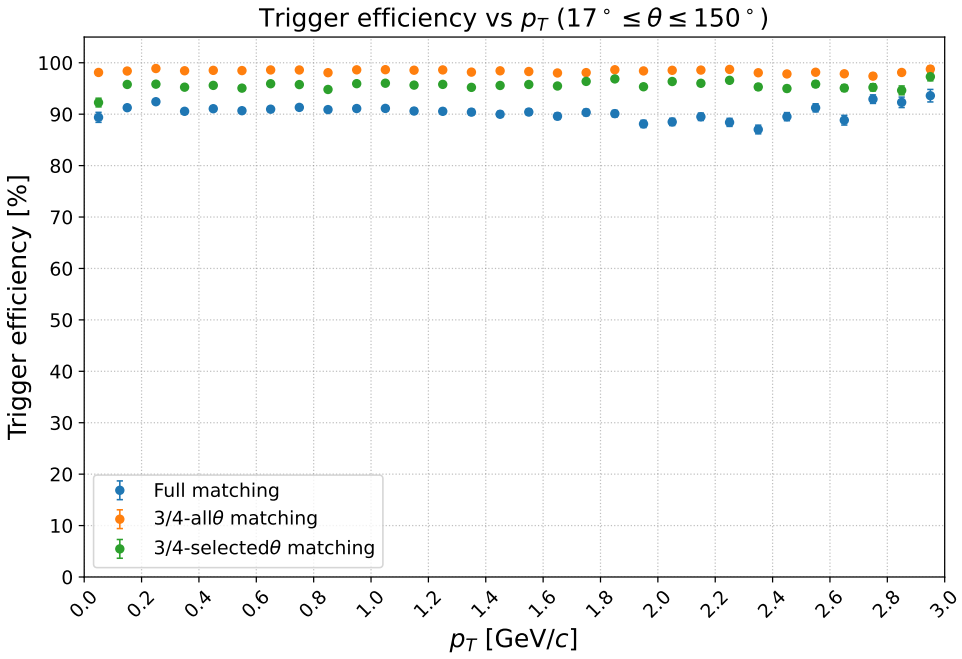

Figure 6.3: Efficiencies of the PN-128 algorithm for On-IP particles. The horizontal axis is transverse momentum p_{T}. The blue(orange, green) plots represent the Full(3/4-allθ, 3/4-selectedθ) matching condition.

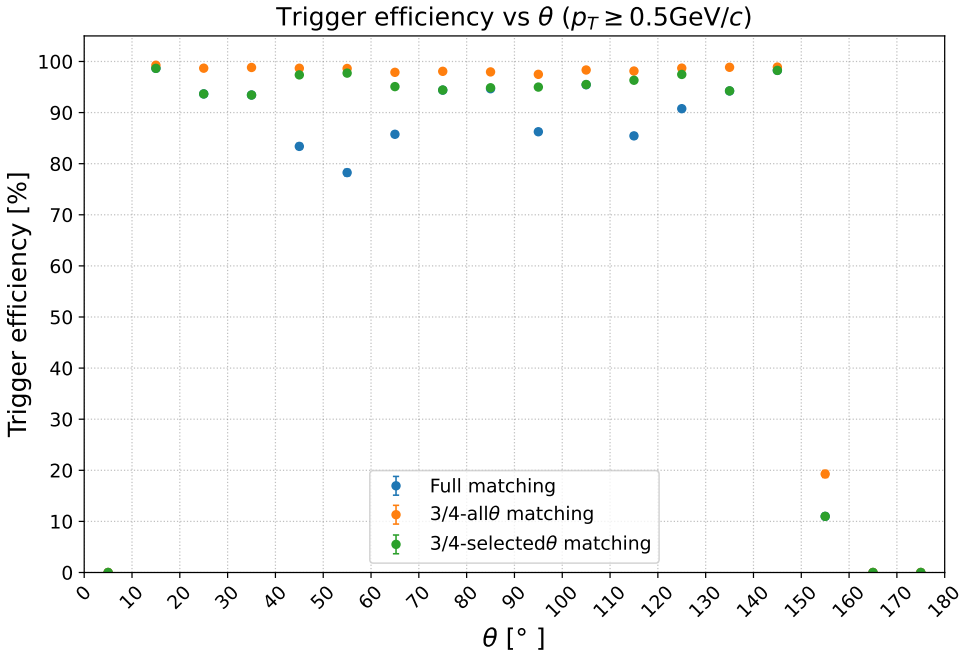

Figure 6.4: Efficiencies of the PN-128 algorithm for On-IP particles. The horizontal axis is particle ejection angle θ. The blue(orange, green) plots represent the Full(3/4-allθ, 3/4-selectedθ) matching condition.

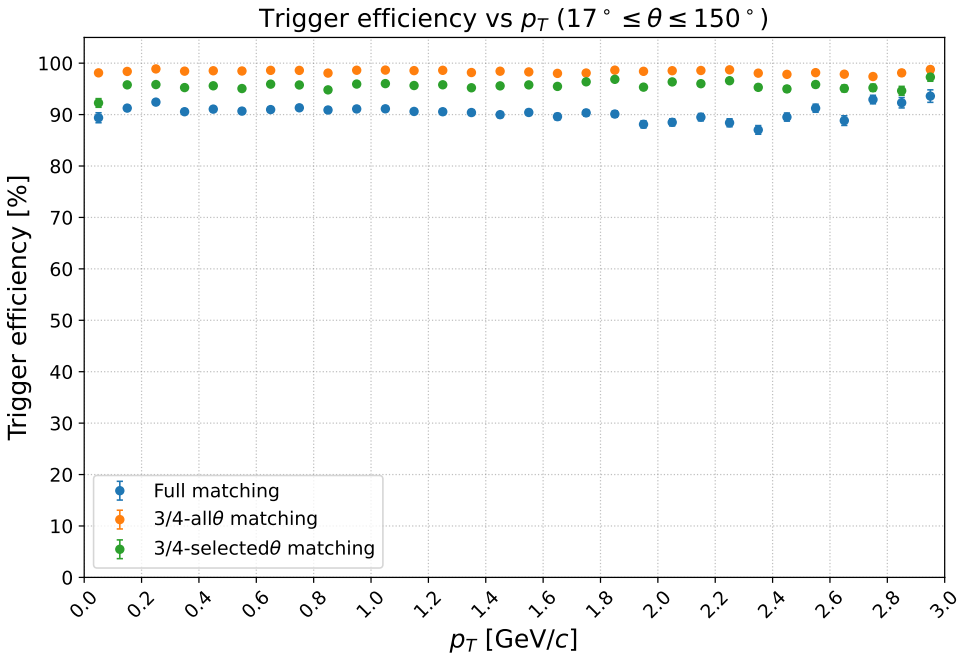

Figure 6.5: Efficiencies of the PN-64 algorithm for On-IP particles. The horizontal axis is transverse momentum p_{T}. The blue(orange, green) plots represent the Full(3/4-allθ, 3/4-selectedθ) matching condition.

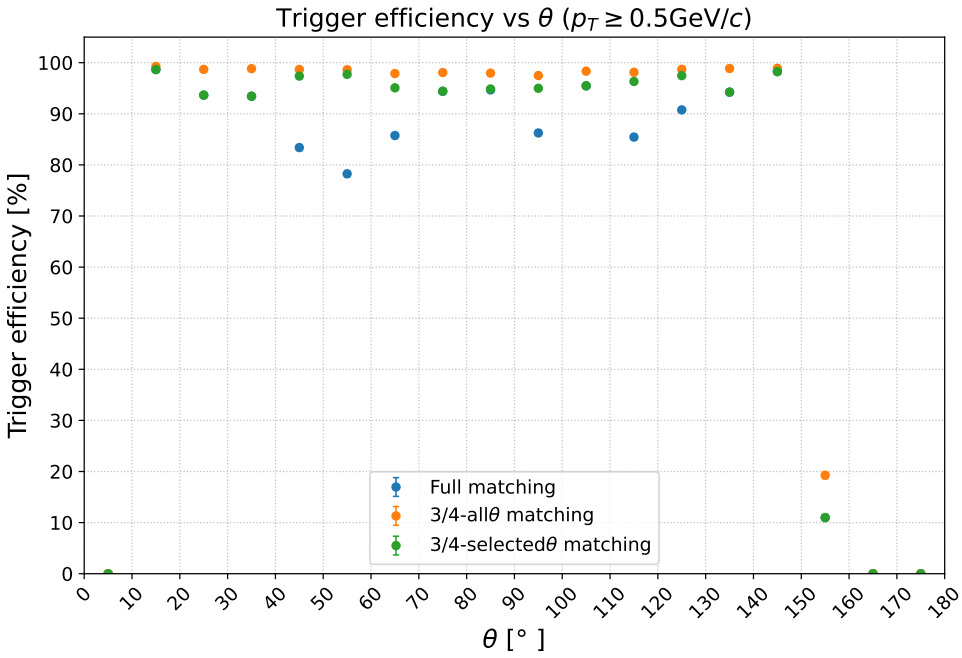

Figure 6.6: Efficiencies of the PN-64 algorithm for On-IP particles. The horizontal axis is particle ejection angle θ. The blue(orange, green) plots represent the Full(3/4-allθ, 3/4-selectedθ) matching condition.

6.2 Evaluation of the discrimination power for On-IP particles

In this section, the trigger algorithms are applied to the test case 2 (Off-IP particle study) and their particle selection areas, defined in Section 3.3, are evaluated. In this section and the next section, only the 3/4 matching conditions are considered.

Fig. 6.7 shows the trigger efficiency as a function of the particle production point z under the 3/4-allθ matching condition. The events with $p_{\mathrm{T}} \geq 0.5\,\mathrm{GeV}/c$ and $30^{\circ} \leq \theta \leq 120^{\circ}$ are selected for the trigger efficiency calculation. The blue plots represent the result of the N-128 algorithm, the orange plots represent that of the PN-128 algorithm, and the green plots represent that of the PN-64 algorithm. These three plots show similar behavior. They have high trigger efficiencies about 98 % around the IP ($z = 0$) and decrease as z moves away from the origin. However, the widths of the three plots are different according to their capability to discriminate On-IP particles from Off-IP particles. The full width at half maximum (FWHM) of the plots is 5.2 cm for the N-128 algorithm, 4.2 cm for the the PN-128 algorithm, and 2.2 cm for the PN-64 algorithm. Moreover, the particle selection area is $-5.9\,\mathrm{cm} < z < 6.9\,\mathrm{cm}$ for the N-128 algorithm, $-4.3\,\mathrm{cm} < z < 4.3\,\mathrm{cm}$ for the PN-128 algorithm, and $-2.1\,\mathrm{cm} < z < 2.3\,\mathrm{cm}$ for the PN-64 algorithm. From these fact, the PN-algorithms have higher Off-IP particle rejection power than the N-algorithm. Furthermore, it is also found that the algorithm using 64-cell has much higher discrimination power than that using 128-cell.

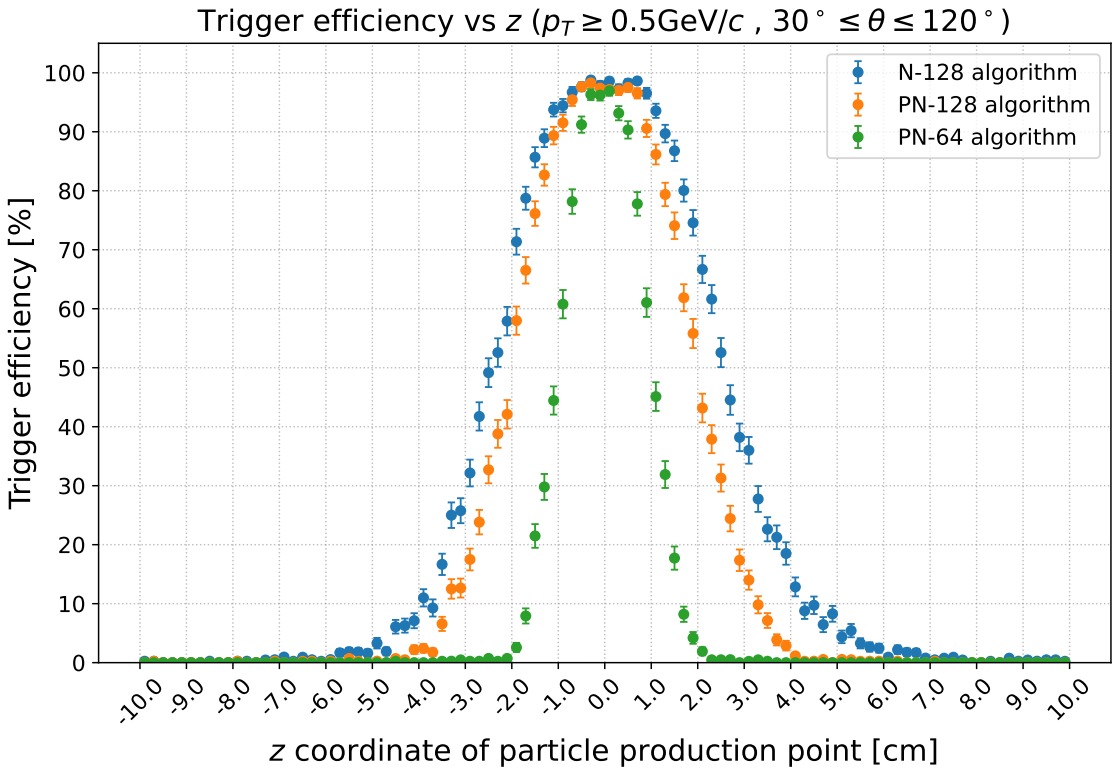

Figure 6.7: Trigger efficiencies under the 3/4-allθ matching condition for Off-IP particles. The horizontal axis is particle production point z. The blue(orange, green) plots represent the N-128(PN-128, PN-64) algorithm.

Fig. 6.8 shows the trigger efficiency as a function of the particle production point z under the 3/4-selectedθ matching condition. The same trend as above can be seen in this figure, however, the widths of these plots are much narrower than above. The FWHMs and particle selection areas are summarized in Table 6.2. It is found that the particle selection areas of all the algorithms except for the N-128 algorithm can achieve the target of $|z| < 5\,\mathrm{cm}$. From the table, it can be seen that FWHMs of the 3/4-selectedθ matching condition is about half of that of the 3/4-allθ matching condition. From this facts, the relaxed matching condition significantly reduces the z position resolution of the trigger.

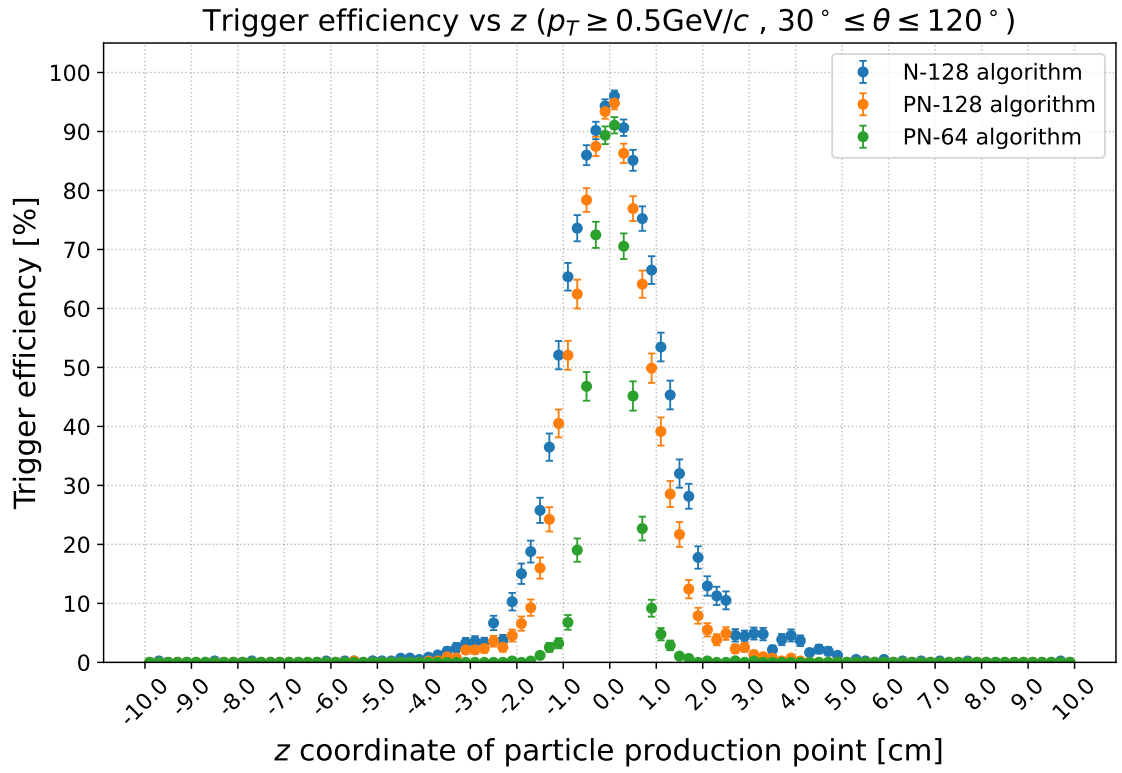

Figure 6.8: Trigger efficiencies of 3/4-selectedθ matching condition for Off-IP particles. The horizontal axis is particle production point z. The blue(orange, green) plots represent the N-128(PN-128, PN-64) algorithm.

Table 6.2: FWHMs and particle selection areas of each trigger algorithm and each trigger condition

	3/4-allθ matching		3/4-selectedθ matching	
	FWHM	Particle selection area	FWHM	Particle selection area
N-128	5.4 cm	$-5.9\,\mathrm{cm} < z < 6.9\,\mathrm{cm}$	2.6 cm	$-3.9\,\mathrm{cm} < z < 5.1\,\mathrm{cm}$
PN-128	4.2 cm	$-4.3\,\mathrm{cm} < z < 4.3\,\mathrm{cm}$	2.2 cm	$-3.3\,\mathrm{cm} < z < 3.3\,\mathrm{cm}$
PN-64	2.2 cm	$-2.1\,\mathrm{cm} < z < 2.3\,\mathrm{cm}$	1.0 cm	$-1.7\,\mathrm{cm} < z < 1.7\,\mathrm{cm}$

6.3 Evaluation of the fake trigger probability

In this section, the trigger algorithms are applied to the test case 3 (Beam background study) and their fake trigger probability are evaluated. The TFP-SVD trigger, synchronized with the SNAP128 clock of 127 MHz, makes trigger decision every about 8 ns. Thus, the fake trigger probability is evaluated in that time window. At the same time, as described in Section 3.2.2, the fake trigger probability must be evaluated in the time window of about 60 ns when matching it with the CDC trigger. Therefore, the fake trigger probability of the logic OR of 8 frames is also evaluated.

The fake trigger probabilities per frame are shown in Table 6.3, and those per 8 frames are shown in Table 6.4. Under a harsh beam background, since many particles contribute to the fake track reconstruction, high position resolution is required to suppress the fake trigger due to such tracks. Since the PN-algorithm (4 layers $\times$ 2 sides) checks more hits and has a tighter trigger conditions than the N-algorithm (4 layers $\times$ 1 side), its fake trigger probability is smaller. Especially for the PN-algorithm with 3/4-selectedθ matching condition, those value for 8 frames are below the target of 10 %.

Table 6.3: Fake trigger probability per frame of each trigger algorithm and each trigger condition

	3/4-allθ matching	3/4-selectedθ matching
N-128	51.0 %	8.4 %
PN-128	10.8 %	1.6 %
PN-64	5.2 %	0.9 %

Table 6.4: Fake trigger probability per 8 frame of each trigger algorithm and each trigger condition

	3/4-allθ matching	3/4-selectedθ matching
N-128	94.6 %	35.8 %
PN-128	35.8 %	5.6 %
PN-64	18.2 %	3.1 %

6.4 Discussion

We evaluated the performance of the three different algorithms with the three different trigger conditions in the three test cases. In terms of the fake trigger probability, the 3/4-selectedθ matching condition shows the best performance among the three trigger conditions. The performances of the trigger algorithms with the 3/4-selectedθ matching condition are summarized in Table 6.5.

Table 6.5: Performance of each trigger algorithm under the 3/4-selectedθ matching condition

	Trigger efficiency	Particle selection area	Fake trigger probability
N-128	95.7 %	$-3.9\,\mathrm{cm} < z < 5.1\,\mathrm{cm}$	35.8 %
PN-128	94.8 %	$-3.3\,\mathrm{cm} < z < 3.3\,\mathrm{cm}$	5.6 %
PN-64	94.2 %	$-1.7\,\mathrm{cm} < z < 1.7\,\mathrm{cm}$	3.1 %

Trigger efficiency

From the On-IP particle study, it is found that sensor insensitive area constraints the trigger efficiency. It is attributed to the geometry of the sensor, any improvement cannot be expected as long as the trigger condition requires perfect matching between online hits and the pattern table using all four layers. Therefore, we have to allow for missing hits in at least one layer for a high trigger efficiency. In fact, while the trigger efficiencies under the Full matching condition are below the target of 95 %, those under the 3/4-allθ matching condition are above the target. Regarding the 3/4-selectedθ matching condition, all trigger efficiencies show the values close to 95 % as shown in Table 6.5.

Considering the discrimination power for On-IP particles and the fake trigger probability discussed below, the PN-128 and PN-64 algorithms are desired. However, their trigger efficiencies are slightly below the target due to the existence of the sensor insensitive areas. Two ideas can be considered in order to increase the trigger efficiency. One is to relax the trigger conditions further. Trigger conditions allowing for two or more missing hits while maintaining the current SVD geometry are expected to result in unacceptable low discrimination power for On-IP particles and high fake trigger probability. Thus, at the same time, it is also necessary to consider increasing the number of layers by replacing part of layers of the CDC or involving the PXD. In that case, we can allow for missing hits in more layers to improve the trigger efficiency. The other is to reduce the insensitive areas of the sensors by increasing the sensor size. However, the larger the sensor size, the longer the strip length, resulting in the larger electrical noise. Therefore, this idea must be carefully considered in the TFP-SVD upgrading project.

Discrimination power for On-IP particles

The Off-IP particle study shows that all the TFP-SVD triggers have so strong discrimination power for On-IP particles compared to the CDC trigger. In particular, the PN-128 and PN-64 algorithms with the 3/4-selectedθ matching condition achieve the target of $|z| < 5\,\mathrm{cm}$. They can narrow the limit on the current particle selection area of the CDC trigger $|z| < 15\,\mathrm{cm}$ by a factor of 3 or more. The particle selection area of the PN-64 algorithm is about half of that of the PN-128 algorithm. From this fact, the algorithm using the 64-cells has stronger discrimination power for On-IP particles. Therefore, there is room to consider other algorithms using further smaller cells.

The shape of the plots in the 3/4-selectedθ matching condition is sharper than that in the 3/4-allθ matching condition. This fact means matching condition using only three out of the four layers significantly reduces the z position resolution of the trigger.

Fake trigger probability

The PN-algorithms with 3/4-selectedθ matching condition can achieve the target on the fake trigger probability. However, the obtained values of a few percent per frame are interpreted as a fake trigger rate of $\mathcal{O}(1)$ MHz. Hence, it is difficult to use them as a standalone sub-trigger. By taking the matching of the CDC and TFP-SVD triggers, the TFP-SVD trigger offers to significantly suppress the fake CDC triggers. The fake trigger rate is expected to be reduced by more than a factor of 10. Considering the reduction of the CDC background trigger rate by taking the matching of the CDC and TFP-SVD triggers, the future trigger rate projections in Table 3.2 are modified as Table 6.6 and the upper limit of 20 kHz for the Total CDCTRG can be observed. Furthermore, additional trigger bits for other physics events can participate in the available space of the trigger rate.

Table 6.6: Projected exclusive rates of the CDC trigger bits at the target luminosity of $\mathcal{L} = 6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ when taking the matching with the TFP-SVD trigger. For the TFP-SVD trigger algorithms, 3/4-selectedθ matching condition is applied.

Trigger bit	No TFP-SVD trigger	Matching with PN-128 algorithm	Matching with PN-64 algorithm
$B\bar{B}$ CDCTRG	28.7 kHz	8.2 kHz	7.7 kHz
Low-multi CDCTRG	25.3 kHz	6.8 kHz	6.3 kHz
Total CDCTRG	54.0 kHz	15.0 kHz	14.0 kHz

In the calculation of the projected CDC trigger rates in Table 6.6, we considered the simplest matching method, which takes the logic AND of the CDC and TFP-SVD triggers. We can also consider another more complicated matching method called ϕ-matching. The concentric TFP-SVD and CDC detectors are divided into several sections in the ϕ direction. The ϕ-matching determines whether the TFP-SVD and CDC simultaneously find particles in the same ϕ section. This matching method is expected to have strong rejection power for low momentum background particles, which do not reach the CDC volume and make many hits in the TFP-SVD. As a next task, we should develop the ϕ-matching algorithm.

Chapter 7

Firmware development for TFP-SVD trigger

In this chapter, the TFP-SVD trigger algorithms developed in Chapter 4 is implemented as firmware. For the first trial, the PN-128 algorithm is chosen, which has a medium number of cells and table patterns.

7.1 Core logic circuit of TFP-SVD trigger

The PN-128 trigger is implemented in the UT4. The FPGA of Xilinx Virtex Ultrascale XCVU080 is mounted on the test board, whose specification is shown in Table 2.6. The clock frequency of the FPGA is set to 127 MHz. As described in Section 4.2, the algorithm consists of three steps. First, the online hit signal is latched for two clocks. Second, the online hit signal is compared with each pattern of the cell pattern table, which contains 88,553 patterns. Finally, trigger decision is made: trigger signal is issued if the online hits match at least one pattern of the pattern table, otherwise the event is vetoed.

The circuit to latch online hit signal is realized as shown in Fig. 7.1. In this circuit, an input signal is split into two, and one is latched for one clock by a flip-flop. By taking the logic OR of the direct input signal and the latched signal, the output signal becomes the logic OR of the previous frame signal and the current frame signal. By latching the output signal further using another flip-flop and taking the logic OR with the direct input signal, the final output becomes the logic OR of three frames. This component is named "latch circuit". The relation between input signal and output signal of the latch circuit is shown in Fig. 7.2. It can be seen that the input signal rises in frame 0 and falls in frame 1, while the output signal rises in frame 0 and falls in frame 3.

Online hits and each pattern of the pattern table are represented by a bit string of 3096-width. Since the width of the bit string is too long to be implemented into a single bit array of the FPGA, it is divided into eight sub-strings. Each sub-string corresponds to each layer from 3 to 6 and to one of the sensor surface sides, either P-side or N-side. For example, since there are 960 cells on the N-side of the layer 6, the sub-string for the section is implemented in a bit array with 960-width.

In this study, the trigger conditions of the Full matching and 3/4-allθ matching are tried to be implemented on a test basis. For the Full matching condition, the circuit to compare online hits with each pattern of the pattern table is realized as Fig. 7.3. It is named "comparison circuit". The patterns of the table, whose size is about 32 MB ($\approx 3096\,\text{width} \times 88,553\,\text{depth}$), are stored in registers of the FPGA. The comparisons are performed for each sub-string. After taking the logic AND of the pattern and online hits, the equivalence operation (=) between

the result and the pattern is performed. If all the results of comparison for each sub-string are "TRUE", a sub-output signal is set to '1', otherwise the sub-output signal is set to '0'. For the 3/4-allθ matching condition, the comparison between online hits and each pattern of the table is performed as Fig. 7.4. The comparison without one layer is realized on firmware by not using the corresponding sub-strings. For example, when performing a comparison without layer 3, the same component as the comparison circuit of the Full matching condition except that sub-strings for P-side and N-side of layer 3 are not used is applied. The comparisons without layer 4, 5, or 6 are performed in the same way, then, the sub-output signal is generated by taking the logic OR of those four results.

These comparison circuits are executed for all patterns of the cell pattern table in parallel, and sub-outputs for the number of patterns of the table are generated. To issue the sub-trigger signal if the online hit signal matches at least one patterns of the table, the logic OR of all the 88,553 sub-outputs is taken at the end of the overall circuit of the algorithm. The overall circuit is shown in Fig. 7.5. The circuit is called "core logic circuit". When taking the logic OR of the sub-outputs, several flip-flops are needed to meet the timing constraint of the FPGA. These flip-flops at this part determine the overall latency of the algorithm. The core logic circuit can be implemented in one UT4 board. Table 7.1 shows the resource utilization of the FPGA. It can be seen that there is adequate room for resource despite the implementation of the large pattern table and a lot of comparison circuits.

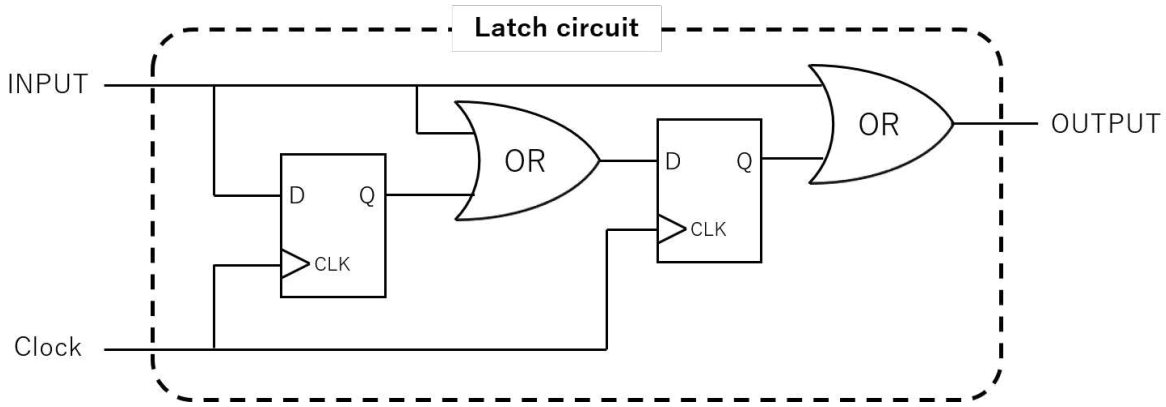

Figure 7.1: Latch circuit to extend bit rise state by two frames

Table 7.1: Resource utilization of the FPGA

	Full matching	3/4-allθ matching
Look-up table (LUT)	8.43 %	9.41 %
RAM for LUT	0.44 %	0.49 %
Flip-flop registers (FF)	1.67 %	1.47 %
Block RAM (BRAM)	2.67 %	2.74 %
IO	11 %	11.82 %
Global buffer (BUFG)	0.31 %	0.31 %

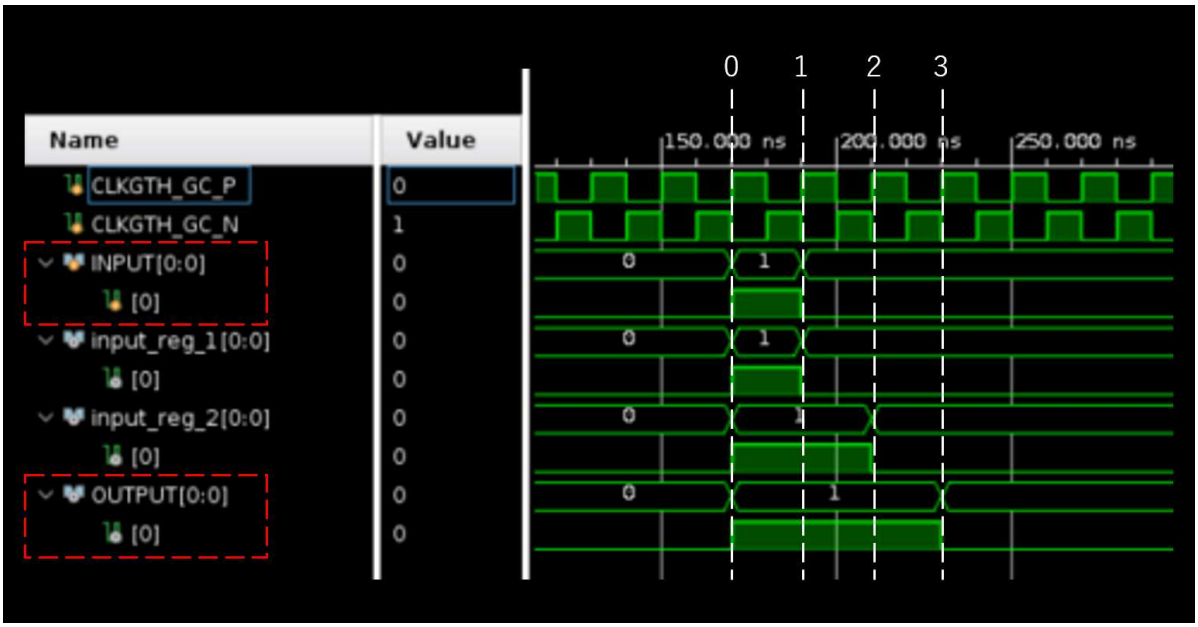

Figure 7.2: Output of the latch circuit in simulation. The bit of the signal named "INPUT" rises in frame 0 and falls in frame 1. The bit of the signal named "OUTPUT" rises in frame 0 and falls in frame 3.

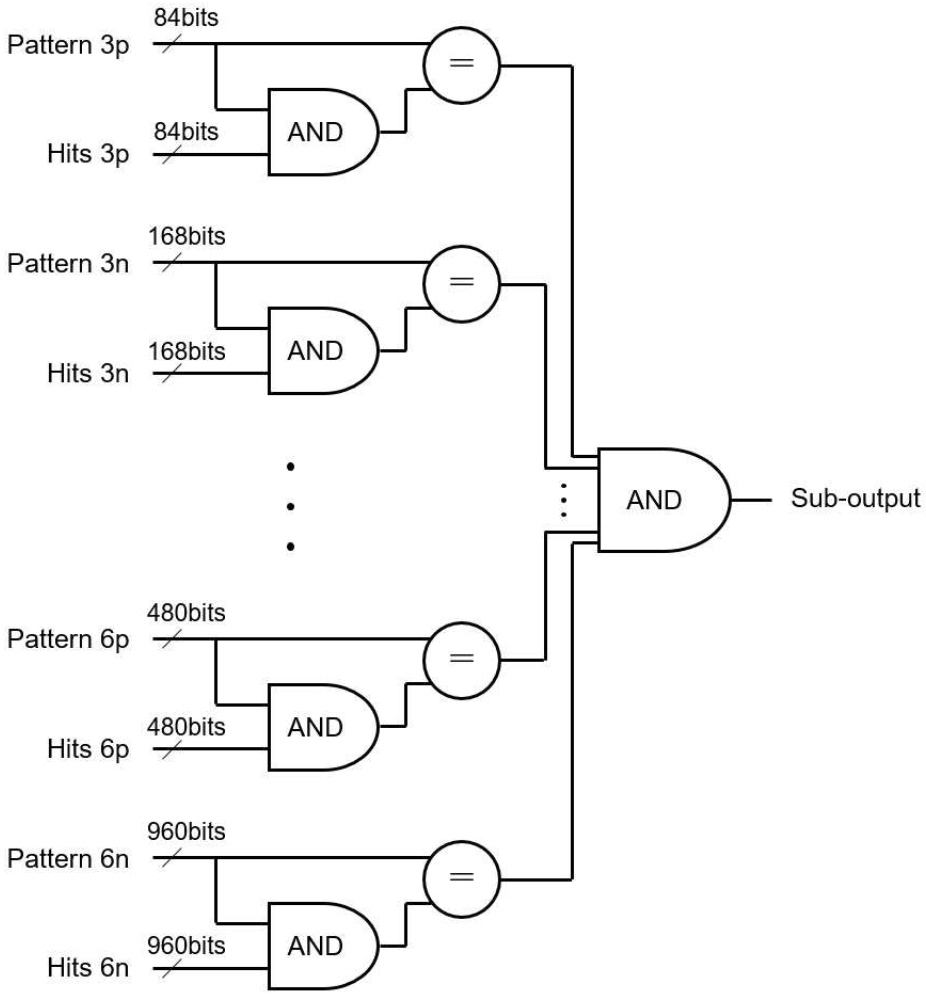

Figure 7.3: Comparison circuit for the Full matching trigger condition. 3p(n) and 6p(n) represent the p(n) side of the layer 3 and 6. The online hits and the pattern of the table are compared for each sub-string.

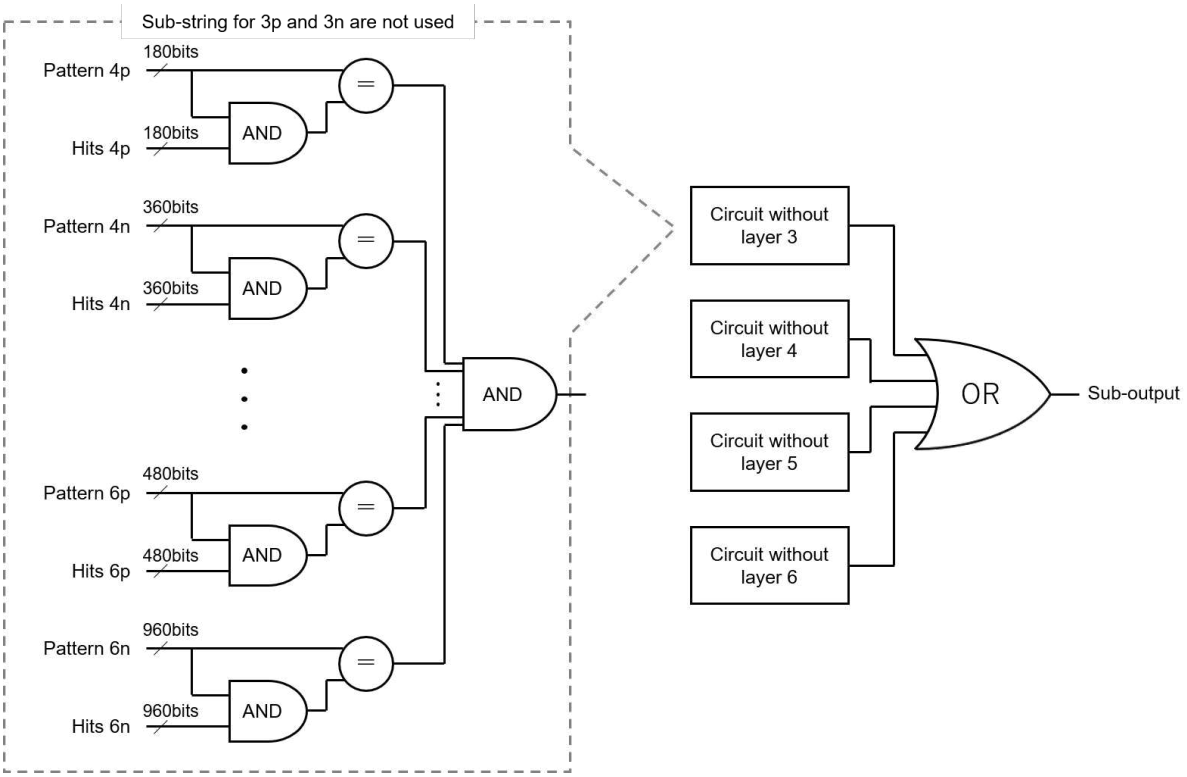

Figure 7.4: Comparison circuit for the 3/4-allθ matching trigger condition. The left side shows the sub component for the comparison without layer 3, in which sub-strings for P-side and N-side of layer 3 are not used. The sub-output signal is the logic OR of the outputs form the sub components without layer 3, 4, 5, or 6.

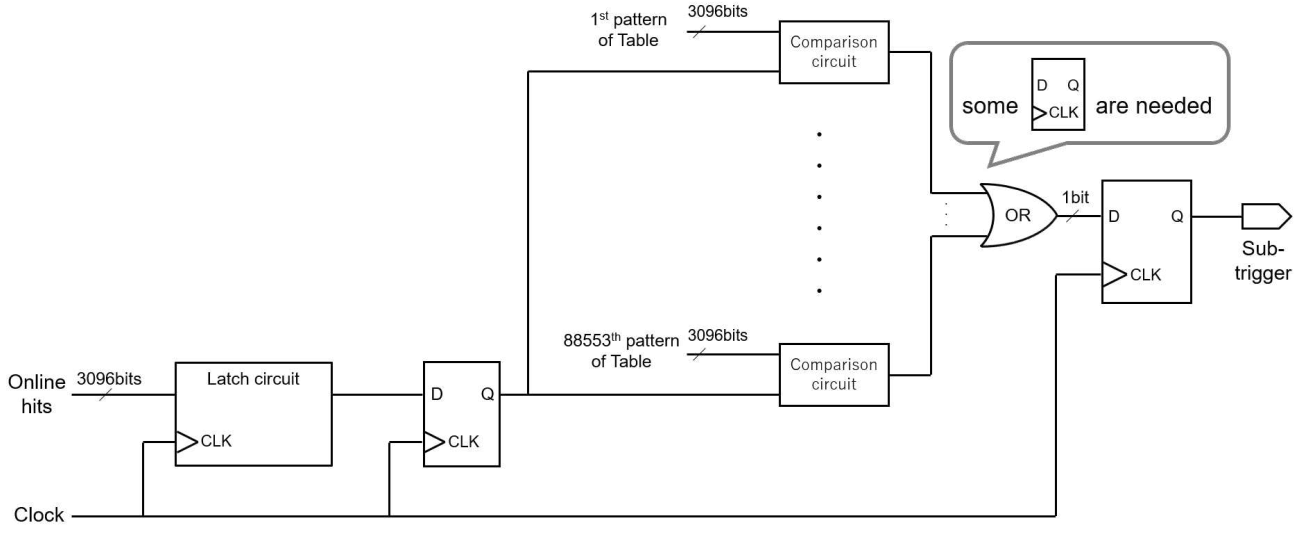

Figure 7.5: Core logic circuit. In this figure, the notation of the sub-strings is simplified and represented as a single 3096-bit signal.

7.2 Operation test of the FPGA

For operation test whether the core logic is implemented correctly, the test samples generated in Chapter 5 are input in the core logic circuit, and the output sub-trigger signal is checked if the results are the same as the simulation results in Chapter 6. The hit samples are stored in Block RAM (BRAM) of the FPGA, in which the hit signal of each frame of each event is in turn input into the core logic circuit at the frequency of 127 MHz. The trigger output can be checked using ChipScope, which is a tool to probe internal signals of the FPGA.

For each test case, 2000 events are input and the results of the triggers are examined. Fig. 7.6 shows the snapshot of ChipScope. As a result, it is confirmed that the core logic circuit reproduces the results obtained by the simulation. From this fact, the algorithm developed in Chapter 4 can be realized as firmware. The signal of the "Input_flag" in Fig. 7.6 is set to '1' when each event is input to the core logic. By counting the gap between the clocks of the "Input_flag" and trigger output, the latency of the core logic can be measured. For both the Full matching and 3/4-allθ matching conditions, the latencies are less than 100 ns (10 clocks).

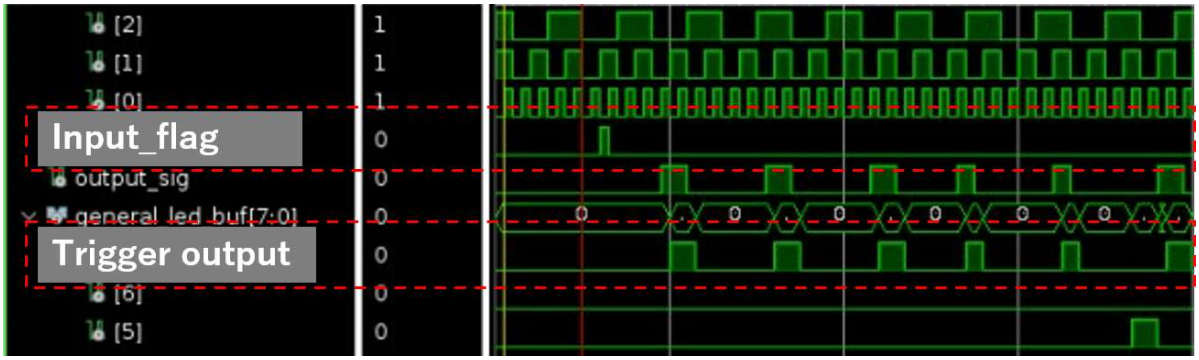

Figure 7.6: Snapshot of the ChipScope. From this output, trigger result and the latency of the core logic can be examined.

7.3 Overall configuration of the firmware

This section explains the overall data transfer from front-end ASICs to the GRL (Section 2.6.1) and estimates the trigger latency of the TFP-SVD trigger.

7.3.1 Data transfer

The considered design of the overall firmware setup is shown in Fig. 7.7. The entire TFP-SVD detector contains 3096 SNAP128 front-end ASICs. Their digitized signals are converted into optical signals and transmitted via optical fiber cables to the UT4 board in which the core logic circuit is implemented. To receive the optical signals of more than 15 Gbps, the protocol of the GTY will be used. The UT4 board is planned to be placed in Electronics Hut (E-Hut) located about 20 m away from the Belle II detector, where various back-end readout systems and monitoring systems are placed [39, 40]. Due to the distance between the SNAP128 chips and E-Hut and the fact that the UT4 board has only 32 GTY lanes, the electrical to optical conversion will be performed in several steps. The first conversion chips are installed in the

DOCKs (Section 2.3.3), and each one receives and serializes signals from the 12 channels of N-side chips or from 6 channels of P-side chips. In this case, 172 conversion chips are required for each side (N-side or P-side). 29 intermediate boards with FPGA will be provided to serialize all the 344 lanes of the optical signals from the first conversion chips. Each of 28 boards receives 6 N-side lanes and 6 P-side lanes, and last one receives 4 N-side lanes and 4 P-side lanes. The FPGA in the board for 6 N-side lanes and 6 P-side lanes have to process the data with the rate of about 15 Gbps, which includes not only core data of about 13 Gbps but also extra bits for the noise robustness. As mentioned above, the data transmission can be realized by the GTY protocol, whose design maximum rate is 25 Gbps. The UT4 board receives those data with 29 GTY input lanes, then makes trigger decision and output sub-trigger signal to the GRL.

7.3.2 Trigger latency

As described in Section 2.7.3, for the output of a hit signal from the D_SEFLTRG, SNAP128 requires several clocks due to the Duration Cut process. The values of the SELFTRG_UPPER and SELFTRG_TIME have not been optimized yet, however, 500 ns is considered to be sufficient [41]. The overall latency can be estimated by counting the time required for the Duration cut process in SNAP128, serialization/deserialization of signals, transmission through optical fiber cables, and the core logic processing. Serialization and deserialization require about 250 ns, respectively. The propagation of light in the fiber cable is assumed to take 5 ns per meter. In our estimation, total latency is about 2.5 μs, in which it takes 1900 ns for hit signals to reach the UT4 board, 100 ns for the core logic and 500 ns for trigger signal to reach the GRL. From this estimation, it is feasible that the TFP-SVD trigger will satisfy the fixed latency of 4.2 μs shown in Table 2.4. The GRL will perform some process such as matching of the TFP-SVD trigger and the CDC trigger after receiving the sub-trigger signals, and the GDL will output the final Level-1 trigger signal, which is send to each front-end modules of the Belle II detector. The current Level-1 trigger system, the processing of the GRL and GDL takes about 500 ns and it takes about 400–500 ns for the Level-1 trigger signal output from the GDL to reach the APV25 chips, the current front-end ASICs of the SVD. If the same latency is assumed, it takes about 1 μs for Level-1 trigger signal to reach the SNAP128 chips after GRL receiving the sub-trigger signal from the UT4 board. After all, the total trigger latency from the beam collision to the arrival of the Level-1 trigger signal at SNAP128 is about 3.5 μs, which is within the SNAP128's maximum acceptable trigger latency of 16 μs described in Section 2.7.2.

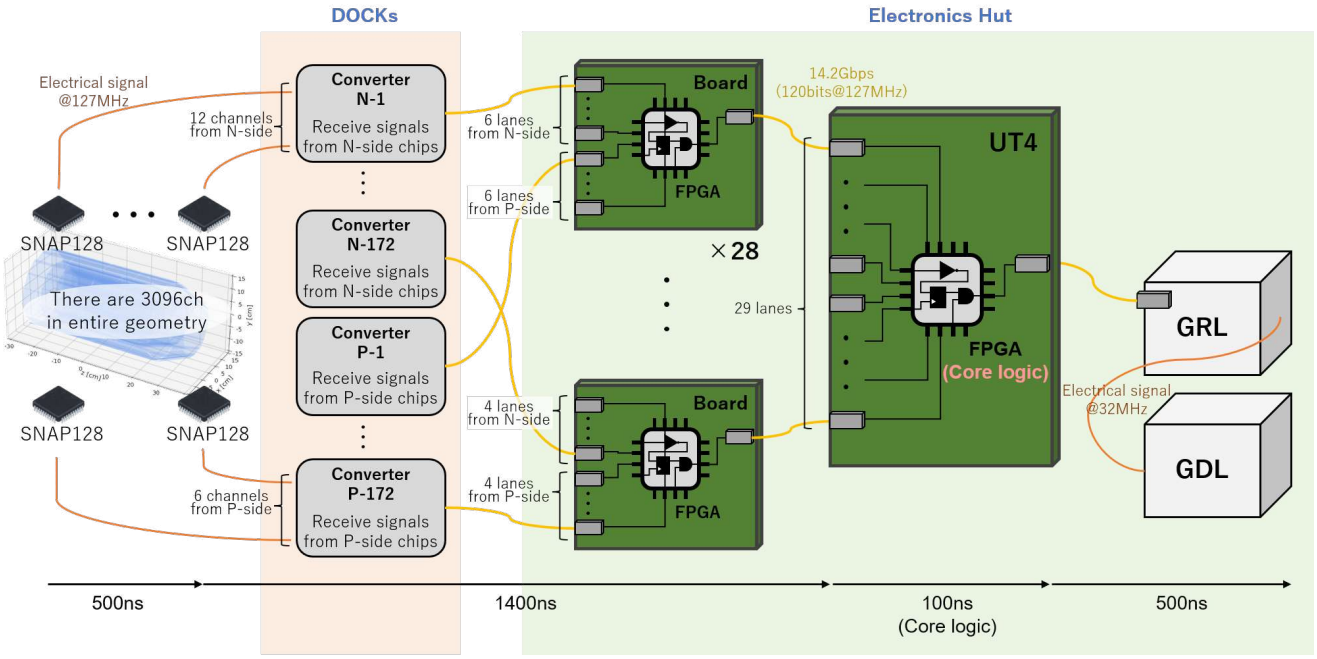

Figure 7.7: Overall setup of the firmware

7.4 Discussion

It is confirmed that the trigger condition of the Full matching and 3/4-allθ matching for the PN-128 algorithm can be implemented to the FPGA. Currently, the maximum trigger latency is limited by the SVD and KLM up to about 5 μs. Table 7.2 shows the acceptable trigger latencies for each front-end of the sub-detectors. Even after the replacement of the current SVD with the TFP-SVD, the limit will be maintained by the KLM. The estimated trigger latency of about 3.5 μs meets the limit of the maximum trigger latency.

Table 7.2: Maximum acceptable Level-1 trigger latency [42]

Sub detector	Value
PXD	5.2 μs at present (3 times larger in the future)
SVD	5.0 μs at present (about 10 μs with the TFP-SVD)
CDC	15 μs + more
TOP	9–12 μs
ARICH	10–15 μs
ECL	$>$ 15 μs
KLM	5.2 μs

In this thesis, we focused on the implementation of the PN-128 algorithm. As a next task, we must confirm the feasibility of the implementation of the PN-64 algorithm. The PN-64 algorithm has twice as many channels (3096 for PN-128, 6192 for PN-64) and ten times as large table size (88, 553 depth for PN-128, 793, 764 depth for PN-64) as the PN-128 algorithm.

Hence, while the PN-128 algorithm can be implemented in one UT4 board, the PN-64 may require additional UT boards. The trigger latency must be also checked because there is additional latency associated with the serialization, deserialization, and conversion between the electric and optical signals between UT boards. Considering the current resource usage of about 9 %, one additional subsequent UT4 board is expected to be enough. In that case, the additional latency can be estimated to be 600 ns under the same assumptions of Section 7.3.2, which can be absorbed by the gap between the current estimation of 3.5 μs and the limit of 5 μs. In addition, the next generation of the UT board, UT5, is currently under discussion. Its upgraded specification is expected to suppress the increase of the core logic latency and to accommodate more input channels and larger table size. Furthermore, the limit on the maximum trigger latency can be extended in the future by improving the readout system of sub-detectors, especially for the KLM.

The D_SELFTRG clock and SELFTRG_TIME clock in the Duration Cut process of SNAP128 have not been determined yet, which account for about 15 % of the total trigger latency of 3.5 μs. They have to be determined in terms of not only the properties of the physics and beam background particles but also the trigger latency. We will study the characteristics of beam background signals to find the optimal values for the D_SELFTRG and SELFTRG_TIME clocks.

Chapter 8

Conclusion

The Standard Model (SM) predicts almost all phenomena of elementary particle physics up to the energy scale of $\mathcal{O}(1)$ TeV, however, it is not considered to be the ultimate theory. To explore new physic laws beyond the SM, the SuperKEKB collider and the Belle II detector plan to accumulate $50\,\mathrm{ab}^{-1}$ of data in about 15 years of operation with the target luminosity of $6.0\times10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. As of June 2022, the world's highest luminosity of about $4.7\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ has already been achieved. However, as the luminosity increases, the beam background from the accelerator also increases, resulting in the higher Level-1 trigger rate. The current trigger rate have reached about 8 kHz and it is projected to exceed the limit of 30 kHz under harsh beam background environment in the future. Therefore, the Level-1 trigger system needs to be improved to remove beam background more efficiently. On the other hand, the upgrading plan of the SVD detector, TFP-SVD plan, is under discussion to enhance the background tolerance and improve the position resolution. The TFP-SVD detector is planed to be installed after the long-term shutdown of Belle II in 2027.

This thesis proposes new sub-trigger system using the TFP-SVD to efficiently remove fake CDC track triggers due to the Off-IP particles, which is expected to be major component of the beam background, and reports the performance of the developed trigger algorithm. Furthermore, the feasibility of the TFP-SVD trigger is confirmed through the implementation of the algorithm into the FPGA of the UT4 board.

Achievements

First of all, the trigger algorithm was developed and implemented in the software to evaluate the performance. With the reasonable assumption on the design of the TFP-DSSD sensor and SNAP128 chip, we considered three different trigger algorithms depending on the cell type: the N-128, PN-128, and PN-64 algorithms. Moreover, we developed the three trigger conditions: the Full, 3/4-allθ, and 3/4-selectedθ matching conditions. The Full matching condition requires the matching between online hits and the pattern table using four layers. The 3/4-allθ matching requires the matching using only three out of the four layers. The 3/4-selectedθ matching applies the matching condition using only three layers to the limited θ direction. To evaluate performance of these trigger algorithms, the trigger efficiency, particle selection area, and fake trigger probability were evaluated for the three test cases.

It was found that the Full matching trigger condition could not achieve sufficient trigger efficiency due to the existence of the sensor insensitive areas. On the other hand, the 3/4-allθ and 3/4-selectedθ matching conditions covered the areas and achieved the trigger efficiencies

around 95 % or more. For these two matching conditions, any significant differences in the trigger efficiencies were not observed among the three algorithms. Regarding the discrimination power for On-IP particles, the 3/4-selectedθ matching condition obtained narrower particle selection area than the 3/4-allθ matching condition. Regarding the fake trigger probability, more significant differences could be seen. The 3/4-selectedθ matching condition had remarkably smaller fake trigger probability than the 3/4-allθ matching condition. Furthermore, under the 3/4-selectedθ matching condition, while the N-128 algorithm showed a fake trigger probability of about 35 %, the PN-128 and PN-64 algorithms showed those of about 5 % or less. As a result, the PN-128 and PN-64 algorithms with the 3/4-selectedθ matching condition met the requirements for the particle rejection area and the fake trigger probability.

The performance of the PN-128 and PN-64 algorithms with the 3/4-selectedθ matching condition are summarized in Table 8.1. Regarding the trigger efficiency, although their values of 94.8 % and 94.2 % are slightly below the target of 95 %, they are close to the efficiency of the current CDC trigger bits. Regarding the background rejection power, as discussed in Section 6.4, by taking the matching of the TFP-SVD and CDC triggers, the trigger rate of the Total CDCTRG trigger bit is projected to be about 15 kHz at the target luminosity, which meets the limit of 20 kHz.

From these facts, these two triggers are expected to provide enough trigger efficiency and background rejection power to the Level-1 trigger system so that the DAQ will operate stably and the trigger bits for the B-physics as well as the τ and dark sector physics will be maintained in the future.

Table 8.1: Performance of the PN-128 and PN-64 algorithms under the 3/4-selectedθ matching condition

	Trigger efficiency	Particle selection area	Fake trigger probability
PN-128	94.8 %	$-3.3\,\mathrm{cm} < z < 3.3\,\mathrm{cm}$	5.6 %
PN-64	94.2 %	$-1.7\,\mathrm{cm} < z < 1.7\,\mathrm{cm}$	3.1 %

After the simulation study, we implemented the PN-128 algorithm as firmware and performed the operation test. We confirmed that the pattern table and the comparison circuits could be accommodated in the FPGA in one UT4 board and the trigger latency was estimated to meet the current requirement of 5 μs. Through these tests, we could confirm the feasibility of the TFP-SVD trigger concept.

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