# Performance of the Belle II SVD using Offline Software Reconstruction

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## Physics Motivation

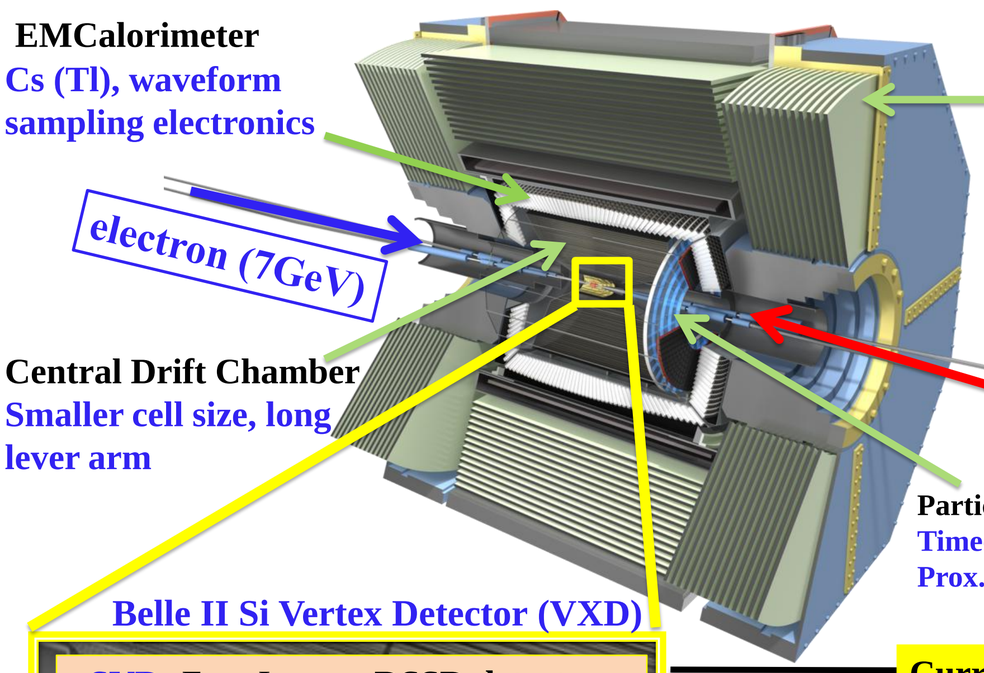
- The silicon vertex detector (SVD) is one of the important sub-detectors of the Belle II experiment at SuperKEKB.
- It consists of four-layers of double-sided silicon strip detectors (DSSDs).
- It plays a key role in the precise measurement of the decay vertex and reconstruction of the low-momentum tracks along with the pixel detector (PXD).
- The excellent performance of the Belle II SVD will provide the measurements of CP asymmetry in the B-meson system with higher precision.
- To achieve the physics goals, reconstruction of tracks with a high efficiency and a good resolution is needed.
- Design luminosity of SuperKEKB: $8\times10^{35}$ cm$^{-2}$s$^{-1}$ that would enable Belle II to collect 50 ab$^{-1}$ of data, 50 times more than its predecessor (Belle).

➡ Leads to harsh background environment in the Belle II.

- To validate the performance of the SVD, a systematic study is needed in the offline software reconstruction environment.

## Belle II Detector

**Design luminosity = $8 \times 10^{35}$ cm$^{-2}$ s$^{-1}$**
**$e^+$ (4 GeV) + $e^-$ (7 GeV) → $B\bar{B}$ at $\sqrt{s}$ =10.58 GeV [at $\Upsilon$ (4S)]**




### Current Status

**The Belle II operation in Phase 2**

- A subset of the vertex detector, comprising six layers with a single ladder per layer, installed since Spring 2018 (Phase 2) successfully joining Belle II first data taking.
- Belle II operation with the full VXD will start in Spring 2019 (Phase3)

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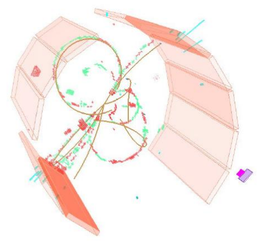
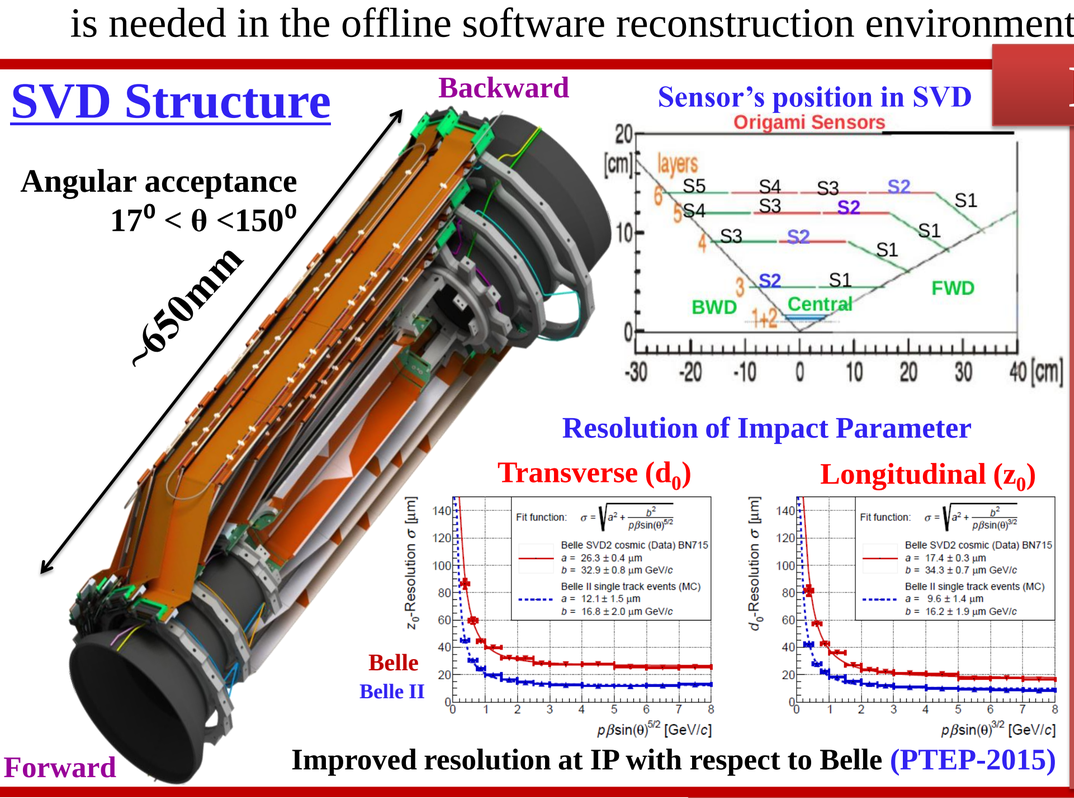


First Phase 2 collision events recorded by Belle II.

## Belle II Silicon Vertex Detector

### SVD Structure




**Sensor's position in SVD**

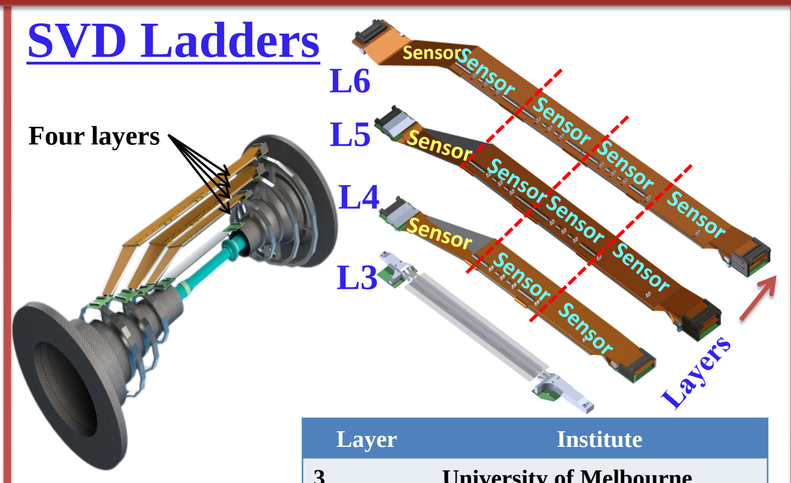



**Resolution of Impact Parameter**




**Improved resolution at IP with respect to Belle (PTEP-2015)**

### SVD Ladders

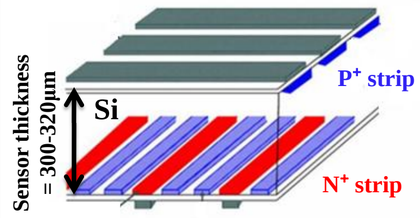



$R_{L3}$ = 39mm
$R_{L4}$ = 80mm
$R_{L5}$ = 104mm
$R_{L6}$ = 135mm

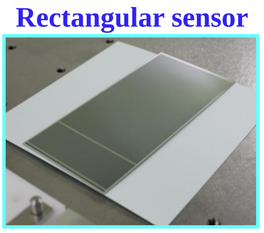
| Layer | Institute |
|---|---|
| 3 | University of Melbourne |
| 4 | TIFR Mumbai, INDIA |
| 5 | HEPHY Vienna |
| 6 | IPMU University of Tokyo |
| FW, BW | INFN Pisa |

### SVD Sensors

**Double Sided Si Strip Detector (DSSD)**




**Rectangular sensor**



| No of Strips | Rectangular | Trapezoidal |
|---|---|---|
| # of *p*-strips | 768 | 768 |
| *p*-strip pitch (μm) | 75 (L3:50) | 50…75 |
| # of *n*-strips | 512 (L3:768) | 512 |
| *n*-strip pitch (μm) | 240 (L3:160) | 240 |
| Active area (mm$^2$) | 7030 (L3:4738) | 5890 |

**Trapezoidal sensor**

**Readout (APV25)**

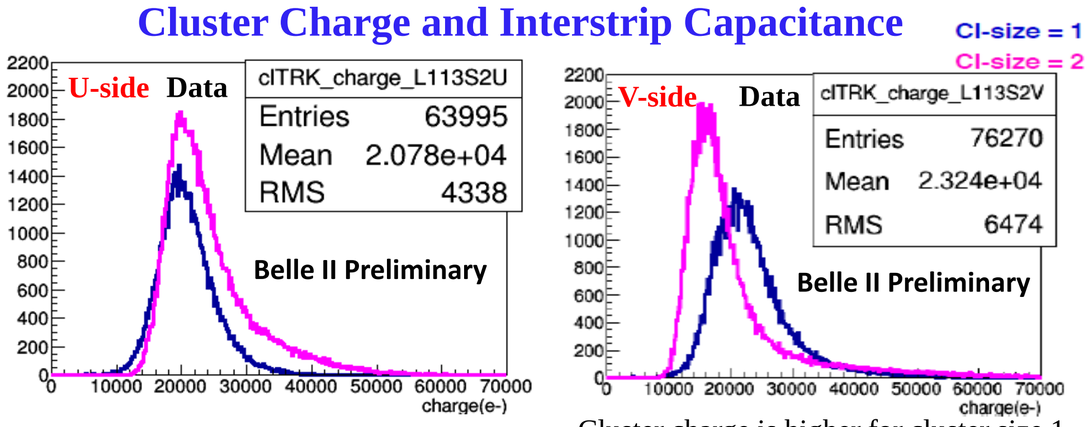
## Monte Carlo Simulation and Data Analysis

### Test Beam Data (2017) (DESY, Germany)

**Set-up: 4 GeV electron beam**
**4 SVD layers + 2 PXD layers in 1T magnetic field**

- In Belle II SVD, charge loss is significant in sensors with large pitch, as the back-side capacitance increases linearly with the implant pitch.
- This sensitivity of the cluster charge to the interstrip capacitance (Cint) can be exploited:
  - ✓To measure the actual interstrip capacitance of SVD sensors .
  - ✓ Tune this important input parameter for the full SVD simulation.
- For this measurement, comparison of test beam data and the full SVD simulation is needed.
- **Cluster charge as a function of the interstrip capacitance** is evaluated with the full SVD simulation, for the various cluster widths and compared to data to measure the Cint.

**Cluster Charge and Interstrip Capacitance**




Cluster charge is slightly higher for cluster size 2

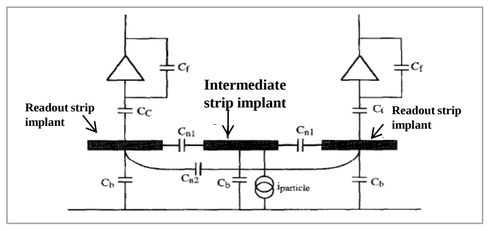
Cluster charge is higher for cluster size 1 as compared to cluster size 2

**Ratio R = $Q_{clw2}$/ $Q_{clw1}$**
$Q_{clw2}$ charge for clw2
$Q_{clw1}$ charge for clw1

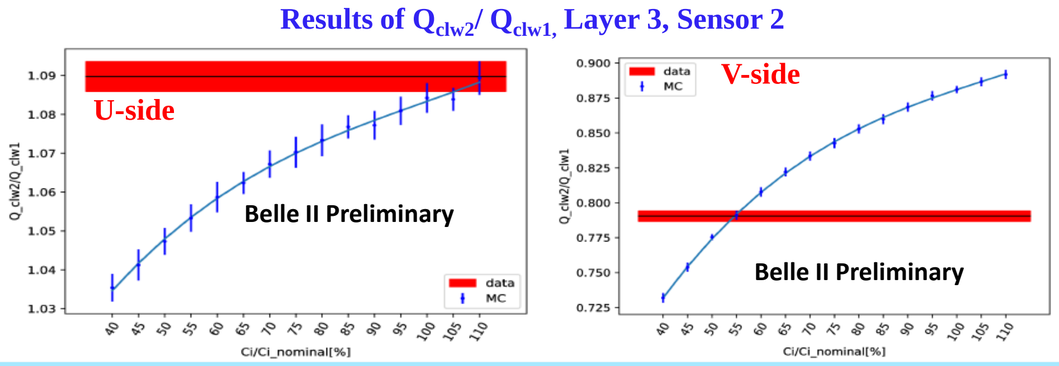
clw: cluster width

M. Krammer, H. Pernegger, NIM A 397 (1997) 232

Events: 1M (MC), ~700k (data)

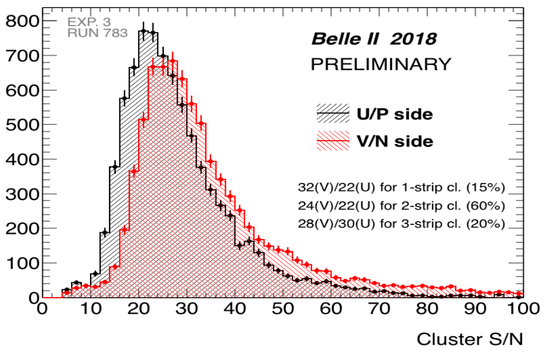



**Results of $Q_{clw2}$/ $Q_{clw1}$, Layer 3, Sensor 2**



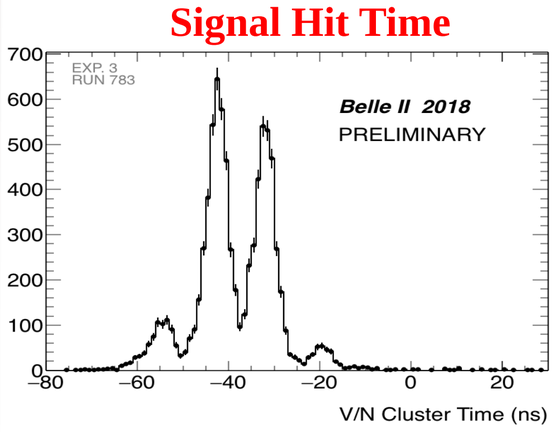

### First Data (2018) (KEK, Japan)

**Signal to Noise Ratio**




S/N greater than 20, with the N side performing slightly better than the P side, as expected.

**Signal Hit Time**




The RMS of cluster times corresponding to a bunch crossing is in the order of 3 ns, nicely matching the design.

## Summary

- Effect of the interstrip capacitance (Cint) on the cluster charge is studied in test beam data and compared with simulations to measure Cint for the different SVD layers/sensors.
- Measured S/N ratio on the first data with tracks of different momentum and inclination matches the design expectations.
- With first data, it is demonstrated that the SVD is clearly able to distinguish bunch crossings of 16 ns apart.

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