Performance studies of Thin Fine-Pitch Silicon Vertex Detector for Belle II Vertex Detector upgrade

(Belle II 崩壊点位置検出器のアップグレードに向けた挟ピッチ薄型シリコン検出器の性能の研究)

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ABSTRACT

The Belle II experiment located at KEK, Tsukuba (Japan) precisely measures the Standard Model parameters analyzing various flavor physics processes to search for new physics beyond the Standard Model. The Belle II aims to accumulate a large data set of $50\,\mathrm{ab}^{-1}$ and to make this target achievable in reasonable time scale, the KEKB collider was upgraded to SuperKEKB to reach an instantaneous luminosity of $6 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. As a part of the Belle II Vertex Detector (VXD), the Silicon Vertex Detector (SVD), which is placed close to the beam pipe, mainly contributes to vertex determination and tracking of charged particles. The Double-sided Silicon Strip Detector (DSSD) is applied in the SVD.

Accompanied by the increase of accelerator instantaneous luminosity, the large beam background degrades the performance of the SVD due to increase in the hit occupancy and radiation damage. The beam background condition of the SVD at the nominal luminosity is predicted using the Monte Carlo (MC) simulation scaled with Data/MC ratios determined by dedicated beam background studies. However, the Data/MC ratio for the luminosity background has not been determined because, using the method in previous studies, the evaluated amount of the luminosity background in the measured data showed strange dependence to the luminosity. In this thesis, a new method of the Data/MC evaluation is developed and used to give the reliable result of the luminosity background measurement on the SVD. Using the new Data/MC ratios, the projection of the SVD hit occupancy at the Belle II nominal luminosity is also updated. The projection turns out that the safety factor to the limit of the occupancy is marginal as it is only 1.9, below the desired safety margin 5.

To achieve a good performance under the high beam background level at the Belle II nominal luminosity, a new silicon strip detector, Thin and Fine-Pitch SVD (TFP-SVD), is proposed as one of the upgrade candidates of the VXD. A new DSSD, TFP-DSSD, and a new front-end ASIC, SNAP128, were developed in the TFP-SVD project. In this work, we developed a test platform dedicated for the performance evaluation of the prototype sensor and ASIC, and performed the performance characterization. In this evaluation, the basic functionality of SNAP128 is confirmed, and the power consumption and analog pulse width meets the design requirements. Also, we found two issues. The first one is that this chip gets saturated when processing the positive signal. The second one is that the noise level at the target detector capacitance is over the design limit and is about 60% larger than the simulation expectation. Based on these results, possible improvements of the design is proposed in the next version of the chip. To evaluate the performance of the sensor, we designed and assembled an integrated test board. Using this test board, the full depletion voltage, leakage current and noise of readout chip connected to the sensor is measured. The measured full depletion voltage and leakage current agree with the expectations. One remaining issue is that the noise of chip is much larger than expectation when connected to the sensor, based on the noise–detector capacitance relationship derived in the chip performance evaluation.

With a better understanding of the achievements and remaining issues in the first prototype, the design of the SNAP128 will be updated and the next version is planned to be taped out in November, 2022. For the noise issue on the sensor, hypothesis of the noise source are proposed and following experiments will follow to eliminate the possible noise sources and remeasure the noise of chips connected to the sensor. As the next step of the sensor evaluation, detector efficiency and signal charge measurement using the cosmic rays and accelerator beam is also under discussion.

Contents

Chapter 1

Introduction

The Belle II experiment is located in KEK, Tsukuba (Japan), making use of the collision data provided by the SuperKEKB accelerator. To perform high precision measurement, Belle II experiment plans to accumulate $50\,\mathrm{ab}^{-1}$ of data in about 15 years of operation. To make this target achievable in reasonable time span, the KEKB accelerator was upgraded to the SuperKEKB accelerator, aiming to achieve an instantaneous luminosity of $6 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. At the same time, as the increase of instantaneous luminosity, the beam background from the accelerator also increases and requires high background tolerance of the Belle II detector, especially the Silicon Vertex Detector (SVD) which is located close to the beam pipe.

This thesis reports two different studies related to the SVD. The first one is understanding the beam background on the SVD, and the second is the development of the upgraded silicon strip detector, the Thin Fine-Pitch SVD (TFP-SVD).

The beam background condition of the SVD at the target luminosity is predicted by the Monte Carlo (MC) simulation scaled by so-called Data/MC ratios. The Data/MC ratios are determined by the beam background studies. One big remaining issue is that the Data/MC ratio for luminosity background has not been given due to different Data/MC factors are measured under different beam injection conditions. In this thesis, a new method for Data/MC measurement is proposed and gives the first consistent measurement of Data/MC factor for luminosity background on the SVD. The beam background projection at the Belle II nominal luminosity is also updated using the new Data/MC factors. According to the projection, the existing SVD barely withstands with the high beam background, and hence there is a strong need of SVD upgrade.

Motivated by achieving better physics performance and better background tolerance at the target luminosity, various Vertex Detector (VXD) upgrade plans are proposed. One of them is the TFP-SVD upgrade plan. In this plan, a new sensor TFP-DSSD and a new front-end readout ASIC (Application-Specific Integrated Circuit) SNAP128 are introduced. In the year 2021, the prototypes of both sensor and readout ASIC were produced and delivered to KEK.

In this work, performance of these prototypes is evaluated. In particular, the noise level, power consumption and waveforms of shaper output are important properties to be confirmed with SNAP128. For the TFP-DSSD, we focus on its full depletion voltage, leakage current, noise level connected to readout chip, detector efficiency and signal charges. We developed the test platform to evaluate the performance of the prototype sensor and ASIC. For the chip, this thesis reports evaluation results of all properties mentioned above. As for the sensor, this thesis reports the measurement of full depletion voltage, leakage current and noise of chips connected to the sensor.

As the introduction of this thesis, this chapter describes the research background of the above two studies. Section 1.1 describes one of the physics motivations of the Belle II experiment. An introduction to SuperKEKB and Belle II detector is given in Section 1.2 and Section 1.3, respectively. Given that the two research subjects are closely related to the SVD, a detailed description of the SVD is given in Section 1.4. Section 1.5 focuses on the beam background conditions of SVD, including the possible detector performance degradation due to beam background and the old background projection to the target luminosity of SuperKEKB. Section 1.6 lists the possible improvements of the current SVD, which is the motivation for the SVD upgrade plans that will be mentioned in Section 1.7. In addition, the last section gives a detailed description of the concepts of upgraded SVD and how it is designed to improve the SVD performance.

The remaining chapters of this thesis is organized in the following way. Chapter 2 gives the first consistent measurement of Data/MC factor for luminosity background on SVD under different beam injection conditions. Chapter 3 focuses on the specifications of TFP-SVD, including the sensor and chip, which are necessary input in the development of evaluation platform. Chapter 4 describes performance evaluation experiment of the prototype SNAP128 ASIC, including the design and assembly of evaluation platform and the first results of the evaluation. In addition, dysfunction in the comparator inside the SNAP128 prototype is found and a simulation study follows to reveal the mechanism of the problem. After the evaluation of SNAP128 prototype, the chips are connected to the TFP-DSSD sensor to make a TFP-SVD prototype. Chapter 5 describes the design and assembly of the TFP-SVD prototype and the corresponding evaluation system. And the first evaluation results of the sensor is shown in Chapter 6. At the end of this thesis, Chapter 7 summarizes the studies reported and gives prospects of the future experiment.

1.1 Physics motivation

The Standard Model (SM) is a $SU(3) \times SU(2) \times U(1)$ gauge field theory that describes the behaviour of elementary particles. It contains the three generations of fermions, vector gauge bosons as the force carriers of electroweak and strong interactions, and scalar Higgs boson (Fig. 1.1). In the electroweak sector of the SM, the weak eigenstates of down-type quarks (d', s', b') is a linear superposition of the mass eigenstates (d, s, b):

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = V \begin{pmatrix} d \\ s \\ b \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{1.1}$$

The mixing matrix V is the so-called Cabibbo-Kobayashi-Maskawa (CKM) matrix [1, 2].

Despite its great success in describing most of the experimental results, many anomalies that cannot be explained by the SM are discovered. For example, the matter-antimatter asymmetry, the origin of the neutrino mass and the fine tuning of the Higgs mass. Further more, in latest experiment results, the measured mass of W boson is higher than the SM prediction with a significance of 7 standard deviations [3]. Now, people are searching for new physics beyond SM, especially the new physics whose energy scale is beyond TeV.

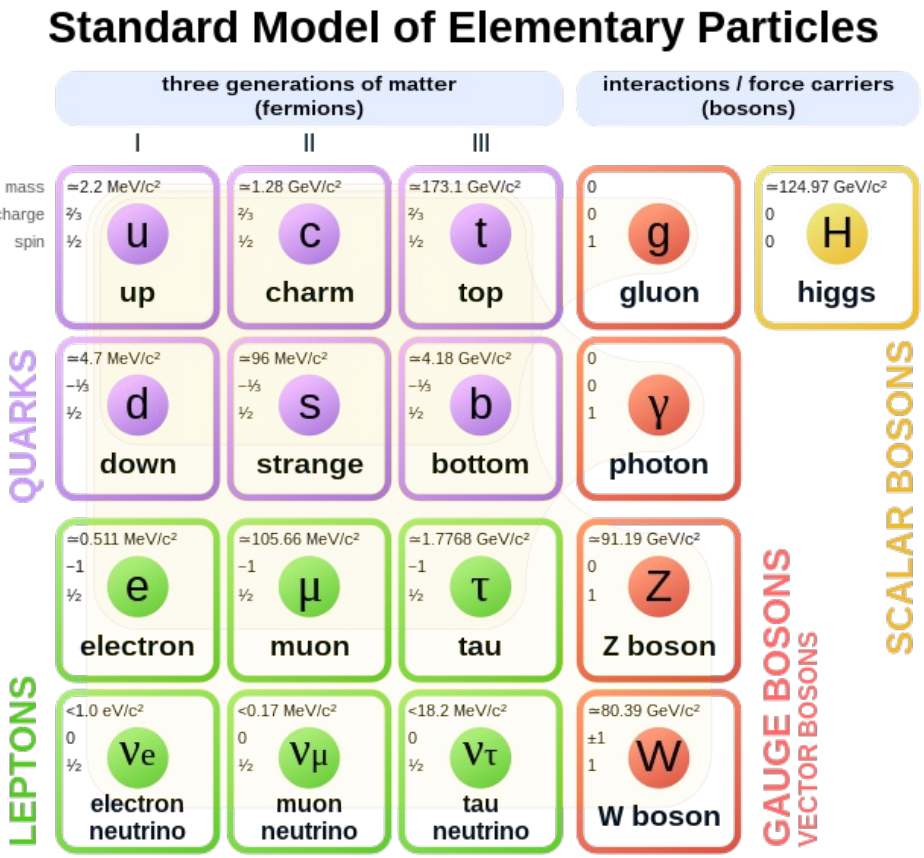


Figure 1.1: Elementary particles in standard model

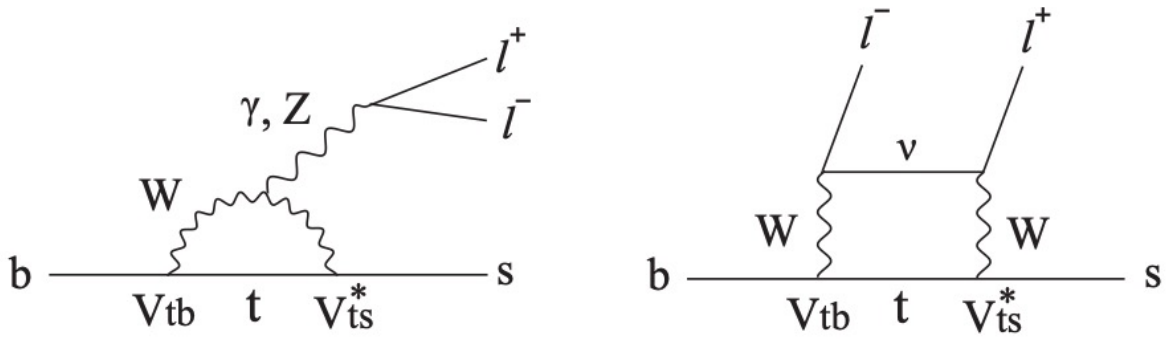


Figure 1.2: Penguin (left) and box (right) diagram of $b \to s l^+ l^-$ process in the SM.

Two different ways of searching for new physics beyond TeV scale are on-going. The first way is direct search in particle interactions at TeV scale like the ATLAS and CMS experiments on the Large Hadron Collider (LHC). The other way is indirect search by performing precise measurement of processes in lower energy scale like the b quark decay. If any deviation of measurement from the SM prediction is observed, one could declare the contributions from undiscovered new physics processes.

One example is to test the lepton flavour universality on the inclusive $B \to X_s l^+ l^-$ decay, where X_s represents any hadronic state that contains at least one s quark, by measuring the ratio of decay branching fractions when $l = \mu$ over $l = e$:

$$R_{X_s} = \frac{Br(B \to X_s \mu^+ \mu^-)}{Br(B \to X_s e^+ e^-)} \tag{1.2}$$

This observable is predicted to be close to 1 in the energy scale that lepton mass is neglectable. This measurement is sensitive to new physics since $B \to X_s l^+ l^-$ process is a $b \to s$ Flavour Changing Neutral Current (FCNC) process, whose tree level diagram is forbidden in the SM and only possible via loop (Fig. 1.2) or higher order diagrams. Recent measurement in the relative exclusive decay $B \to K l^+ l^-$ by LHCb experiment gives $R_K = 0.846^{+0.042\ +0.013}_{-0.039\ -0.012}$, indicating a 3.1σ discrepancy from the SM prediction [4]. Given this result, it is important to perform an independent measurement in the inclusive decay.

In addition to the test of lepton universality, the angular distribution of $B \to X_s l^+ l^-$ is also fruitful in searching for new physics. Generally, the $b \to s l^+ l^-$ transition in the SM is described using the following effective Hamiltonian [5]:

$$\mathcal{H}_{\text{eff}} = -\frac{4 G_f \lambda_t}{\sqrt{2}} \frac{\alpha}{4\pi} \sum_{i=7,9,10} C_i \mathcal{O}_i + h.c. \tag{1.3}$$

where C_i, $\mathcal{O}_i$ represents Wilson coefficients and effective operators. G_f, α and $\lambda_t = V_{tb} V_{ts}^*$ stand for Fermi constant, fine-structure constant and product of CKM matrix elements, respectively. $\mathcal{O}_7$ is the electromagnetic operator that contributes via the penguin process. $\mathcal{O}_9$ and $\mathcal{O}_{10}$ represent contributions from lepton vector and axial vector current. These operators

are written as:

$$\begin{aligned}
\mathcal{O}_7 &= \frac{e}{16\pi^2}\,\bar{s}\sigma_{\mu\nu}\left(m_s P_L + m_b P_R\right) b F^{\mu\nu}, \\
\mathcal{O}_9 &= \frac{e}{16\pi^2}\left(\bar{s}\gamma^\mu P_L b\right)\left(\bar{\ell}\gamma_\mu \ell\right), \\
\mathcal{O}_{10} &= \frac{e}{16\pi^2}\left(\bar{s}\gamma^\mu P_L b\right)\left(\bar{\ell}\gamma_\mu \gamma_5 \ell\right),
\end{aligned} \tag{1.4}$$

where e is the coupling constant of electromagnetic interaction. P_L and P_R are left-hand and right-hand operators $(1-\gamma_5)/2$ and $(1+\gamma_5)/2$. $F_{\mu\nu}$ is the electromagnetic field tensor.

Besides the inclusive branching fraction measurement, which is sensitive to the absolute value of C_7, C_9 and C_{10}, the forward-backward asymmetry (A_{FB}) measurement of $B \to X_s l^+ l^-$ decay also draws attention because it is sensitive to the interference between vector lepton current ($\mathcal{O}_9$) and axial vector lepton current ($\mathcal{O}_{10}$) by its dependence on $\Re(C_9 C_{10})$ [5]. The forward-backward asymmetry is defined to be

$$A_{FB} = \frac{N(\cos\theta > 0) - N(\cos\theta < 0)}{N(\cos\theta > 0) + N(\cos\theta < 0)} \tag{1.5}$$

where θ refers to the angle between B and l^+ momenta in the dilepton center-of-mass reference. If TeV scale particles like heavy leptoquark [6] contribute, the relevant Wilson coefficients deviate from the the SM prediction:

$$C_i = C_i^{\mathrm{SM}} + C_i^{\mathrm{NP}} \tag{1.6}$$

where C^{SM} is the contribution from the SM while C^{NP} represents the contribution from new physics.

Precise measurement of inclusive $B \to X_s l^+ l^-$ decay requires high statistics and low background environment provided by the collider, as well as a hermetic detector with high momentum resolution and high lepton identification efficiency. The only experiment that is still in operation and satisfies all these requirements is the Belle II experiment making use of the data provided by SuperKEKB accelerator. In particular, the SVD contributes to this analysis by providing vertex information to help rejecting continuum background ($q\bar{q}$ events).

1.2 SuperKEKB

The SuperKEKB [7] (Fig. 1.3) is an electron-positron collider with the center-of-mass energy $\sqrt{s}$ set to the $\Upsilon(4S)$ resonance. The $\Upsilon(4S)$ mesons subsequently decay into $B\bar{B}$ pairs which can be used to study B meson decays.

A schematic drawing of SuperKEKB is shown in Fig. 1.3. It consists of a linear accelerator (LINAC), positron damping ring and main storage rings. The LINAC accelerates electrons and positrons up to the designed energies. In addition, the positrons are also generated inside LINAC by shooting electron beams into a tungsten target. The accelerated beams are injected into two main storage rings, High Energy Ring (HER) and Low Energy Ring (LER). The damping ring nearby the LINAC is to reduce the emittance of positron beam before injecting it into the storage ring. The Belle II detector is located at the crossing point of the two storage rings where the two beams collide. The electron beam has 7 GeV and is circulated in the HER, while the positron beam has 4 GeV and is circulated in the LER. This asymmetric beam energy results in the Lorentz boost of the e^+e^- center-of-mass system with $\beta\gamma = 0.28$, which offers the indirect CP violation measurement in the Belle II experiment.

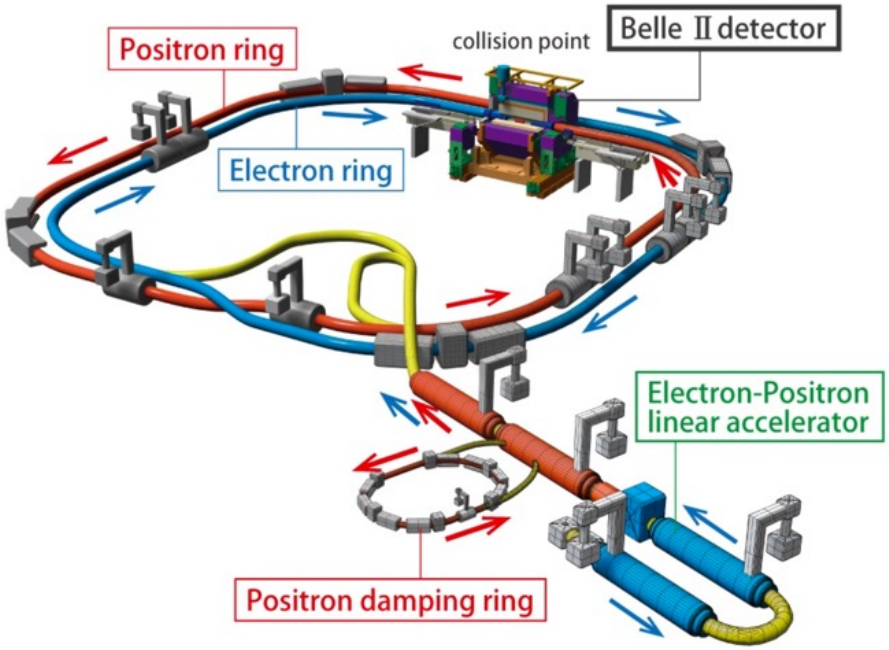


Figure 1.3: The schematic drawing of the SuperKEKB

The beams are injected into the main storage ring from the Beam Transport (BT), which is the yellow pipe in Fig. 1.3. There are two different injection modes: "normal injection" and "continuous injection", with the former one used to accumulate the beam current fast with Belle II High Voltage (HV) off, while the latter one used when Belle II is taking data with HV on. Usually, beam current is kept during continuous injection, thus it is also called "top-up injection".

To perform high precision physics measurement, Belle II experiment plans to accumulate $50\,\mathrm{ab}^{-1}$ of data in total. To make this target achievable in reasonable time span, the KEKB accelerator was upgraded to the SuperKEKB accelerator, aiming to achieve an instantaneous luminosity of $6 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The benchmark luminosity in the future is $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. To achieve the instantaneous luminosity goal, the so-called "nano-beam" scheme [8] is applied in the SuperKEKB. The instantaneous luminosity L of the e^+e^- collider at the beam-beam limit collider is proportional to the following components:

$$L \propto \gamma_{\pm} \frac{I_{\pm}\xi_{y\pm}}{\beta_y^*} \tag{1.7}$$

where (+) and (-) stands for positrons and electrons. γ is the Lorentz factor. I is the beam current. ξ_y represents the beam-beam effect in vertical direction. β_y^* is the vertical beta function at the collision point. From this formula, increasing the beam current and squeezing the vertical beta function at collision point are effective methods to increase collision luminosity. For this reason, in the upgrade of KEKB to SuperKEKB, the beam current of LER and HER are increased from 1.6 A to 2.8 A and from 1.2A to 2.0 A, respectively. And the β_y^* decreases from 5.9 mm to about 0.3 mm. As the beam size at the collision point is squeezed, the beam

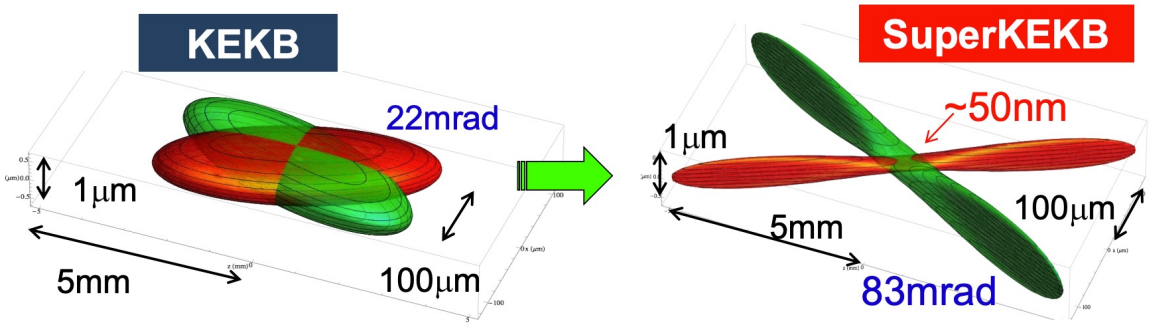


Figure 1.4: Beam pattern at the collision point for KEKB (left) and SuperKEKB (right). Compared with KEKB, in nano-beam scheme of SuperKEKB, the beams are squeezed to a much smaller size at the collision point and the crossing angle of two beams are much larger to reduce the overlap region of two beams [9].

Beam parameters	KEKB achieved	SuperKEKB target
$\beta^*_{\rm y}$(LER/HER)[mm]	5.9/5.9	0.27/0.3
$\beta^*_{\rm x}$(LER/HER)[mm]	1200/1200	32/25
I(LER/HER)[A]	1.64/1.19	2.80/2.00
number of bunches	1584	1761
θ [mrad]	22	83
$L\left[\times 10^{35}\ {\rm cm}^{-2}\ {\rm s}^{-1}\right]$	0.21	6

Table 1.1: Beam parameters achieved by KEKB (left) and the target parameters of SuperKEKB (right). The $\beta^*_{x(y)}$ is the beta function in horizontal (vertical) direction at the collision point. I is beam current. θ is the crossing angle of LER and HER beams. L is instantaneous luminosity.

size before and after the collision point steeply expands. This phenomenon is called "Hourglass effect". In the head-on collision scheme applied in KEKB, the beam-beam effect happens in the overlapped expanded part of the beams enlarges beam emittance while not contributing much to the luminosity. In the nano-beam scheme, in addition to squeezing the beam at collision point, the two beams forms a relative large crossing angle, reducing the length of overlap region and could avoid the beam collision in the expanded area as shown in Fig. 1.4. The beam parameters achieved by KEKB and the target parameters of SuperKEKB is shown in Table 1.1. The projected luminosity of SuperKEKB is shown in Fig. 1.5. By the year 2034, SuperKEKB is expected to reach the target luminosity $6.0 \times 10^{35}\,{\rm cm}^{-2}\,{\rm s}^{-1}$.

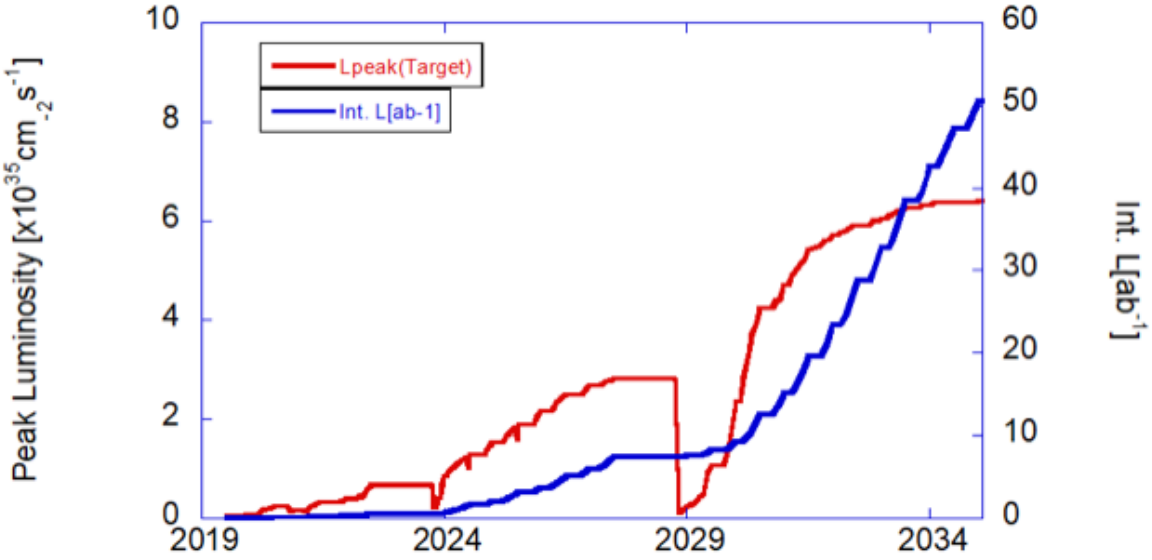


Figure 1.5: Luminosity projection of SuperKEKB [10]

1.3 Belle II detector

The Belle II detector [11] is a general purpose detector which consists of 7 sub-detectors surrounding the Interaction Point (IP). A schematic drawing of Belle II detector is shown in Fig. 1.6. Starting with the innermost to outside, there are the Vertex Detector (VXD) system, consisting of Pixel Detector (PXD) and Silicon Vertex Detector (SVD), Central Drift Chamber (CDC), Time of Propagation counter (TOP), Aerogel Ring Imaging Cherenkov counter (ARICH), Electromagnetic Calorimeter (ECL), and K_L^0 and μ detector (KLM). A super-conductor solenoid is placed between ECL and KLM, generating a 1.5 T magnetic field along the Z axis (see definition below) , which bends the trajectory of charged particles for momentum measurement.

The global coordinate system of Belle II is shown in Fig. 1.7. The origin point is defined to be the nominal interaction point. The Z axis is along the bisector of the angle between the LER and HER beam pipe in the horizontal plane. The X axis is in the horizontal plane and points outside of the main storage ring. The Y axis is vertical and points upwards. The X-Y-Z axises forms a right-handed Cartesius coordinate system. The forward direction is defined to be along the Z axis direction and backward direction is defined to be against the Z axis direction. In addition, in this thesis, the radius r is defined to be $\sqrt{x^2+y^2}$, the polar angle $\theta = \arccos(z/\sqrt{x^2+y^2+z^2})$ and azimuth angle ϕ is defined to be $\arctan(y/x)$.

The Belle II detector covers a polar angle interval of $17° < \theta < 150°$. Due to the asymmetrical energy of the beams, the system of the produced particles is boosted to the forward direction, thus Belle II is designed to have a larger geometry acceptance in the forward direction.

The VXD (Fig. 1.8) is placed closest to the IP. It is a 6 layer silicon detector, with the inner two layers being the PXD and the outer four layers being the SVD, mainly contributing to vertex detection and tracking of charged particles. The vertex resolution of VXD is

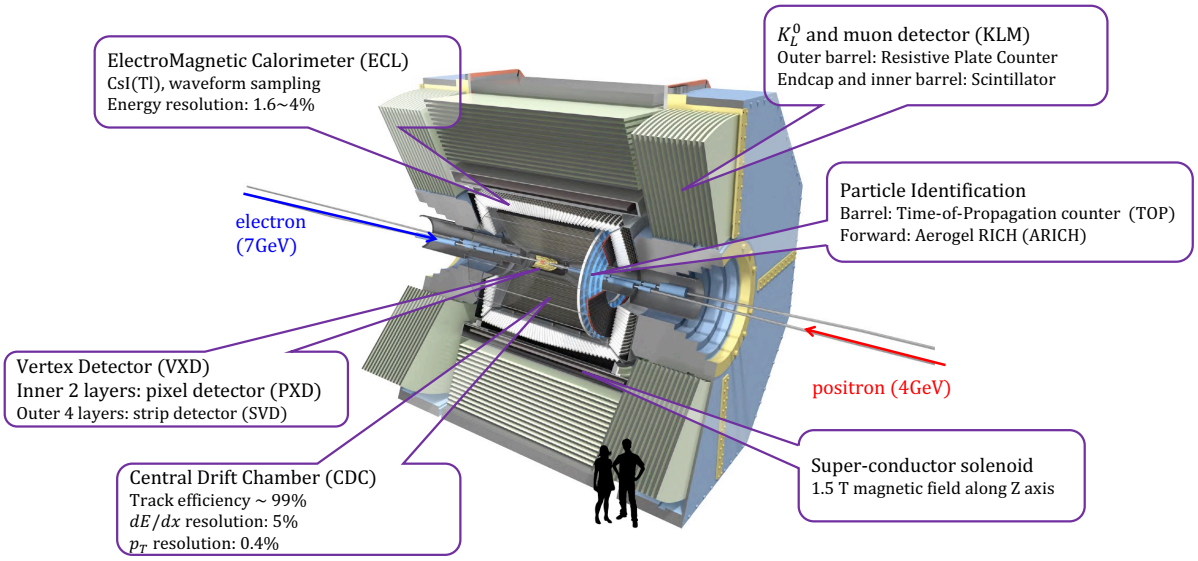


Figure 1.6: Schematic drawing of Belle II detector.

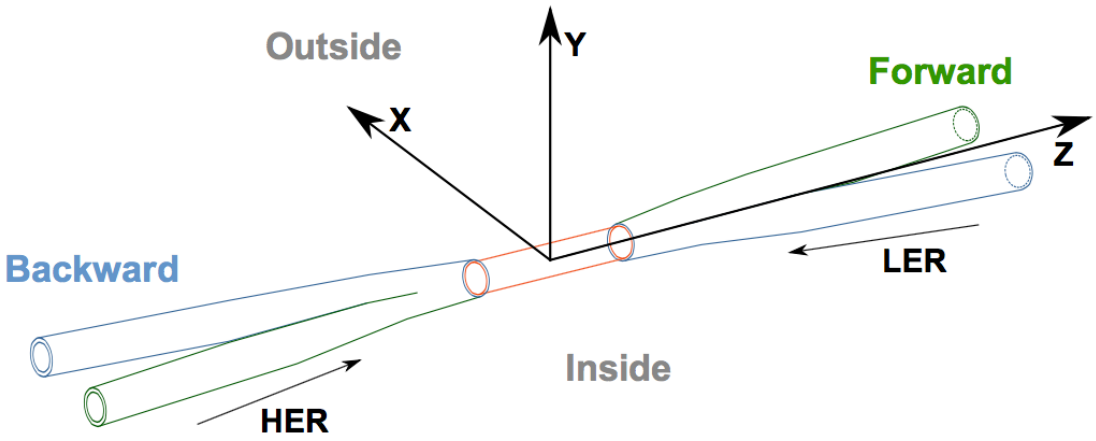


Figure 1.7: The global coordinate system of Belle II

about 15 µm.

The PXD makes use of the DEpleted P-channel Field Effect Transistor (DEPFET) [12] technology. To detect the B meson decay vertex at a resolution of $O(10$ um), the inner most layer of the PXD is placed only 14 mm away from the IP, with the pixel size being fine to 50×50 um^2.

The SVD is a silicon strip detector which is located outside the PXD, to be described in detail in Section 1.4.

The CDC is a drift chamber located outside the VXD. It has 14,336 sense wires and is the main tracking detector. There are two kind of wires in the CDC: axial wire and stereo wire.

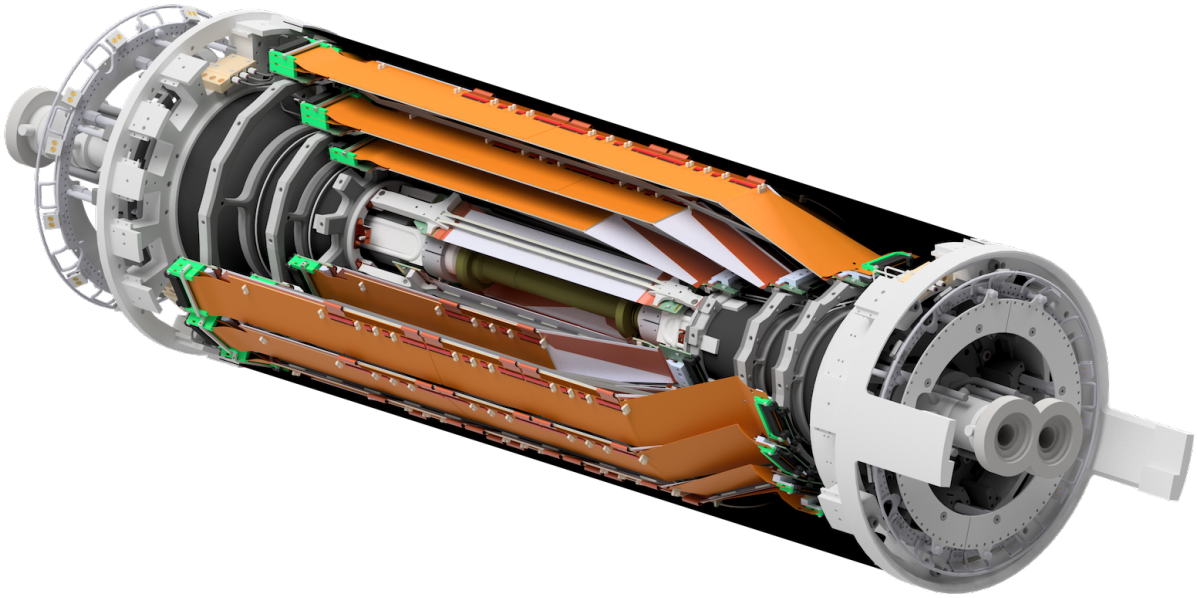


Figure 1.8: Belle II Vertex Detector (VXD)

Axial wire is along the Z axis, contributing to the 2 dimensional tracking in X-Y plane, while stereo wire is at a small angle with the Z axis, enabling the CDC to do 3 dimensional tracking. The tracking efficiency of CDC is up to 99% and with the 1.5 T magnetic field generated by the solenoid the resolution of transverse momentum p_T in CDC is 0.4%. The CDC hit information is the most important input for the Belle II tracking trigger algorithm. In the meantime, the CDC also participates in the particle identification (PID) system using the ionization energy loss (dE/dx) information of charged particles, with a good dE/dx resolution down to 5%. The PID of the CDC is particularly important for low-momentum particles that are hard to reach the TOP and ARICH, which are the particle identification detectors outside the CDC.

The TOP and ARICH are mainly responsible for identifying $K^{\pm}$ and $\pi^{\pm}$ particles. TOP uses quartz as the radiator and detect Cherenkov photons using Micro-Channel Plate (MCP) PMTs. ARICH uses the silica aerogel as the radiator and detect the Cherenkov photons using Hybrid Avalanche Photon Detector (HAPD).

The ECL is a collection of CsI(Tl) scintillation crystal detectors which detect the scintillation photons with the PIN photo-diodes. It measures energies and positions of electrons and photons. In addition, it also provides the PID information and measures luminosity by detecting electrons scattered via the Bhabha process.

The KLM is placed at outer most of the whole Belle II detector and detects K_L^0 and μ. The end-cap sections have a sandwich structure of 14 iron plates and 14 plastic scintillator layers. The barrel part has 14 iron plates and 15 Resistive Plate Chambers (RPC) and scintillator layers. Muons are detected from the combination of the CDC tracks and KLM hits, while K_L^0 only have clusters within KLM.

In Belle II, the trigger system have inputs from the CDC, ECL, TOP and KLM and outputs the trigger signal via the global decision logic (GDL)[13]. The bandwidth limit on the data acquisition (DAQ) system requires the total trigger rate below 30 kHz.

1.4 Silicon Vertex Detector (SVD)

The SVD [14] contributes to tracking, decay vertex reconstruction, and particle identification via energy loss measurements. The Silicon strip detector features in its small strip pitch and thus is able to provide high-resolution position detection. On the other hand, the material budget of the SVD is required to be as small as possible to minimize the multiple scattering process, which is the main source of uncertainties in the track reconstruction. For these reasons, the Double-sided Silicon-Strip Detector (DSSD) technology and APV25 front-end ASIC are applied in the SVD.

1.4.1 Double-sided Silicon-Strip Detector (DSSD)

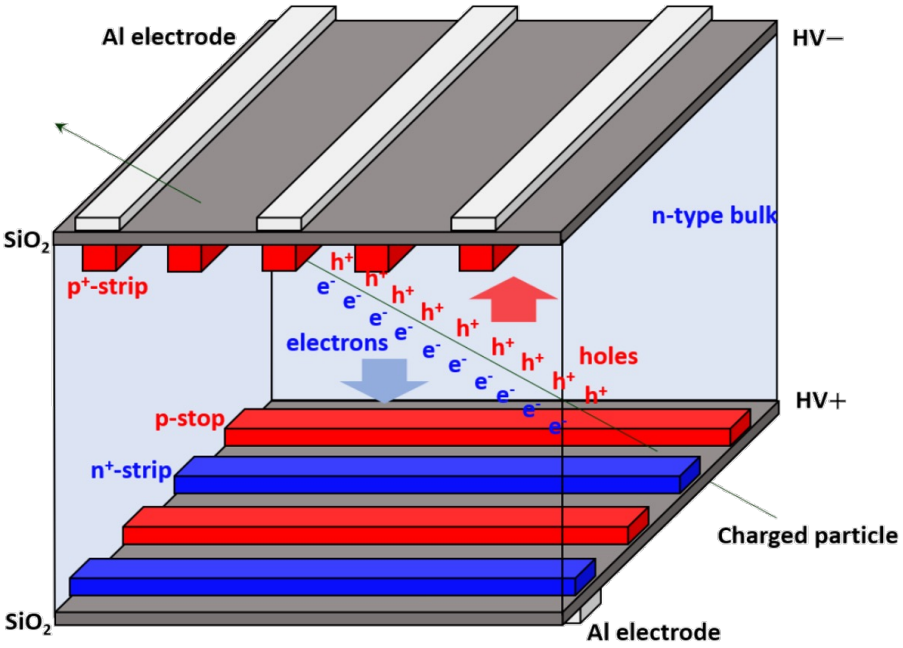


Figure 1.9: Structure of DSSD. p^+-strip and n^+-strip are more deeply doped compared with n-type bulk.

Figure 1.9 shows the structure of a DSSD, in which readout strips on two sides of one silicon bulk are placed perpendicular to each other, enabling the SVD to readout 2-dimensional information using a single silicon sensor. Inverse bias voltage of 100 V is applied between the p^+-strips and n^+-strips, under which the bulk is fully depleted. When charged particles pass through the DSSD, electron-hole pairs are created and drifted to n^+-strip and p^+-strip respectively along with the electrical field created by inverse bias voltage. The electric signals are read out via aluminum electrodes that are AC coupled to the n^+ and p^+ strips. In order to improve the spacial resolution, floating strips are placed between every two readout strips. The charge collected by these floating strips is read out by the neighboring readout strips and the effective strip pitch is reduced to half of readout pitch. The silicon oxide contains fixed

	Small rectangular	Large rectangular	Trapezoidal
Location	Layer 3	Layer 4–6 (except FW)	Layer 4–6 (FW)
Readout strips P-side	768	768	768
Readout strips N-side	768	512	512
Readout pitch P-side	50 μm	75 μm	$50 - 75$ μm
Readout pitch N-side	160 μm	240 μm	240 μm
Sensor active area [mm^2]	122.90×38.55	122.90×57.72	$122.76 \times (38.42 - 57.59)$
Sensor thickness	320 μm	320 μm	300 μm
Manufacturer	Hamamatsu	Hamamatsu	Micron

Table 1.2: Specifications of the DSSD sensor used in the SVD.

positive oxide charges, which attract electrons in the n-type bulk and strips and thus create a conductive layer in the silicon, shorting all n-type doped areas. For this reason, p-type stop strips (p-stop) are placed between every two adjacent n^+-strips in order to prevent the divergence of collected charges on each strip and suppress the noise level. The specifications of the DSSD sensors applied in the SVD is summarized in Table 1.2. The thickness of the DSSD is 300 µm and 320 µm, with a material budget corresponding to approximately 0.4% of radiation length X_0.

The cluster charge (defined in Section 1.4.4) is regarded as the signal charge generated inside DSSD when a charged particle pass through. Distribution of cluster charge of sensors located in Layer 3, BW (see Section 1.4.3) in real operation is shown in Fig. 1.10, with the sensor thickness being 320 µm. The most probable value for cluster charge is about 21,000 electrons on P side and 18,600 electrons on N side.

1.4.2 Front-end readout ASIC: APV25

The signals generated by the DSSD is read out by the front-end ASIC, APV25 [15, 16]. It is a low-noise fast-speed charge sensitive amplifier chip made by the 250 nm CMOS technology. It is also known to be strong against irradiation damage and past irradiation experiment shows that APV25 can work properly after 100 Mrad of total ionizing does [17].

The block diagram of one analog channel in APV25 is shown in Fig. 1.11. For each channel, a pre-amplifier and a shaper are implemented to amplify and shape the signals from the sensor. There is an optional inverter, which is used to change the polarity of shaper input in order to process both positive and negative signals from the P side and N side of DSSD. The shaper output for negative signal is shown in Fig. 1.12. The pulse width at 1/4 pulse height is about 200 ns.

The shaper output is written to a capacitor array pipeline of 192 cells at a clock frequency of 31.8 MHz. For each cell, the write-in switch is connected to the shaper output bus and the read-out switch is connected to input bus of circuit afterwards, recording the voltage of shaper output in one clock period. A FIFO with a depth of 32 is implemented to record the cell addresses that are requested for output by the trigger signals. The labeled cells are skipped in the write cycle until they are read out. The shortest period of one write loop in the pipeline when 32 cells are labeled is $(192 - 32) \times$ clock period $= 5.0$ µs, which is also the maximum acceptable level-1 trigger latency. An analog pulse shape processor (APSP) is placed at the output of pipeline which is a switched capacitor filter matrix that has two different modes: the

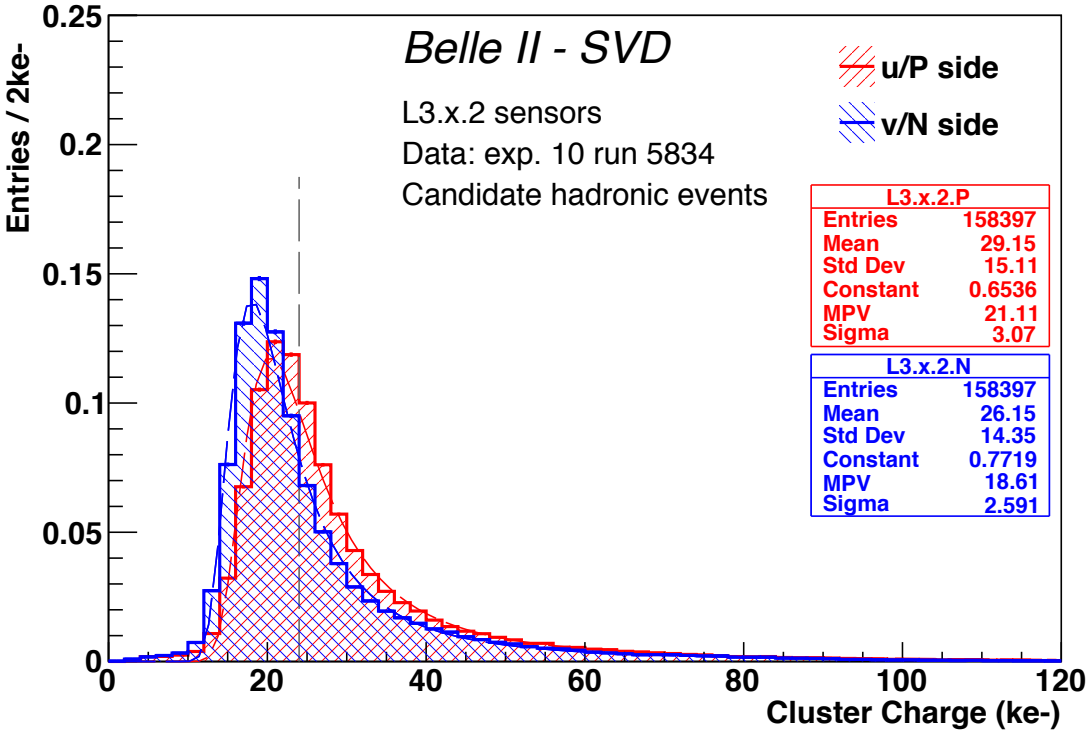


Figure 1.10: Cluster charge of SVD sensors located in Layer 3, BW. The red and blue histograms corresponds to the cluster charge on P and N side, respectively.

deconvolution mode and the pass-on mode (also called "peak mode" in reference[15]). In the SVD application, only pass-on mode is used, in which the data read out from the pipeline is passed on directly to the Multiplexer (MUX) stage.

In the real operation, to fully reconstruct the shaper output, three or six cells of data are read out in one event. These two data taking modes are called "3-sample" mode and "6-sample" mode, respectively. This multi-sample readout allows to reconstruct both peak amplitude and hit time, which is crucial in rejecting off-time backgrounds by applying the hit-time cut. Initially, the SVD only operates in 6-sample mode, but a mixed 3/6 operation is under discussion to save both bandwidth and dead time at high luminosity operation.

The output of APV25 is shown in Fig. 1.13. Each output frame contains a 12-bit digital header (3-bit header, 8-bit readout cell address and 1-bit error flag) and the analog data of the 128 channel inputs. The APV25 output is digitized by 10-bit Flashing Analog-to-Digital Converters (FADC) in the downstream of APV25 and sent to back-end devices for further reconstruction and archiving.

The Equivalent Noise Charge (ENC) of one channel in APV25 is $(270 + 38 \times C/\mathrm{pF})\ e^-$ [18], where C represents the detector capacitance, referring to the capacitance between input pad of two adjacent channels on the chip. In the SVD, the chips are placed on a flexible circuit board on top of the sensors to reduce the length of electrical patterns between the readout strip on sensor and APV25 analog input. This is the so called "chip-on-sensor" concept. With

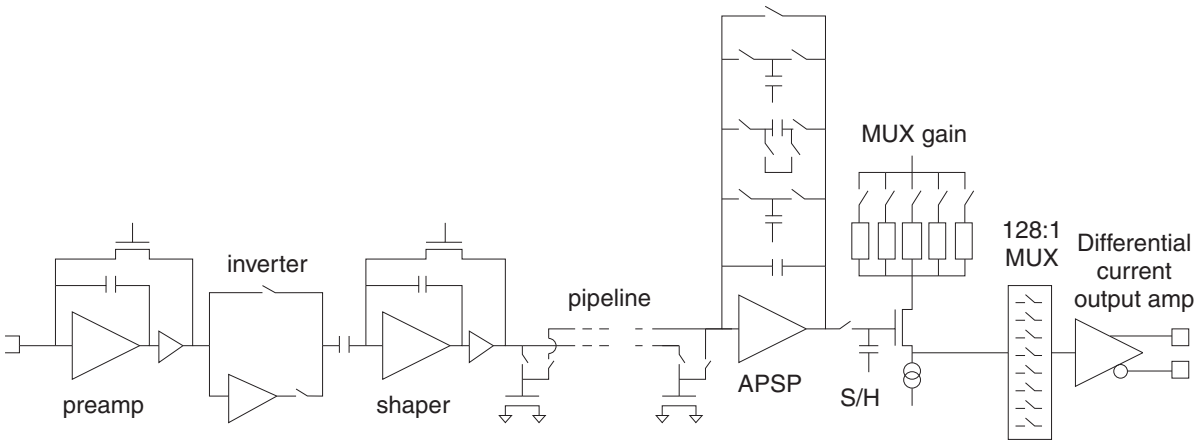


Figure 1.11: Block diagram of one channel in APV25 front-end readout chip

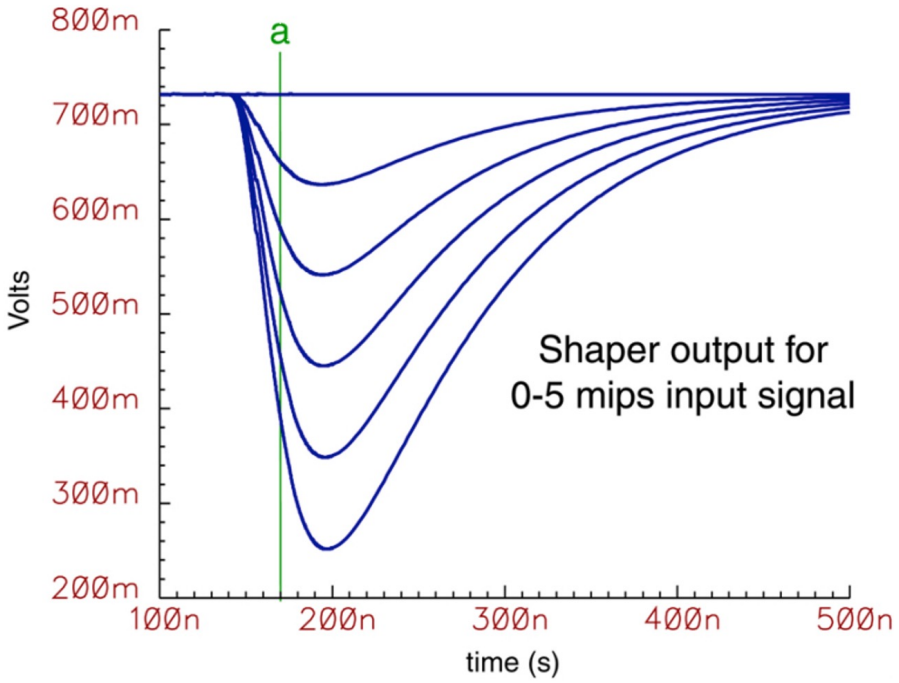


Figure 1.12: Shaper output of APV25 at different signal input. 1 mip = 24,000 input electrons. [15]

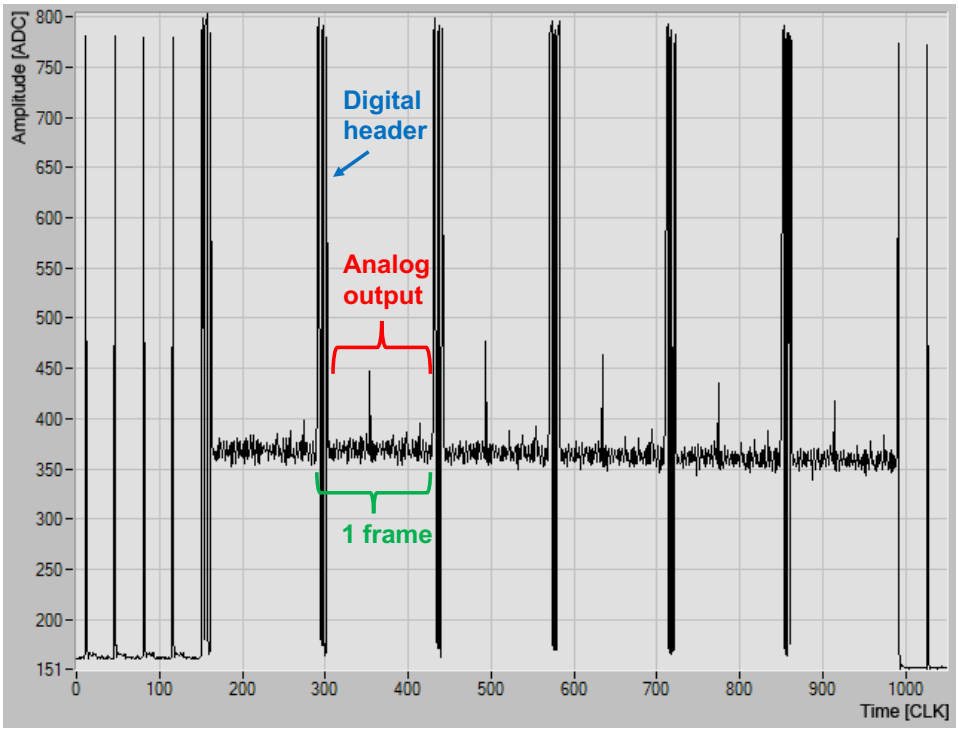


Figure 1.13: APV25 output digitized by the flash ADC chips.

this concept, detector capacitance is dominated by the inter-strip capacitance of the sensor. After connected to the sensor, the measured APV25 noise level is no larger than 1000 e^-, guaranteeing a good signal to noise ratio (S/N) on each strip.

1.4.3 Structure of the SVD

The SVD is the outer 4 layers of the VXD, named as Layer3–6, placed at 39 mm, 80 mm, 104 mm and 135 mm from the Z axis, respectively. The material budget of one layer corresponds to about $0.7\%X_0$. Each SVD layer contains 7–16 ladders and each ladder is composed of 2–5 DSSD sensors. The structure of layer and ladders of the SVD is shown in Fig. 1.14. Ladders are numbered anticlockwise viewing toward the -Z direction. Figure 1.15 shows the sensor position in the r-Z plane. The sensors are named as BW, -Z, CE, +Z and FW according to their Z position. In total, 172 sensors are installed in the SVD.

1.4.4 Hit information reconstruction

In each event, 3 or 6 samples of shaper waveform are read out from each channel of APV25. After online and offline selections, the digitized shaper waveform samples are used to reconstruct the SVD hits, which includes the information of 3 dimensional position, hit time and ionization charge generated inside SVD. With these information, the tracking of charged particles and the particle identification is performed afterwards.

The online selection is the zero-suppression performed in FADC. In this process, only the strips with at least one sample above 3 times of the noise is kept. The noise of each channel is pre-measured before physics run and pre-loaded in the FADC.

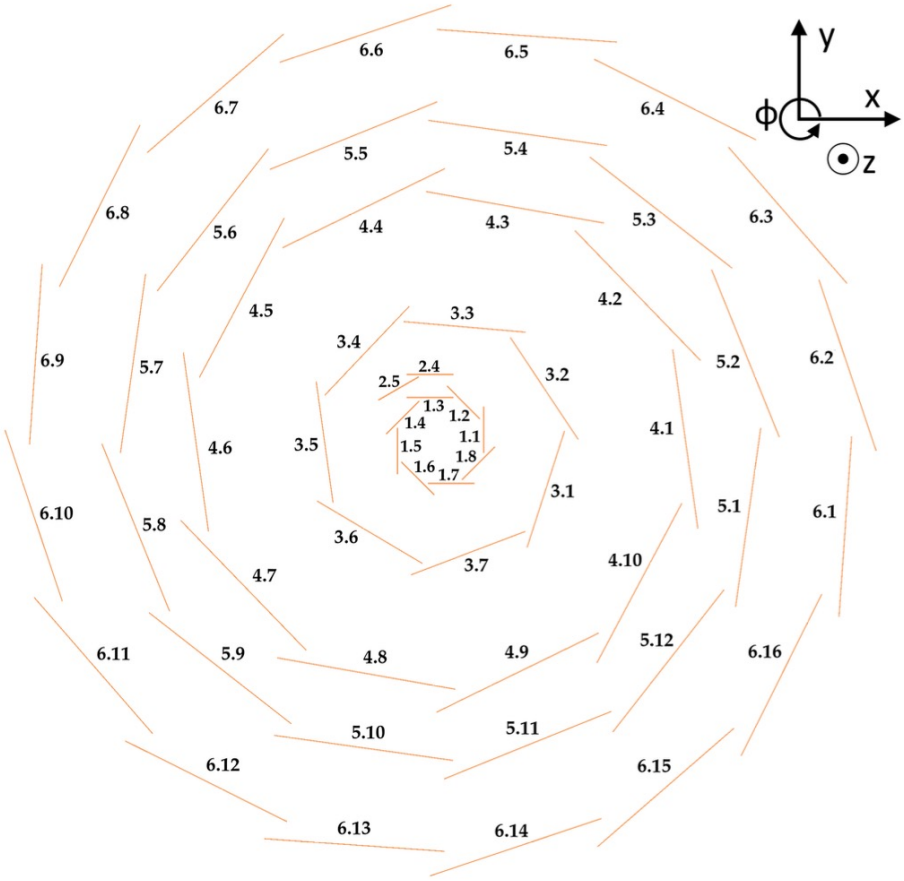


Figure 1.14: Structure of the VXD in X-Y plane. The outer 4 layers (Layer 3–6) are the SVD while the inner two layers (Layer 1–2) are the PXD.

The offline selection follows to reconstruct the clusters and calculate the hit position, hit time and ionization charge. A group of adjacent strips is regarded as a cluster if at least one strip (called seed strip) has Signal-to-Noise ratio (S/N) > 5 and the other strips have S/N $>$ 3. The number of strips within one cluster is called cluster size. Given the high S/N of DSSD and APV25, these requirements is loose enough to satisfy excellent hit efficiency of more than 99% and good hit position resolution. The signal charge collected by each strip is calculated using the pulse height - input charge relationship measured in advance, with the highest sample regarded as the pulse height. The cluster charge is defined to be the sum of signal charge of each strip in the same cluster.

In this thesis, the SVD occupancy is defined to be the fraction of fired strips in one sensor in one event, with the fired strip defined to be a strip with S/N > 5. Simulation study shows that with an occupancy of about 5%, the SVD tracking efficiency is 91% and fake rate is 17% [19], closing to the 90% track efficiency and 20% fake rate limit. For this reason, the hit occupancy limit of the SVD is set to be 5%.

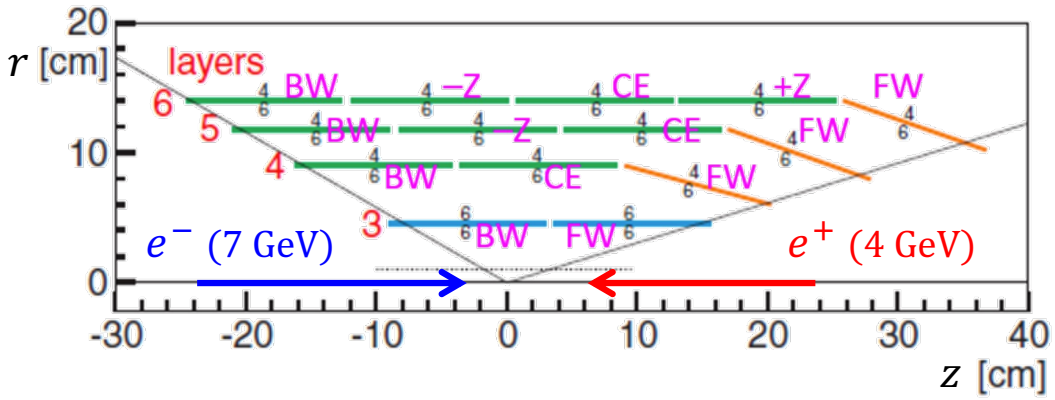


Figure 1.15: SVD DSSD sensor locations in the r-Z plane.

1.5 Beam background conditions of the SVD

1.5.1 Possible detector performance degradation due to beam background

In the SVD, the beam background increases the hit occupancy which degrades tracking performance of the SVD and takes up the precious bandwidth for data transmission in the DAQ system. At the same time, the background also leaves radiation damage on the sensors that can increase the leakage current, strip noise, and change the full depletion voltage of sensors.

Radiation effects are evaluated using the total ionizing dose (TID) and the non-ionizing energy loss (NIEL) on the sensor. The latter one is described using the 1-MeV neutron equivalent fluence. Radiation effects damages both surface and bulk of one sensor. Damage on the surface increases surface leakage current and then raises the strip noise. NIEL causes bulk displacement and increases the bulk leakage current. It also modifies the effective doping concentration and changes the full depletion voltage (Fig. 1.17). Currently, the noise in the SVD is dominated by the contribution from detector capacitance, while the leakage current originated noise suppressed by the relative short shaping time of APV25. In the long time range operation, the noise from bulk leakage current could be comparable with that from detector capacitance.

The most restrictive limit on the SVD beam background comes from the tracking performance degradation, which requires the hit occupancy of the SVD innermost layer (Layer 3) to be less than 5% [19]. Current extrapolation shows that after about 6 Mrad of TID, corresponding to about 1.4×10^{13} neq/cm^2 of 1-MeV neutron equivalent fluence, a significant reduction in S/N is expected [20]. At this level radiation level, the noise would increase by about 40% due to the noise contribution from bulk leakage current becoming comparable with that from detector capacitance. As for the change in the full depletion voltage, past experience from the BaBar experiment, whose silicon sensor is similar to the SVD, shows that no significant performance degradation is expected even with a NIEL of 2.5×10^{13} neq/cm^2 [21].

The types of particles that dominantly contribute to the SVD beam background are electrons and positrons. They increase hit occupancy and cause radiation damage. The bulk damage mainly comes from the neutrons and hadrons. These beam background particles either come from the beam collisions at the IP or from the secondary particles in the off-IP

scatterings between beam background products and accelerator beam pipe or other detector material.

1.5.2 Background level projection at target luminosity

The beam background rate at nominal luminosity is estimated by a simulation carried out at the designed machine parameters (Table 1.1). The simulated single-beam background values are re-scaled by the Data/MC factors, the ratio of real occupancy over simulated occupancy at the same beam parameters, derived in dedicated beam background studies [14]. The luminosity background components are not scaled since reliable Data/MC factors was not derived (to be studied in Chapter 2). The re-scaled simulation is shown in Fig. 1.16, with expected hit occupancy, dose rate, and 1-MeV neutron equivalent fluence being about 3% (corresponding to a hit rate of $2.0\,\mathrm{MHz/cm^2}$), $0.22\,\mathrm{Mrad/smy}$, and $5.2 \times 10^{11}\,\mathrm{neq/(cm^2\,smy)}$, respectively. 1 smy (Snowmass year) is $1 \times 10^7\,\mathrm{s}$, representing the approximate operation time in one year. This extrapolation involves a large uncertainty, because it assumes collimators can be operated close to ideal settings and does not include injection background. With this caveat, considering the occupancy limit of about 5%, we will have a safety margin of about 1.7 with respect to the present background extrapolation. A safety factor, about 3, is derived for radiation damage effects after 10 years of operation at the design machine parameters, considering the above-quoted limits of $6\,\mathrm{Mrad}$ and $1.4 \times 10^{13}\,\mathrm{neq/cm^2}$.

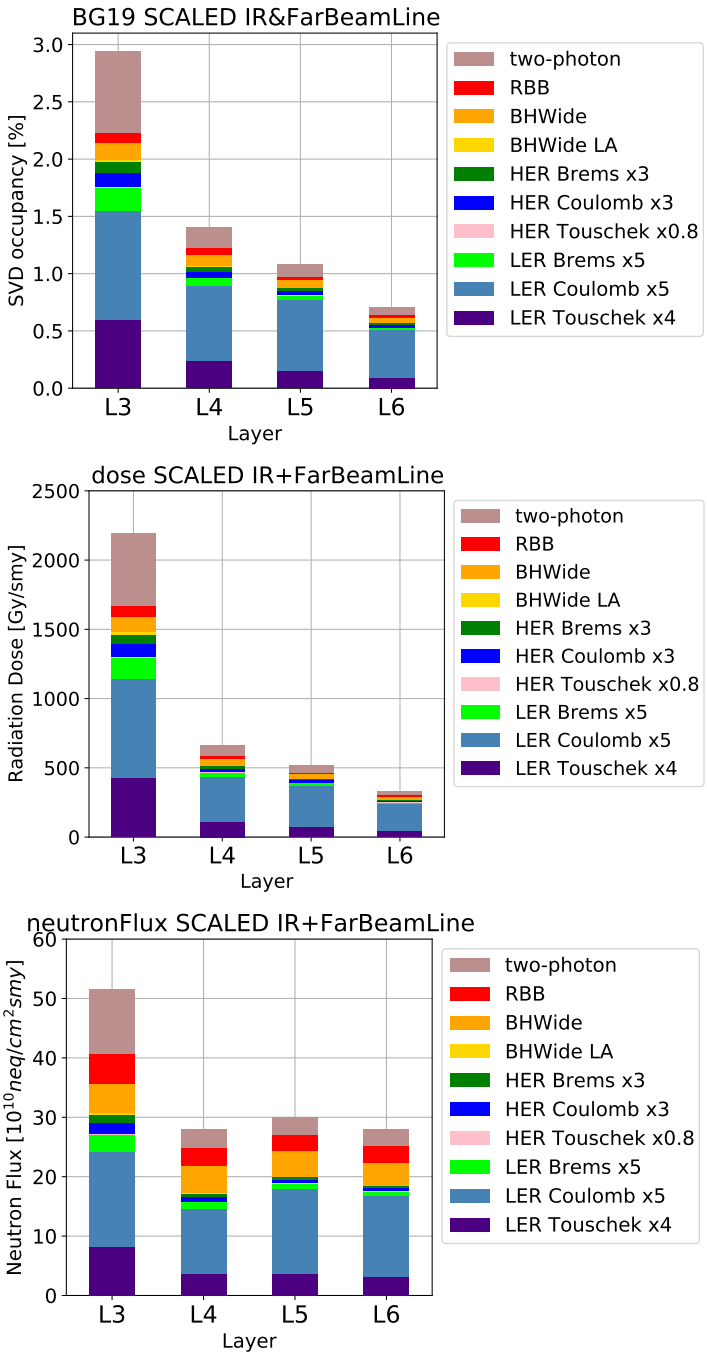


Figure 1.16: Occupancy, TID and 1-MeV neutron equivalent fluence of all the SVD Layers in MC simulation. Contributions from luminosity background (two-photon, "RBB", "RHWide" and "BHWide LA") and single-beam background (Bremsstrahlung, Coulomb scattering, and Touschek effect) are considered, with each component is re-scaled using Data/MC factors derived in 2020 and 2021 background studies. This simulation is performed at a luminosity of $8.0 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ [14]

1.6 Possible improvements of the SVD

This section lists the possible improvements of the SVD, which are the motivations of the VXD upgrade plans to be described in Section 1.7.

Firstly, better beam background tolerance is expected for the upgraded SVD. Even though the extrapolated hit occupancy at the target luminosity is below the the SVD limits, the safety factor of 1.7 is marginal. Furthermore, this extrapolation could be under-estimated because a perfect collimator configuration was applied to minimize the occupancy and beam loss rate, ignoring the beam injection efficiency. In addition, this extrapolation does not include the injection background. If a smaller pulse width of the shaper output can be realized in the readout electronics, the signal pile-up could be avoided and thus a limit on hit rate could be raised.

Secondly, better physics performance can be achieved by further reduction of material budget. Due to the relative long lifetime, K_S^0 decays within the SVD volume without leaving hits on the PXD. For this reason, the multiple scattering of charged particles inside the SVD degrades the vertex resolution of K_S^0. On the other hand, multiple scattering also degrades the tracking of low momentum particles.

Thirdly, a longer level-1 trigger latency is expected from SVD. The maximum acceptable level-1 trigger latency is limited by the depth of analog pipeline in APV25, which is 5.0 µs as calculated in Section1.4.2. This value is the smallest among all subsystems and becomes the bottleneck of the allowed process time in the level-1 trigger system. With a longer level-1 trigger latency, the trigger system can be more sophisticated to achieve better performance.

Fourthly, participation in level-1 trigger of VXD can contribute to beam background rejection. As the increase of the SuperKEKB luminosity, the triggers caused by beam background appear more frequently and the total trigger rate could go beyond the Belle II trigger rate limit of 30 kHz. A powerful method of rejecting beam background triggers would be confining the vertex of the event be near the IP since a large fraction of beam background comes from beam pipe and origins in large Z area. Currently, the VXD hit information is not used in the level-1 trigger decision and thus the Z coordinate of vertex could be reconstructed only from the CDC. However, the Z resolution of the CDC is about ±15 cm, far from satisfactory. Participation of the VXD is expected to greatly improve this Z resolution.

1.7 The Thin Fine-Pitch SVD (TFP-SVD) upgrade plan

The upgraded SVD should be able to tolerate the simulated hit rate, dose rate and 1-MeV neutron equivalent fluence simulated at an instantaneous luminosity of $8.0 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ (Fig. 1.16) with a safety factor of 5. To be specific,

- Hit rate $>$ 10 (3.2) MHz $\cdot\,\mathrm{cm}^{-2}$
- Total ionizing dose $>$ 11 (3.0) Mrad
- 1-MeV neutron equivalent fluence (NIEL) $> 2.6 \times 10^{13}$ (1.4×10^{13}) neq $\cdot\,\mathrm{cm}^{-2}$

are required for detector placed at the position of Layer 3 (Layer 4) of the current SVD in 10-years' operation. Four different detector upgrade plans are proposed:

- Thin Fine-Pitch SVD (TFP-SVD)

	Thickness	Readout strip pitch (P/N side)
Current DSSD (Large rectangular sensor)	320 µm	75/240 µm
TFP-DSSD (target)	140 µm	75/85 µm

Table 1.3: Comparison of thickness and readout pitch between TFP-DSSD and the DSSD used in current SVD

- DEPFET
- CMOS MAPS
- Silicon On Insulator (SOI)

While the TFP-SVD and DEPFET maintain the combination of the pixel and strip detectors as the current VXD, CMOS MAPS and SOI program aim to replace the whole VXD with pixel detector. The TFP-SVD also plans to replace the inner layers of CDC if they cannot withstand the high hit rate at high luminosity.

This thesis focuses on the TFP-SVD program and the detailed upgrade proposal is introduced in this section. The detailed description of other upgrade plans can be found in the Snowmass Whitepaper of Belle II upgrade [22].

1.7.1 New sensor: TFP-DSSD

A new DSSD sensor with thinner thickness down to 140 µm, and strip pitches of less than 100 µm both in p-side and n-side was proposed, named as TFP-DSSD. A comparison of thickness and readout pitch between TFP-DSSD and the DSSD used in current SVD is shown in Table.1.3. With the thickness being only half of current DSSD, the new sensor has a small material budget of only $0.19\%X_0$. The TFP-SVD continues adapting the "chip-on-sensor" concept and plans to replace the copper flexible circuit board with aluminum flexible circuit board, which reduces the material budget further. The target material budget of TFP-SVD is about $0.4\%X_0$ per layer which improves the K_S^0 vertex resolution and the momentum resolution of low-momentum tracks. The thinner thickness also mitigates the rising full depletion voltage caused by the NIEL damage. Figure 1.17 shows the measured full depletion voltage as the function of NIEL flux for a 300 µm thick semiconductor sensor, whose thickness is close to the DSSD applied in the SVD. After the type-inversion happens around 1×10^{12} neq/cm^2, the full depletion voltage raise rapidly and exceeds 100 V at around 2×10^{13} neq/cm^2. A higher depletion voltage brings difficulties into the real operation, and thus limits the acceptable NIEL. On the other hand, the full depletion voltage is proportional to the square of the sensor thickness, with the half thickness, the full depletion voltage reduced to 25%. Considering the leakage current damage rate $\alpha = 4 \times 10^{-17}$ A/cm [23], the expected leakage current with 52.6 mm × 59.0 mm × 140 µm volume sensor at 25 °C is calculated to be about 450 µA after 10 Mrad irradiation.

The finer strip and smaller sensor size pitches reduce the average hit rate on each strip and thus can mitigate the signal pile-up in high luminosity operation. However, on the other hand, the thinner thickness and finer pitch also reduces the signal charge induced on each readout

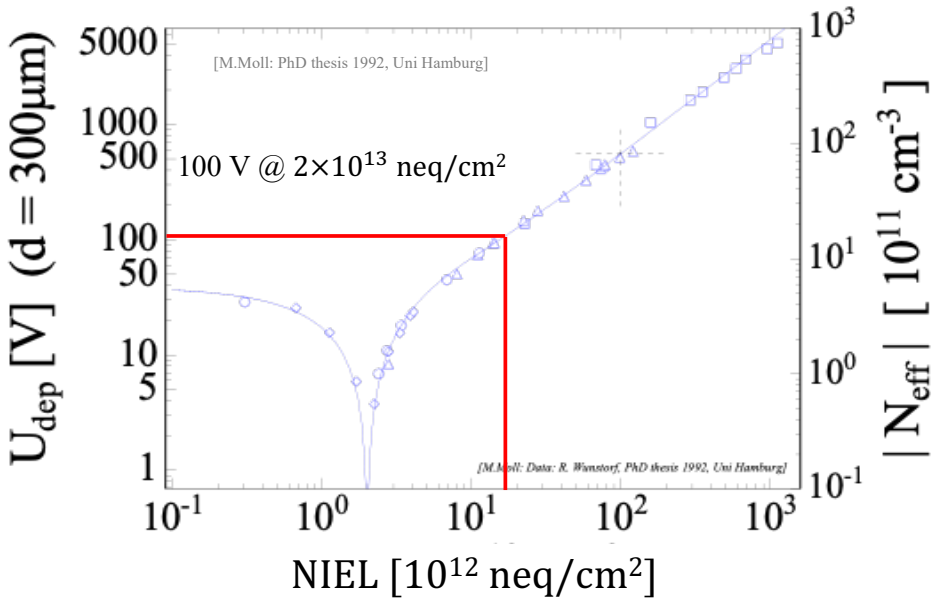


Figure 1.17: Measured full depletion voltage as a function of NIEL flux for a 300 µm thick semiconductor sensor [24]. N_{eff} refers to the density of effective charge carriers of the bulk when no bias voltage is applied.

strip. To increase the number of charge induced on each strip, in TFP-DSSD, all of the floating strips are removed from the sensor design compared to the DSSD in the SVD to avoid charge sharing among the adjacent strips. Simulation study on the 140 µm thick TFP-DSSD sensor shows that the minimal charge of the seed strip in one cluster for TFP-DSSD is about 4000 electron (Fig. 1.18) [25].

The TFP-DSSD sensor has a size of 52.6 mm × 59.0 mm for the first version and aims to make 70 mm × 70 mm sensors out of 4-inch wafer. The inter-strip capacitance is 6.5–8.0 pF for the first version size and the target of total detector capacitance (including capacitance from sensor bulk and pitch adapter etc.) is 15 pF.

1.7.2 New front-end ASIC: SNAP128

Given the upgrade requirements and the properties of the TFP-DSSD sensor, a dedicated new ASIC, SNAP128 (SVD upgrade with NArrow Pitch sensors with 128-channel inputs), is developed as the front-end readout chip of TFP-DSSD. The development is being done by the electrical system group in KEK [26], based on the SliT128 readout ASIC [27] for KEK g-2 experiment.

To guarantee a strip S/N larger than 5, which is defined to be the ratio of signal charge collected by one TFP-DSSD strip and ENC of one channel in front-end ASIC, the ENC of each channel in SNAP128 is required to be smaller than 800 electrons at a detector capacitance of 15 pF. To reduce the signal cable amount by high-speed serial links, instead of digitizing the shaper output using a 10-bit ADC like the FADC in the SVD, only the binary data of the strip hit information are read out. The pulse width of shaper output is designed to be 52 ns, with which the possibility of signal pile-up will be 5.9% (1.9%) for expected hit rate with safety

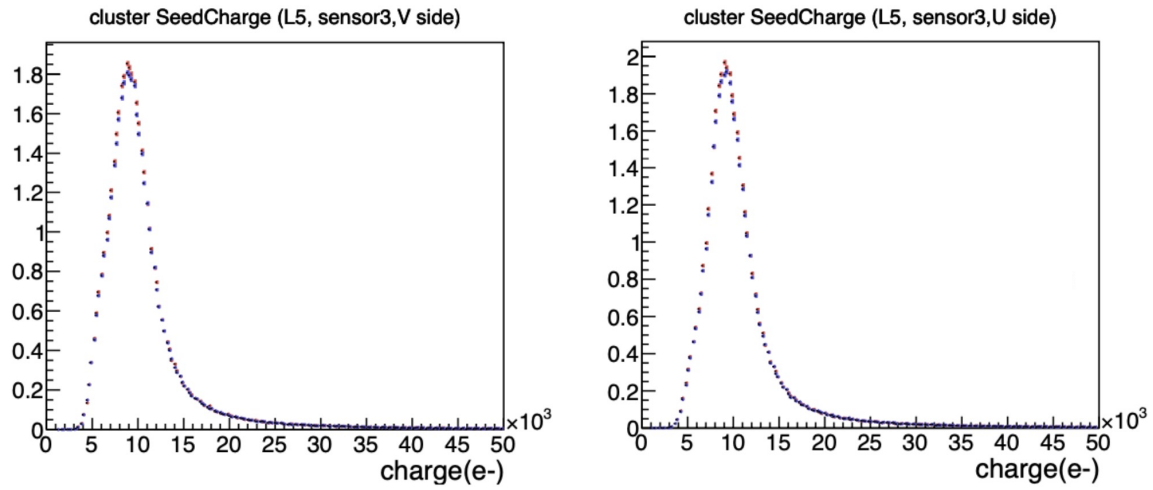


Figure 1.18: Distribution of signal charge in seed strip of one cluster for TFP-DSSD sensor in simulation. A sensor thickness of 140 µm is assumed.

factor 5 on Layer 3 (Layer 4) sensors at benchmark luminosity (assuming the area covered by one strip being 85 µm × 70 mm and cluster size being 2). And finally, the hit information is to be sampled with the 127 MHz clock for enough hit-time resolution to distinguish the physics particle hits and the beam background hits.

The logic OR of the 127 MHz binary hit information from 128 channels are output to participate the level-1 trigger decision. With the participation of the VXD, the level-1 trigger is expected to find tracks with a production point resolution of about 1 cm. The extraneous tracks due to the beam background that originate close to the interaction point results in frequent fake CDC triggers. They can be efficiently rejected by the new VXD level-1 trigger. Currently, the performance and algorithm of this trigger is being developed [28] and is not covered in this thesis.

The digital part of each channel has a 2048-depth ring buffer, which holds the binary hit information up to about 16 µs (= 1/127 MHz×2048) until the chip receives the trigger signal. When the trigger signal arrives, the binary information in the corresponding time window is read out from the ring buffer. The readout binary data from the 128 channels are serialized and sent as the SNAP128 output as a 127 Mbps output data.

The power consumption is to be kept at the same level as APV25, 400 mW/chip, for the feasibility of the heat absorption by a realistic cooling system.

Chapter 2

Studies of luminosity beam background in the SVD

Expected high beam background level at the target luminosity is the main concerns for the future operation of SVD and is the main motivation for the TFP-SVD upgrade plan. There are two main beam background categories: single-beam background and luminosity background. While the modeling of single beam background in real data and its comparison with simulation has been studies thoroughly by H. Tanigawa [29], behavior of luminosity beam background cannot be explained by the assumed model and thus the measurement and simulation could not be compared properly. In this chapter, a spatial distribution fitting method is proposed to extract luminosity background components from real data and performed the comparison between data and simulation (derive Data/MC ratio). The beam background projection at benchmark luminosity is also updated using the new Data/MC ratio for luminosity background.

Section 2.1 shows a detailed description of the significant beam background sources in the SVD. Section 2.3 describes the dataset to be used in this analysis. Section 2.4 shows the modeling of single-beam background and its extraction from the real data. Section 2.2 shows the strategy to extract luminosity background contribution in real data. Section 2.5 gives a detailed description of the luminosity background simulation. Section 2.6 and Section 2.7 shows the extracted fit result and the comparison result between data and simulation. And finally, a summary of this study is given in Section 2.8.

2.1 Beam background sources

Beam backgrounds can be categorized into single-beam background and luminosity background. The single beam background represents the background that are induced by the existence of one beam, while the luminosity background is also called collision background, which is induced due to the collision of electron and positron beams.

For the single-beam background, the contribution from the intra-beam scattering (Touschek effect), and the scattering between beam particles and residual gas nucleus (Beam-gas scattering) are dominant. Due to the scattering between electrons/positrons within one bunch, the particles deviate from the trajectory inside the collider and hit into the beam pipe and create electromagnetic shower. If the particle loss happens near the detector, the shower leaves hits on the detector. The beam-gas scattering can be further divided into the Coulomb scattering and the Bremsstrahlung. In the Coulomb scattering case, the beam particles are scattered out of the trajectory directly. In the bremsstrahlung case, the beam particles lose energy after passing by the charged residual nucleus while keeping the motion direction. Later the particles deviate from the trajectory gradually due to the energy loss. A schematic for the Touschek

scattering, Coulomb scattering and bremsstrahlung is shown in Fig. 2.1. Other sources of single-beam background like synchrotron radiation are neglectable when considering the SVD occupancy.

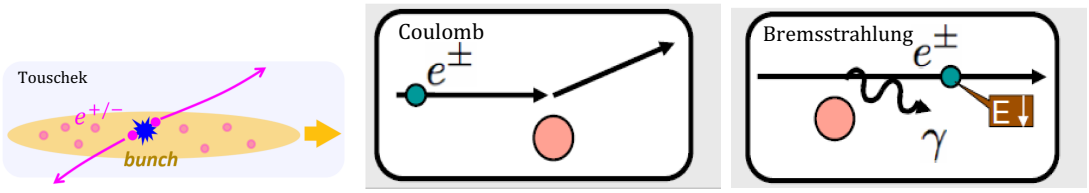


Figure 2.1: Schematic for three Single-beam background processes: Touschek effect (left), Coulomb scattering (mid) and bremsstrahlung (right).

Given that Touschek effect is the particle effect within one bunch, the rate is proportional to

$$I \cdot \frac{I/n_b}{\sigma_x \sigma_y \sigma_z} = \frac{I^2}{n_b \sigma_x \sigma_y \sigma_z} \tag{2.1}$$

where I is beam current, n_b is number of bunches in one beam, σ_x, σ_y represent the beam size in x, y direction respectively. σ_z is the bunch length.

Beam-gas scattering is the particles scattered out of trajectory due to scattering with the residual gas nucleus inside the beam pipe. The rate is proportional to

$$I \cdot P \tag{2.2}$$

where P is the pressure in the beam pipe.

Luminosity background comes from the beam collision. For SVD, the dominant processes are two-photon process and radiative Bhabha, whose Feymann diagrams are shown in Fig. 2.2. The two-photon process $e^+e^- \to e^+e^-e^+e^-$ produces low-momentum electron-positron pairs that spiral inside the SVD volume, leaving considerable number of hits on SVD. The photon produced in the radiative Bhabha scattering $e^+e^- \to e^+e^-\gamma$ hits the downstream materials and produce secondary particles. These particles then leave hits on the detector. In addition, the beam electrons and positrons whose energy is lost in the radiative Bhabha process deviate from the trajectory and hit the beam pipe. The rate of luminosity background is proportional to the collision luminosity L.

In SuperKEKB, beams are injected into the main storage ring at a frequency of 50 Hz in continuous operation. The phase space of injected beam does not overlap totally with the acceptable phase space of storage ring. For this reason, large beam loss happens in a few microseconds right after injection. Figure 2.3 shows the average occupancy of one side of SVD Layer 3 sensors after LER injection. It is observed that the occupancy right after injection (0∼10 µs) is more than a factor 10 larger compared with the occupancy a few microseconds away from the injection. For this reason, the events right after injection, which are heavily polluted by injection background, are vetoed out and not sent to DAQ system and thus does not contribute to SVD occupancy while taking physics data. But irradiation effects from injection background like TID and NIEL should still be considered in the beam background projection to the target luminosity.

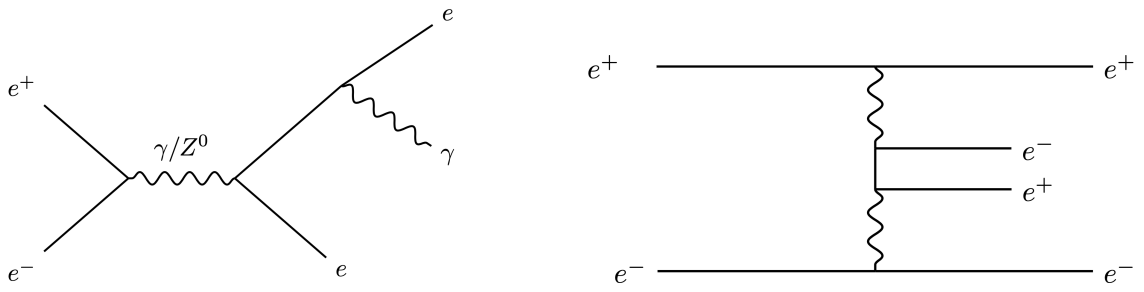


Figure 2.2: Feynman diagrams of Luminosity background. Left for radiative Bhabha process and right for two-photon process

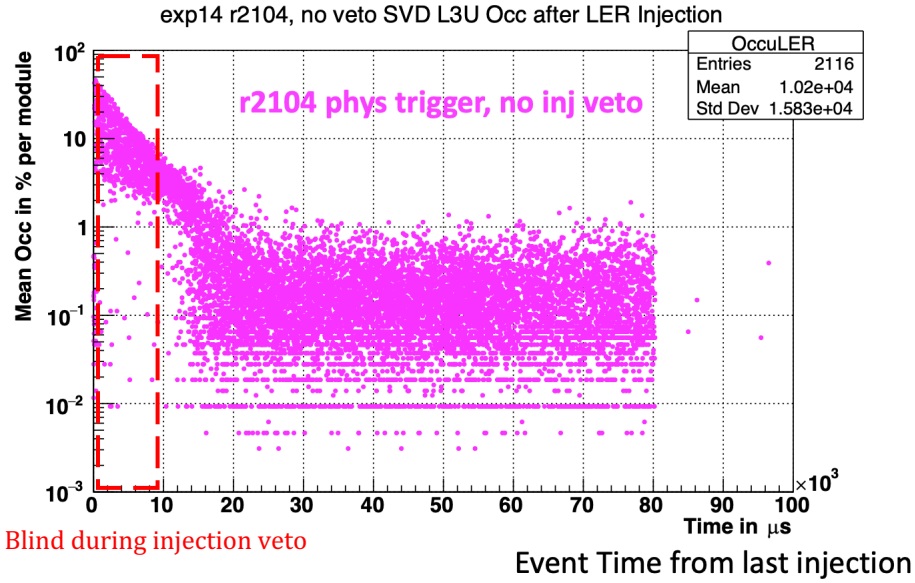


Figure 2.3: SVD occupancy in Layer 3 as a function of time after injection. The green rectangle represents the injection veto. Events within this veto are not sent to DAQ system in the physics run.

2.2 Analysis strategy

Luminosity background could be seen only when beams collide, with contribution from single-beam background. For this reason, the luminosity background is extracted by subtracting the estimated single-beam background contributions from the measured SVD hit occupancy. The single-beam background occupancy can be measured in advance by either electron or positron beam injected in the main ring alone. At the same time, the expected hit occupancy of the luminosity background is simulated using the Monte Carlo (MC) simulation. And finally, the ratio between the occupancy of the luminosity background from the measurement and simulation is defined as a Data/MC ratio to describe this discrepancy between the reality and expectation.

In the previous study performed by Hikaru Tanigawa [29], only the average occupancy of Layer 3 sensors was used to evaluate the luminosity background:

$$O_L = \mathcal{O}_{\rm data} - O_B^{LER} - O_B^{HER} - O_T^{LER} - O_T^{HER} \tag{2.3}$$

where O_L is the extracted luminosity background occupancy, $\mathcal{O}_{\rm data}$ is the average occupancy in the SVD layer 3 sensors, $O_B^{LER(HER)}$ is the beam-gas background from LER (HER) and $O_T^{LER(HER)}$ is the Touschek background from LER (HER). The modeling of single-beam background occupancy is described in Section 2.4. However, the beam-beam effect* can change the beam size in the ring and then affects the Touscheck background component. This can cause the discrepancy of the Touschek hit occupancy from the one estimated from the single-beam background study and the extrapolated single-beam background occupancy becomes larger than the total occupancy in the collision period (top plot in Fig. 2.4). For this reason, correction factors (a and b) are introduced in for LER and HER Touschek component:

$$O_L = \mathcal{O}_{\rm data} - O_B^{LER} - O_B^{HER} - a \cdot O_T^{LER} - b \cdot O_T^{HER} \tag{2.4}$$

In Hikaru's study, he estimated the Touscheck contributions to the beam loss from the beam loss rate (dI/dt) measurement, which is an independent measurement of the SVD hit occupancy, and determined the correction factors as the ratios between the Touscheck contributions during the single-beam and during beam collisions. Using the beam loss rate monitor, an integrated beam loss over the entire main storage ring is calculated, while only the beam loss around the IP should be taken into account when considering beam background on the SVD. The Touschek correction factor obtained from the beam loss rate monitor is possibly not able to evaluate change in Touschek background near the IP. With $a = 0.91$ and $b = 0.46$ derived in beam loss rate measurement, the calculated Data/MC ratio has a 30% difference when the accelerator is in "top-up" beam injection mode or in no beam injection mode (bottom plot in Fig. 2.4). To solve this problem, we developed a new method to evaluate the correction factors using the SVD data. In the method, we treat the correction factors as free parameters and determine the luminosity background and correction factor simultaneously by fitting the spatial distribution of the measured hit occupancy with the pre-determined spatial distributions of the single-beam background and luminosity background. The details of the method is described in Section 2.6.

*Effects on the beam property due to the interaction between the electron and positron beams when they are crossing at the IP

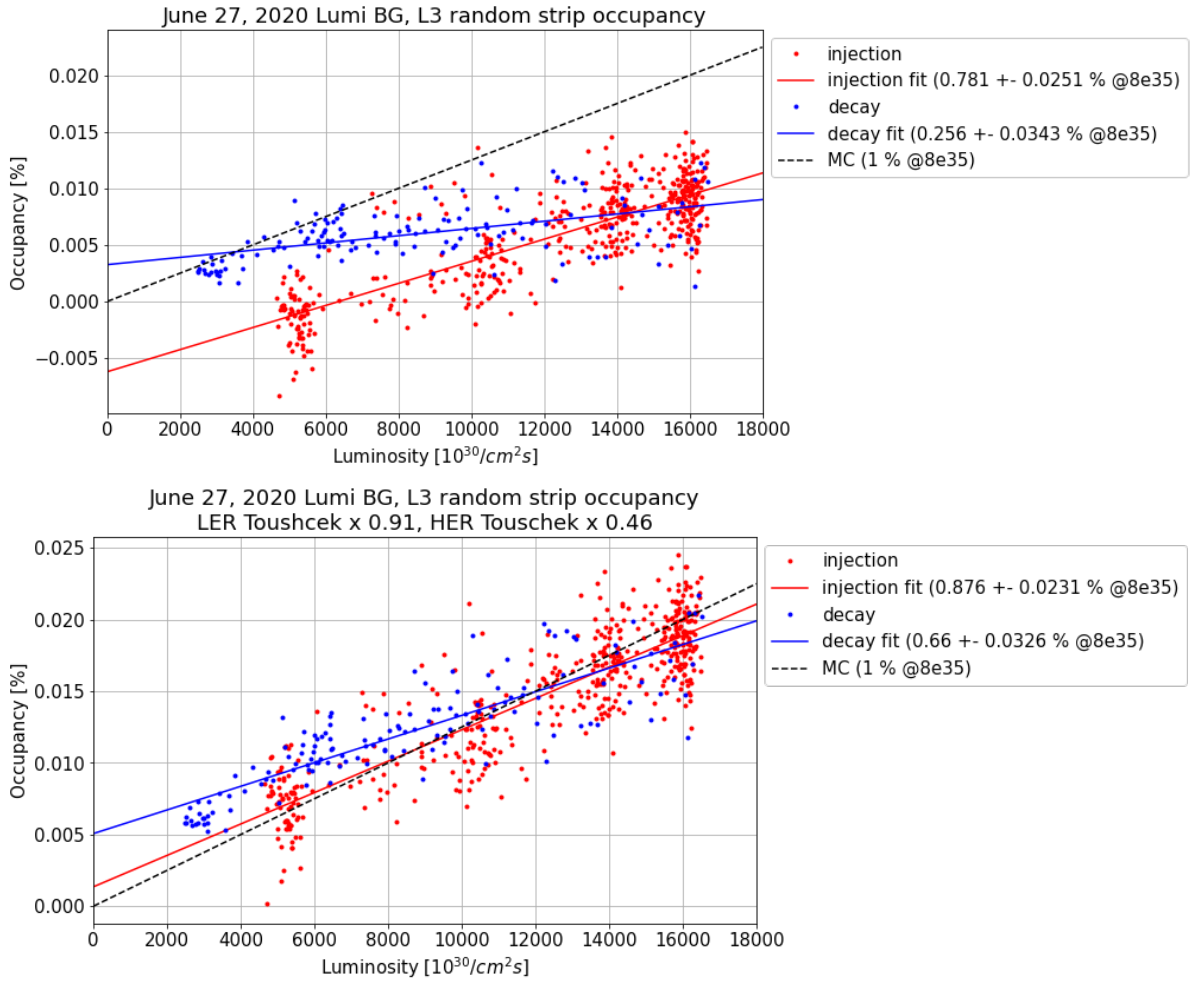


Figure 2.4: Extracted luminosity background occupancy as a function of luminosity using the method in Hikaru's study [29]. The red (blue) dots represents the data in "top-up" (decay) period. The red and blue line represents the corresponding linear fitting between occupancy and luminosity. The black dashed line is the simulation result. The top plot is derived without Touschek correction factor and the bottom plot used the correction factor from beam lifetime study. In the top plot, the extracted occupancy has minus value while for the bottom plot, the extrapolated occupancy from "top-up" and decay period data to Belle II benchmark luminosity has a 30% difference.

2.3 Dataset used in this analysis

The strip charts of the beam background study run on June 16, 2021 is shown in Fig. 2.5, showing the LER/HER beam current, recorded luminosity and the average occupancy on SVD Layer 3 sensors in every 10 s and the recorded luminosity of Belle II. In this run, LER and HER beams are injected alone first to study the single-beam background and the two beams collide afterwards to study the luminosity background.

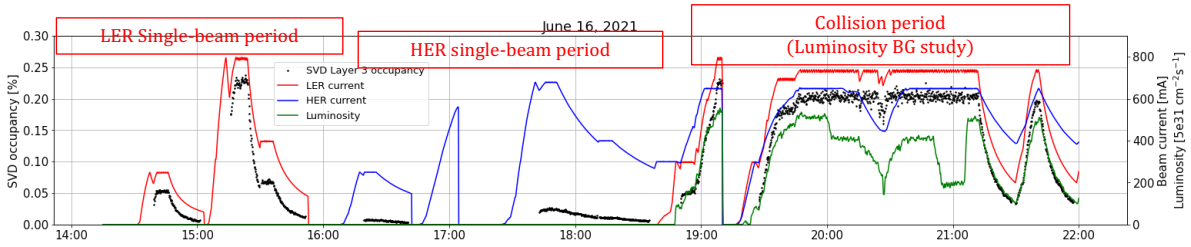


Figure 2.5: Strip chart of June 16, 2021 beam background study. The red and blue lines stands for the beam current in LER and HER, respectively. The green points represents the recorded luminosity. The black points represents the average occupancy on SVD Layer 3 sensors of every 10 seconds.

2.4 Modeling of single-beam background

Considering the mechanism of the background creation explained in the Section 2.1, The single-beam background occupancy of each SVD sensor can be written in the following formula:

$$\mathcal{O}_{\text{singlebeam}}(I, P_{\text{BP}}, \sigma, n_b | T, B) = T \cdot \frac{I^2}{n_b \sigma_x \sigma_y \sigma_z} + B \cdot I P_{\text{BP}} \tag{2.5}$$

with the first term being the contribution from Touschek components and the second term being that of beam-gas components. Coefficients T and B represents the amount of the contributions from the Tousheck and beam-gas background, respectively. I is the beam current, n_b is the number of bunch and $\sigma_{x(y)}$ is the beam size in horizontal (vertical) direction. σ_z is the bunch length. While $\sigma_{x(y)}$ can be monitored in real time by the X-ray and Synchrotron Radiation monitor, the bunch length is measured using a streak camera and cannot be monitored while operation. For this reason, the bunch length as a function of bunch current ($I_b = I/n_b$) is measured in advance: σ_z [mm] $= 4.15 + 2.63(I_b$ [mA]) for LER and σ_z [mm] $= 4.91 + 2.29(I_b$ [mA]) for HER [30].

P_{BP} is the beam pipe pressure averaged over the measurements at 12 locations in the ring. They are measured by cold cathode gauges (CCG). The CCGs are close to the sputter ion pumps which are located outside the beam pipe. For this reason, the change in the pressure measured by the CCGs is smaller than the actual change in the pressures of the beam pipe. Therefore, the pressure measured by the CCGs is represented as [31]:

$$P_{\text{CCG}} = k_0 + k_1 \cdot P_{\text{BP}} \tag{2.6}$$

Using P_{CCG}, Eq. 2.5 can be rewritten as:

$$\mathcal{O}_{\text{singlebeam}}(I, P_{\text{CCG}}, \sigma, n_b | T, B_2, B_3) = T \cdot \frac{I^2}{n_b \sigma_x \sigma_y \sigma_z} + B_2 \cdot I P_{\text{CCG}} - B_3 \cdot I \tag{2.7}$$

with the new coefficients B_2 and B_3 are both larger than 0.

Occupancy of each SVD sensor is fit to the single-beam background model (Eq.2.7) to extract the floating parameter T, B_2 and B_3, with which contribution from single-beam background can be extrapolated to the collision period. As an example, the fitting results of sensor

L3.1.1 for LER and HER single-beam background are shown in Fig. 2.6. The hit occupancy under different beam currents and different numbers of bunches are used to determine the Touschek and beam-gas components separately. The occupancy data in the decay period is used as the input of fitting to avoid the possible injection background and the fitting result (magenta line) agrees well with the data. The extrapolation of the fitting result agrees with the measured occupancy even during the beam injection. This indicates that the contributions from the injection background is well eliminated by the injection veto. The extrapolated occupancy in the collision period is also shown in Fig. 2.6.

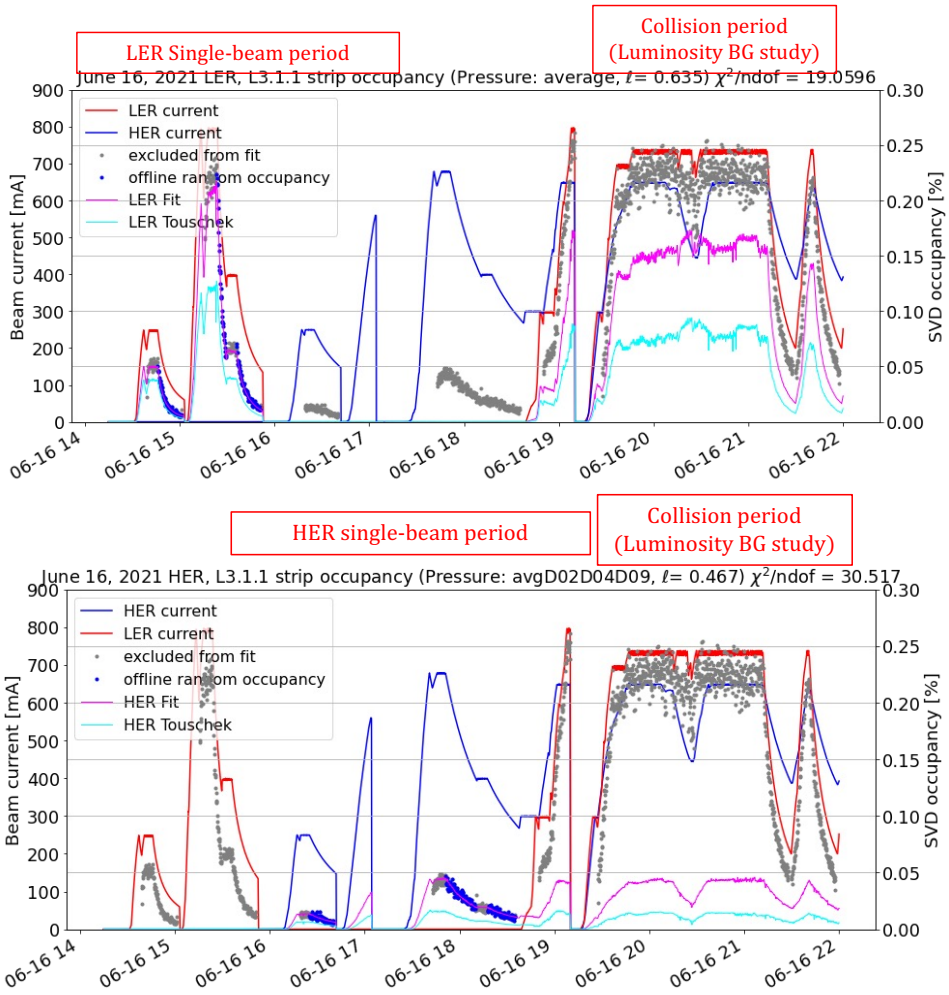


Figure 2.6: Single-beam background fitting result for LER (above) and HER (below). The horizontal axis represents time in the format "month-date hour". Before 18:50 is the single-beam period while after that is the collision period. In the single-beam period, for both LER and HER, beams are first injected with $n_b = 393$ and afterwards changed to $n_b = 1174$ to have a better separation between Touschek and beam-gas components. The blue dots represents the occupancy that are used as the input of fitting, while the gray dots are unused. The magenta line represents the fitting result and the light blue line represents the contribution from Touschek component. The different between these two lines is the contribution from beam-gas component.

2.5 Simulation of luminosity background

The luminosity background is estimated using the Monte Carlo simulation. The generator of the two-photon process is AAFH [32]. The radiative Bhabha process is divided into three different categories depending on the scattering angle of electron and positron ($\theta_{e^\pm}$). "BH-WideLargeAngle" (BHWide LA) refers to events with both θ_{e^+} and θ_{e^-} are larger than 1° and at least one of them are larger than 10°. "BHwide" refers to events that both θ_{e^+} and θ_{e^-} are larger than 0.5° and ate not BHWide LA events. The rest of Radiative Bhabha events are called "RBB". The generator for "BHWide LA" and "BHWide" events is BHWIDE [33] and "RBB" uses BBBREM [34] as the generator. These events are generated at a luminosity of L =8.0 $\times$ 10^{35} $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

The events from the generator mentioned above are used as the input of Geant4 [35] to calculate their interaction with the detector. Since the Belle II trigger is not synchronized with the collision, the energy deposition of each event is randomized in the time axis. After that, the energy deposition information are then passed on to the Belle II Analysis Software Framework (basf2) [36] to simulate the signal propagation inside sensor and the response of APV25, followed by the reconstruction of hit information and calculation of occupancy. The simulated occupancy of each luminosity background component averaged on each SVD layer is shown in Fig. 2.7.

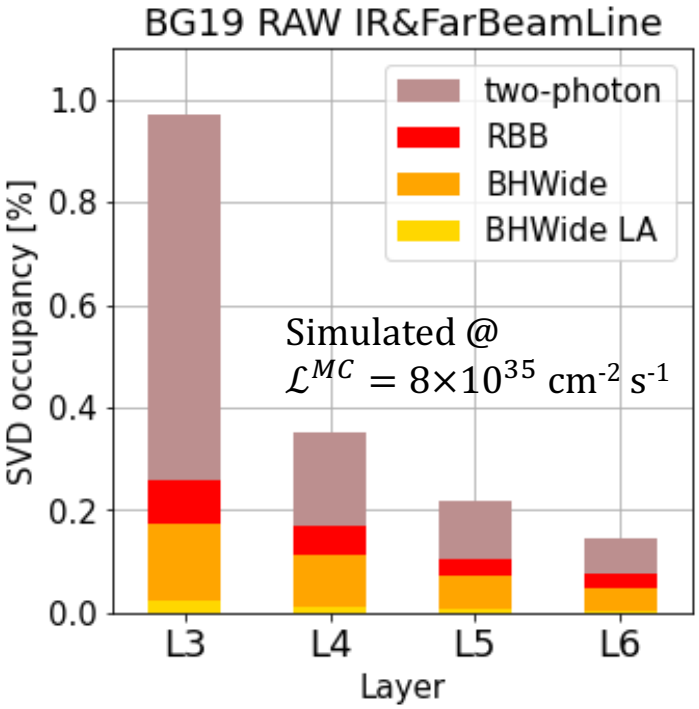


Figure 2.7: Simulated occupancy of each component averaged on each SVD layer. This occupancy is simulated at a luminosity of 8.0 $\times$ 10^{35} $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

2.6 Extraction of luminosity background from data

The hit occupancy of each sensor during the beam collision can be expressed as the following formula:

$$\mathcal{O}_{\rm data}(i) = O_B^{LER}(i) + O_B^{HER}(i) + a \cdot O_T^{LER}(i) + b \cdot O_T^{HER}(i) + \frac{\mathcal{L}^{Fit}}{\mathcal{L}^{MC}} \cdot O_L^{MC}(i) \tag{2.8}$$

where i is the index of the SVD sensor, $\mathcal{O}_{\rm data}(i)$ is the measured occupancy of the $i^{\rm th}$ sensor. $O_{B(T)}^{LER(HER)}(i)$ is expressed as:

$$O_B^{LER(HER)}(i) = B_2^{LER(HER)}(i) \cdot IP_{\rm CCG} - B_3^{LER(HER)}(i) \cdot I \tag{2.9}$$

$$O_T^{LER(HER)}(i) = T^{LER(HER)}(i) \cdot \frac{I^2}{n_b \sigma_x \sigma_y \sigma_z} \tag{2.10}$$

with $O_B^{LER(HER)}(i)$ being the LER (HER) beam-gas background occupancy of the $i^{\rm th}$ sensor and $O_T^{LER(HER)}(i)$ being the LER (HER) Touschek background occupancy of the $i^{\rm th}$ sensor. Coefficients $B_{2(3)}^{LER(HER)}(i)$ and $T^{LER(HER)}(i)$ are determined by the single-beam background study as described in Section 2.4. $O_L^{MC}(i)$ is the simulated luminosity background occupancy of the $i^{\rm th}$ sensor, as mentioned in Section 2.5. a and b are correction factors for LER and HER Touschek background, representing the difference of Touschek occupancy with and without collision. The luminosity background $O_L^{MC}(i)$ is scaled to the current luminosity by applying a scaling factor $\mathcal{L}^{Fit}/\mathcal{L}^{MC}$, where $\mathcal{L}^{MC}$ $=8.0 \times 10^{35}\,{\rm cm}^{-2}\,{\rm s}^{-1}$. The scaling factor L^{Fit} is interpreted as the estimated luminosity. The correction factors a, b, and estimated luminosity $\mathcal{L}^{Fit}$ are common parameters for all sensors.

As shown in Fig. 2.5, the occupancy averaged in every 10 seconds are measured during the beam collision. At each time, the measured hit occupancies of all sensors during the beam collision are simultaneously fitted with the function shown in the right hand side of Eq. 2.8, using three fitting parameters, a, b and L^{Fit}. Because the spatial distributions of the occupancies are different for each background component, Touscheck, beam-gas, and luminosity, the fit can determine these parameters using the spatial information of the measured occupancy. By comparing $\mathcal{L}^{Fit}$ with measured luminosity (green dots in Fig. 2.5), one can derive the Data/MC ratio, which is described in Section 2.7.

The Touschek component of LER and HER and the luminosity background can be separated making use of the different characteristics of their spatial distribution. Figure 2.8 shows the SVD occupancy averaged among sensors at the same Z position. For example, L3FW represents the averaged occupancy of all Layer 3 sensors in the FW position (see the sensor location in Fig. 1.15). It can be seen that in Layer 4, 5, and 6, the LER single-beam background peaks in the forward direction while the HER single-beam background peaks in the backward direction, while in Layer 3 the peaks are seen in the opposite side. This is because the background in outer layers is mainly from upstream of the beam, while the background in inner layer, which is close to the beam pipe, is mainly from the material around the interaction point.

The luminosity background is separated from the single-beam background using the occupancy distribution in ϕ direction. Fig. 2.9 shows the normalized hit occupancy distribution of LER Touschek, HER Touschek and luminosity background in ϕ direction for Layer 3, 4, 5 and 6. Each data point in the plot is calculated from the hit occupancy in one ladder, which is the

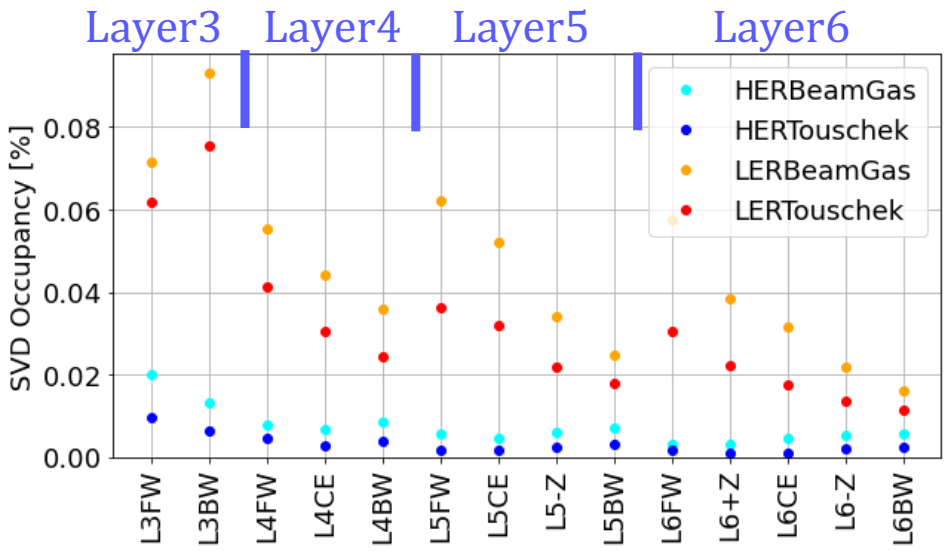


Figure 2.8: Single-beam background distribution in Z direction

averaged occupancy of all sensors in each ladder. For example, L3.1 represents the occupancy averaged over all sensors in the ladder L3.1 (see the ladder index in Fig. 1.14). Single-beam background peaks at the –X direction in Layer 4,5,6 since the beams are injected into IP chamber from the –X direction, while the luminosity background peaks in the +X direction because the colliding e^+e^- is boosted in the +X direction as shown in Fig. 1.7. Given the difference in the ϕ distribution in Layer 4, 5 and 6, Luminosity background can be separated from single-beam background.

The fitting result at a specific time (20:00:05 Jun 16, 2021) is shown in Fig. 2.10. The measured spatial distribution of the hit occupancy can be represented by the model of Eq. 2.8. The luminosity contribution to the hit occupancy is just about 8% of the total occupancy in Layer 3 at the luminosity of about $1.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The LER single-beam background is the dominant contribution to the hit occupancy.

The result of a, b and $\mathcal{L}^{Fit}$ in the whole collision period is shown in Fig. 2.11. $\mathcal{L}^{Fit}$ (magenta points) shows the same trend as measured luminosity (green points). LER Touschek correction factor (a) is close to 1 while HER Touschek correction factor (b) suffers from large fluctuation. This is because the background contribution from HER single-beam background is very small.

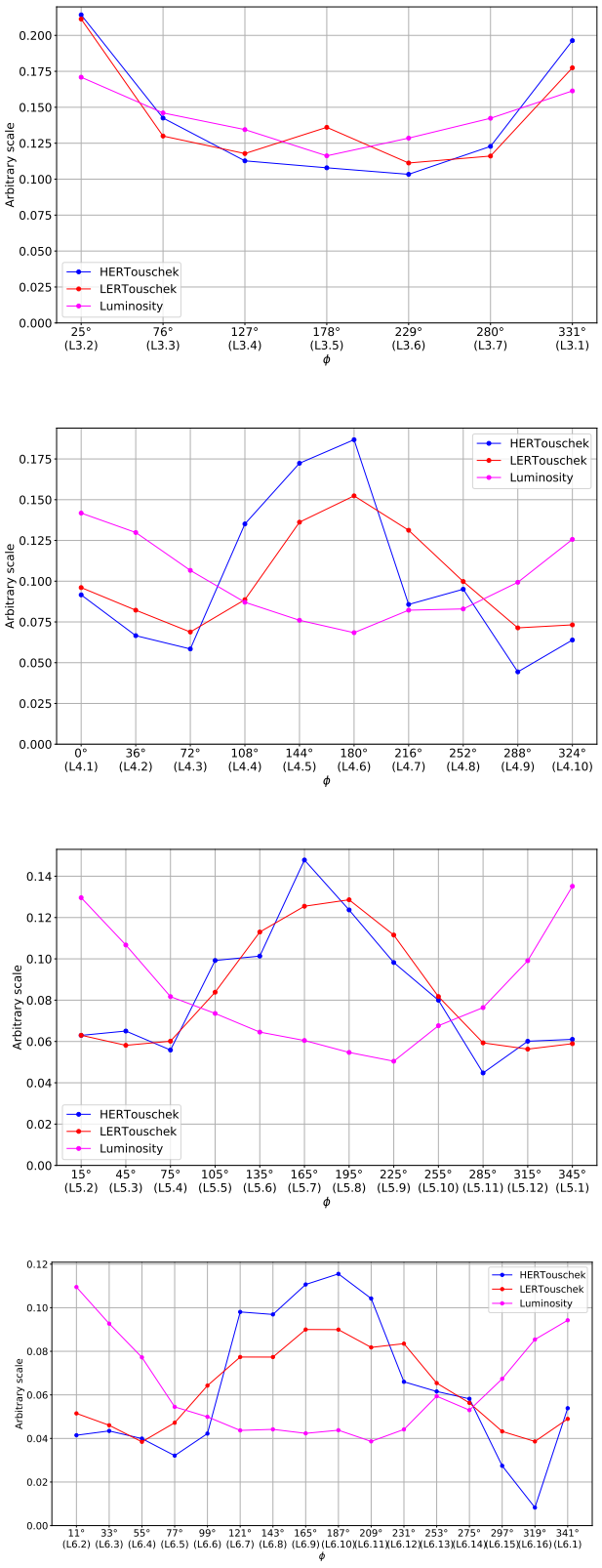


Figure 2.9: Normalized single-beam background and luminosity background distribution in ϕ direction. From top to bottom are distribution in Layer 3, 4, 5 and 6.

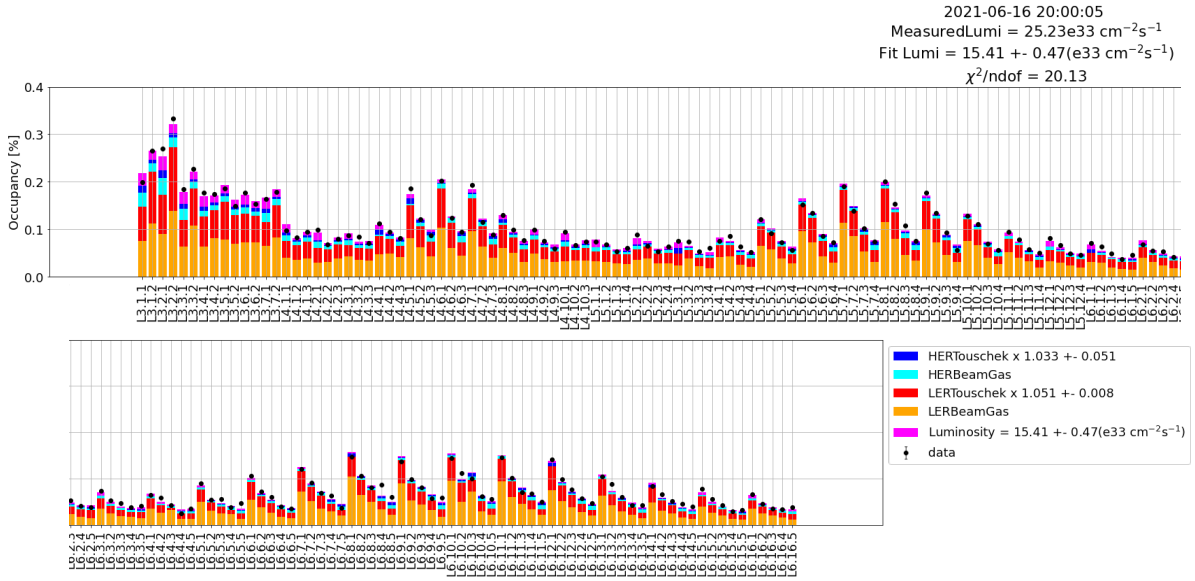


Figure 2.10: Fitting occupancy model to the total occupancy in data. The columns are the occupancy model and the black points are the occupancy of each SVD sensor. The Fit result a, b and $\mathcal{L}^{Fit}$ are shown in the legend of this plot.

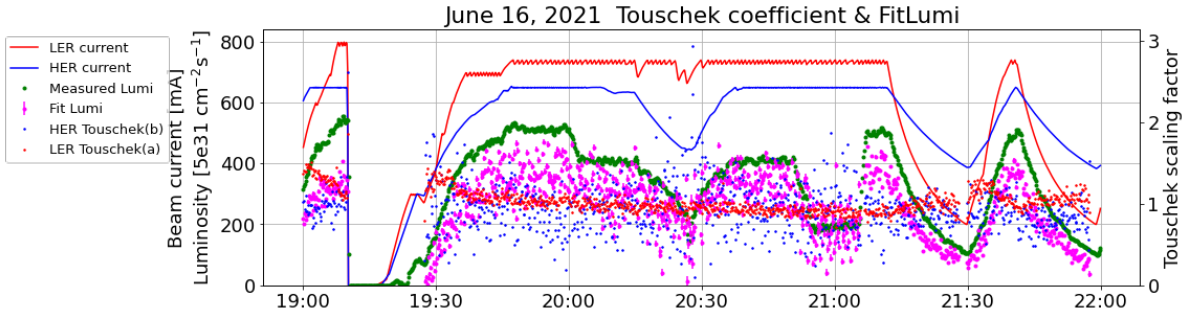


Figure 2.11: Fit results of a, b and $\mathcal{L}^{Fit}$ in the whole collision period. The green dots represents the measured luminosity and the magenta dots represents the $\mathcal{L}^{Fit}$. The LER and HER Touschek correction factors (a and b) are represented by the red and blue dots.

2.7 Extraction of Data/MC ratio

Figure 2.12 shows the $\mathcal{L}^{Fit}$ (Fit Lumi) as a function of measured luminosity (Measured Lumi). A linear relation is clearly confirmed. The data in top-up injection period and decay period are plotted separately and they show good consistency. A fitting was performed by assuming the proportional relationship between these two variables and derived the ratio between the fit luminosity and measured luminosity being 0.74.

Here, we evaluate the Data/MC ratio from the result. The Data/MC ratio for the luminosity background is defined as a ratio between the measured occupancy and simulated

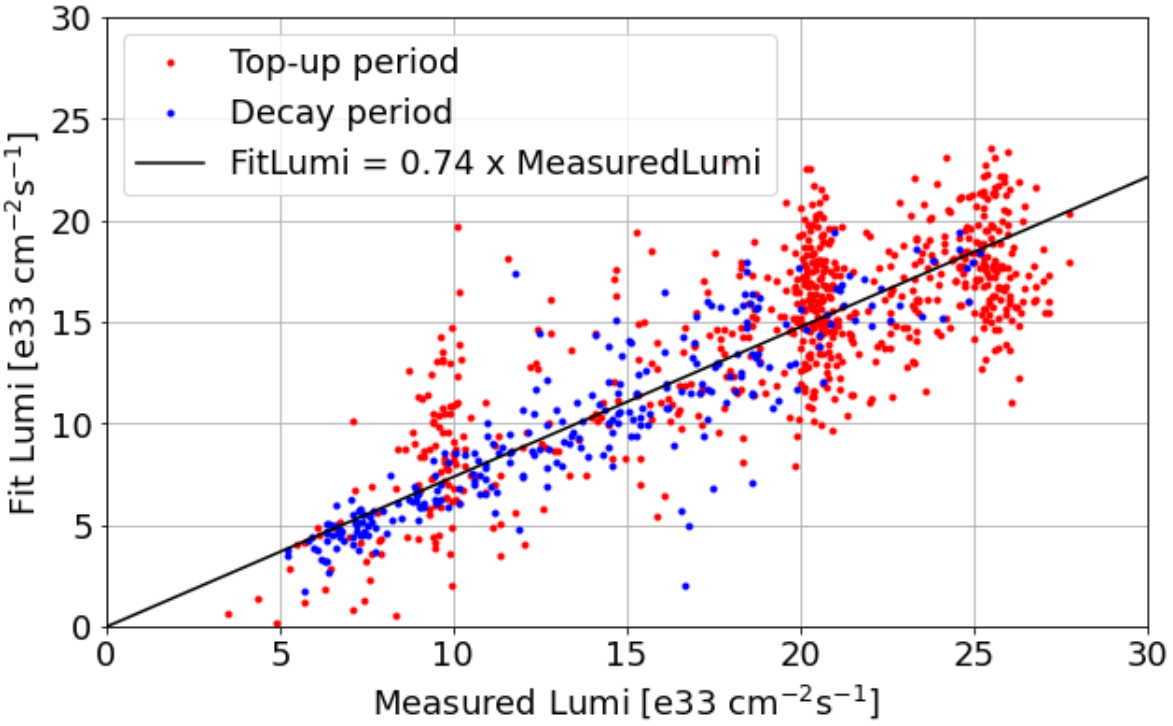


Figure 2.12: $\mathcal{L}^{Fit}$ (Fitlumi) as a function of Measured luminosity. The data point in top-up injection period and decay period are plotted separately but no obvious difference in these two data sets is observed.

occupancy under the same luminosity. Since the occupancy of the luminosity background is proportional to the luminosity, the definition is equal to the ratio between the measured luminosity and simulation luminosity which give the same occupancy both in the measurement and in the simulation. In the fitting results, L^{Fit} can be interpreted as the luminosity which results in the measured occupancy in the simulation. Therefore, the Data/MC is also equal to the ratio between L^{Fit} and the measured luminosity $L^{measure}$. The resulting Data/MC ratio is $L^{Fit}/L^{measure} = 0.74$. Currently, we believe that this discrepancy is caused by the underestimation of the occupancy from secondary particles generated in the beam background events in simulation.

2.8 Results and discussion

Up to now, luminosity background was studied three times in May 2020, June 2020, and June 2021 and the averaged over the collision period is summarized in Table 2.1. While the Data/MC ratio converging to 0.74 and LER Touschek correction factor (a) to 1, HER Touschek correction factor (b) is suffering from large fluctuation due to the small contribution from HER single-beam background.

Making use of the extracted Data/MC ratio for SVD luminosity background, the SVD beam background projection at Belle II benchmark luminosity is re-calculated and shown in Fig. 2.13. The expected hit occupancy, dose rate, and 1-MeV neutron equivalent fluence in

Dataset	June 2021	June 2020	May 2020
Data/MC	0.74	0.74	0.75
a (average)	1.04	1.02	0.73
b (average)	0.95	0.55	1.21

Table 2.1: Result luminosity background studies in May 2020, June 2020 and June 2021. The average Touschek correction factor are derived by averaging over the whole collision period

layer 3 sensors become 2.7% (corresponding to a hit rate of $1.8\,\mathrm{MHz/cm^2}$), $0.20\,\mathrm{Mrad/smy}$, and $4.6 \times 10^{11}\,\mathrm{neq/(cm^2\,smy)}$, respectively, with a reduction of about 10% compared to the result shown in Fig. 1.16. However, the ratio of occupancy limit 5.0% over the new expected occupancy 2.7% is about 1.9, still below the desired safety margin 5. For this reason, the conclusion that the existing SVD barely withstands with the high beam background near target luminosity still holds, and the motivation for the SVD upgrade does not change.

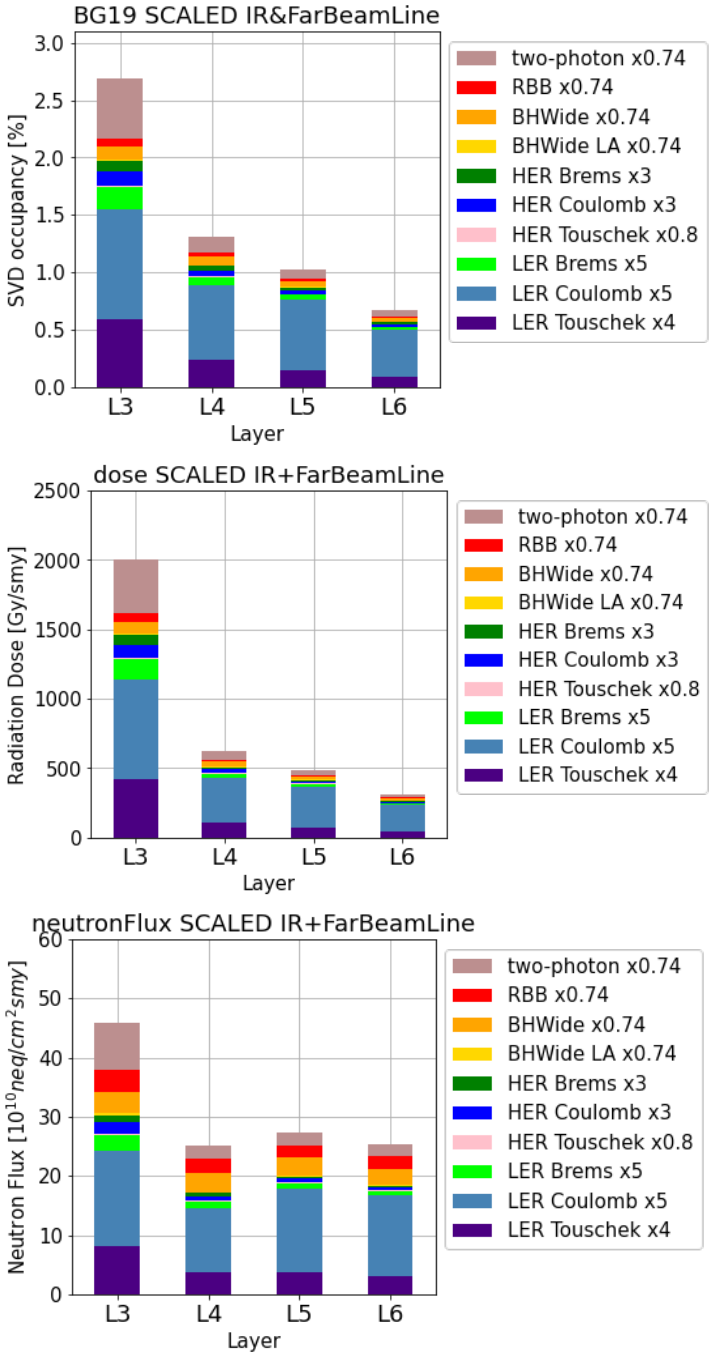


Figure 2.13: Re-calculated occupancy, total ionizing dose and equivalent neutron flux of all the SVD Layers with Data/MC factor for luminosity background being 0.74. Compared to the result without re-scaling luminosity background, a reduction of about 10% is observed in total occupancy, dose and neutron flux for layer 3 sensors.

Chapter 3

Specifications of TFP-SVD prototypes

As described in Section 1.7, a new sensor TFP-DSSD and a new front-end readout chip SNAP128 was developed for the TFP-SVD project. Currently, the first prototype of the sensor and chip prototype has been produced and delivered to KEK (Tsukuba), Japan, followed by a performance evaluation that is reported in this thesis. In particular, the first version of SNAP128 is named as SNAP128A.

This chapter shows the necessary specifications of the first prototype TFP-DSSD sensor and SNAP128A that are used in the performance evaluation.

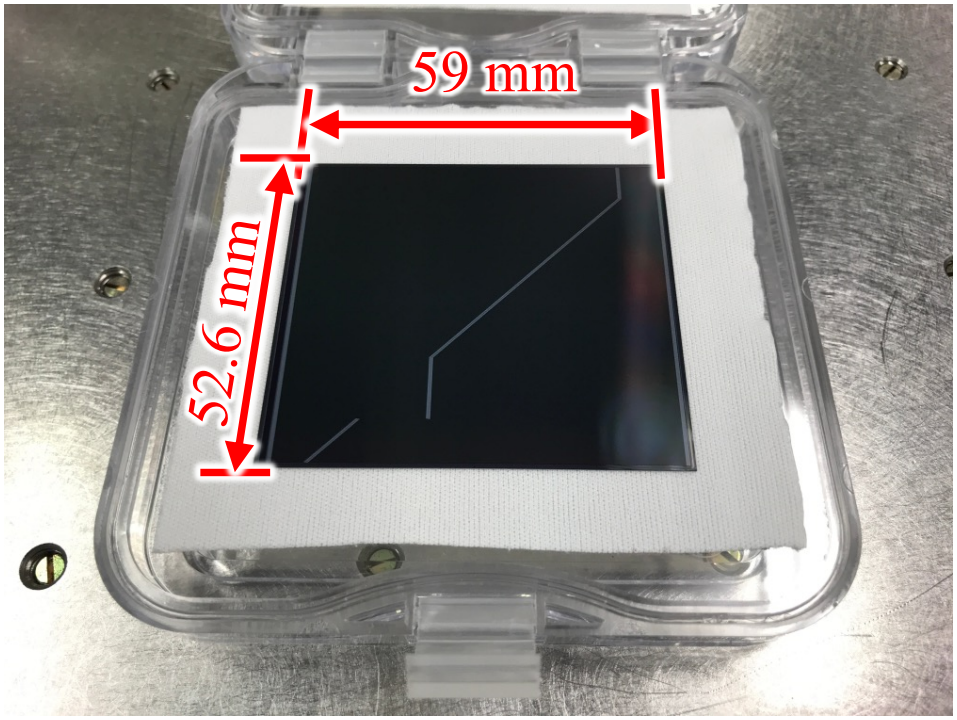


Figure 3.1: Prototype TFP-DSSD sensor (P-side)

Quantities	Value
Sensor dimension	52.6 mm × 59.0 mm
Sensor active area	51.2 mm × 57.6 mm
Sensor thickness	140 µm
Readout strips (P-side)	1024
Readout strips (N-side)	768
Readout pitch (P-side)	50 µm
Readout pitch (N-side)	75 µm
Inter-strip capacitance (P-side)	8.0 pF
Inter-strip capacitance (N-side)	6.5 pF
Strip width	14 µm
n-type substrate	6 kΩ/cm
Floating strip	No
Readout coupling	AC
Bias resistance	10 MΩ
Full depletion voltage	< 15 V
Manufacturer	Micron Semiconductor

Table 3.1: Properties of the first prototype TFP-DSSD sensor.

3.1 Specification of prototype TFP-DSSD sensor

The first prototype TFP-DSSD sensor was fabricated by Micron Semiconductor in England. A photo of the sensor is shown in Fig. 3.1. The design of the prototype sensor is a dimension of 52.6 mm×59.0 mm and 140 µm thickness. And the active area, which the readout strips cover, is 51.2 mm × 57.6 mm. The number of the readout strips and strip pitch is 1024 (768) and 50 µm (75 µm) for the P (N) side, without floating strips. The inter-strip capacitance between two readout strips is expected to be about 8.0pF and 6.5pF in the P strip and N strip, respectively, according to measurements of other silicon strip sensors [37]. Properties of prototype TFP-DSSD sensor are summarized in Table 3.1.

The layout of the TFP-DSSD sensor in the P-side and N-side is shown in Fig. 3.2. Each doped strip is AC coupled to an aluminum readout strip. The analog input channels of the front-end ASIC are electrically connected to the aluminum readout strips. The doped strips are connected to the bias ring via a 10 MΩ bias resistor. This resistor on the one hand makes sure that all strips are electrically connected such that the electrical potential of each strip is the same. On the other hand, the resistance is enough large that the charge collected by each strip does not go to the bias ring, but goes to the readout ASIC inputs via the AC-coupled aluminum layer.

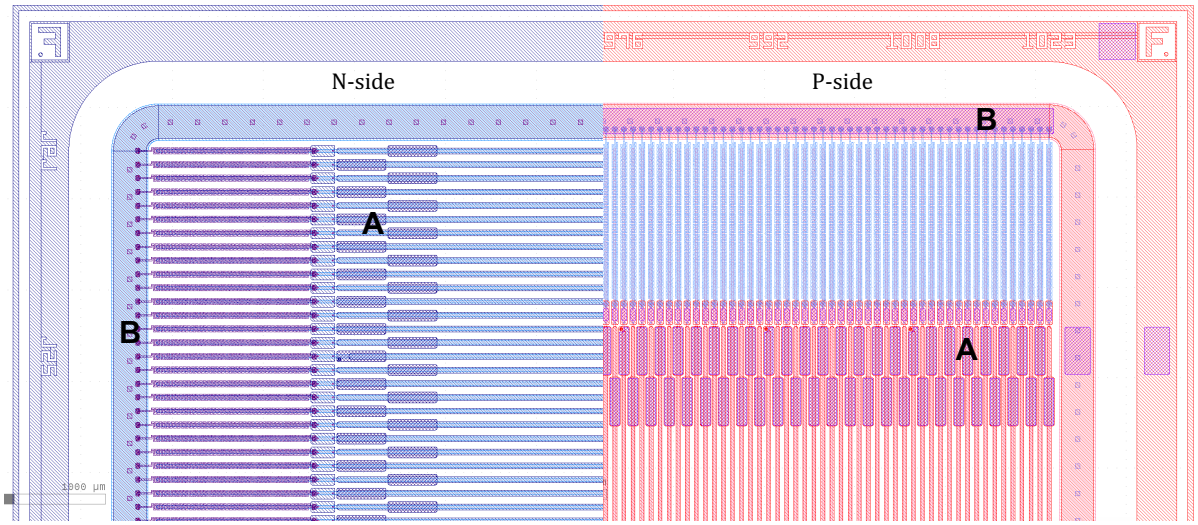


Figure 3.2: Layout of TFP-DSSD sensor. The left side shows the N-side strips while the right side shows the P-side strips. "A" are bonding pads that are connected to the aluminum strips and are used for the wire-bonding connection to the readout chips. Each aluminum strip is AC coupled to an doped strip behind. "B" is the bias ring. The purple area in the layout is not masked by passivation and can be electrically connected to outside devices via the wire bonding.

3.2 Specification of SNAP128A front-end ASIC

SNAP128A is produced using the 180 nm Complementary Metal Oxide Semiconductor (CMOS) technology. Figure 3.3 shows the outlook of the chip, with a dimension of 5.945 mm×6.120 mm. On the left side of the chip are three columns of wire bonding pads. The pads in the most left column are inputs for the power supply of analog circuit and outputs for the monitoring signals. The pads in the inner two columns are inputs of the analog signal from the sensor strips. The channel order of the bonding pads are in a zigzag arrangement. The pads on the right side of the chip are inputs for the digital power supply and inputs and outputs for the digital signals. Six power inputs are supplied to SNAP128A, with four are for the analog circuit: AVDD (+0.9 V), VM (+0.2 V), AGND (0 V) and AVSS(-0.9 V), and remaining two for the digital circuit: DVDD (+0.9 V) and DVSS (-0.9 V).

The block diagram for data processing in SNAP128A is shown in Fig. 3.4.

The input signal is firstly processed by the usual structure of a Charge Sensitive Amplifier (CSA) and a CR-RC shaper. The CSA and shaper need to process both positive and negative signals because SNAP128A reads out the signal from both P-side and N-side of the DSSD sensor. Figure 3.5 shows the simulated shaper output, with $10,000e^-$ input charge and 12 pF detector capacitance. The simulation is based on the schematic model, which means that the parasitic capacitance and resistance from the CMOS is not taken into consideration. The output of the shaper can be monitored using an output pad on the chip (MONOUT_CR_RC). The signal only from one selected channel can be output. The channel is selected by an internal register which is written by the slow-control access to the chip.

A comparator is located just after the CR-RC shaper. In the comparator, the shaper output

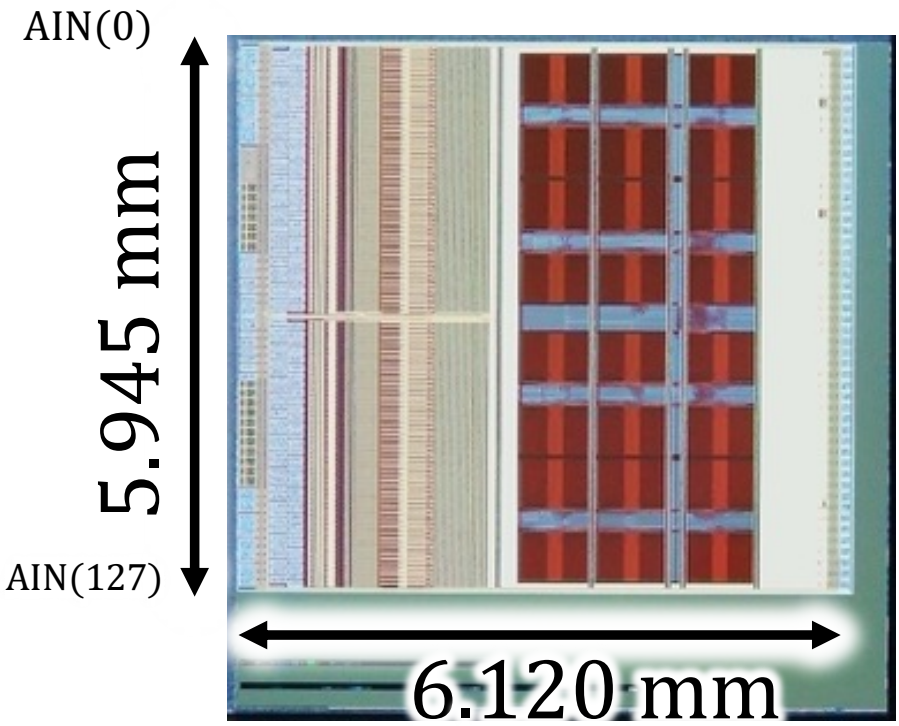


Figure 3.3: SNAP128A.

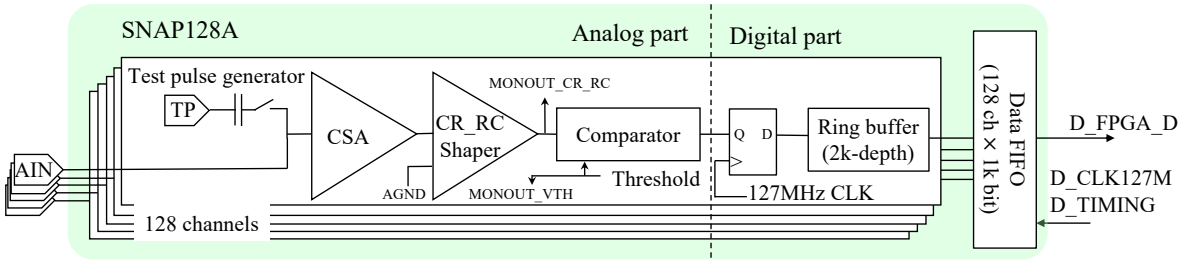


Figure 3.4: Block diagram of signal process in SNAP128A

is compared with a threshold voltage, which is determined by the external input voltage and internal 8-bit Digital-to-Analog Converter (DAC) circuit. The comparator output gives the binary hit information whether the signal is above or below the threshold. This scheme is called "binary readout" as shown in Fig. 3.6. In this thesis, this threshold is named as "comparator threshold". The comparator threshold can be monitored by an output pad on the chip (MONOUT_VTH). The same as MONOUT_CR_RC, only one channel selected by the slow-control can be monitored. The comparator has two selectable polarities such that it outputs logic-high when the shaper output is over (below) the threshold for the positive

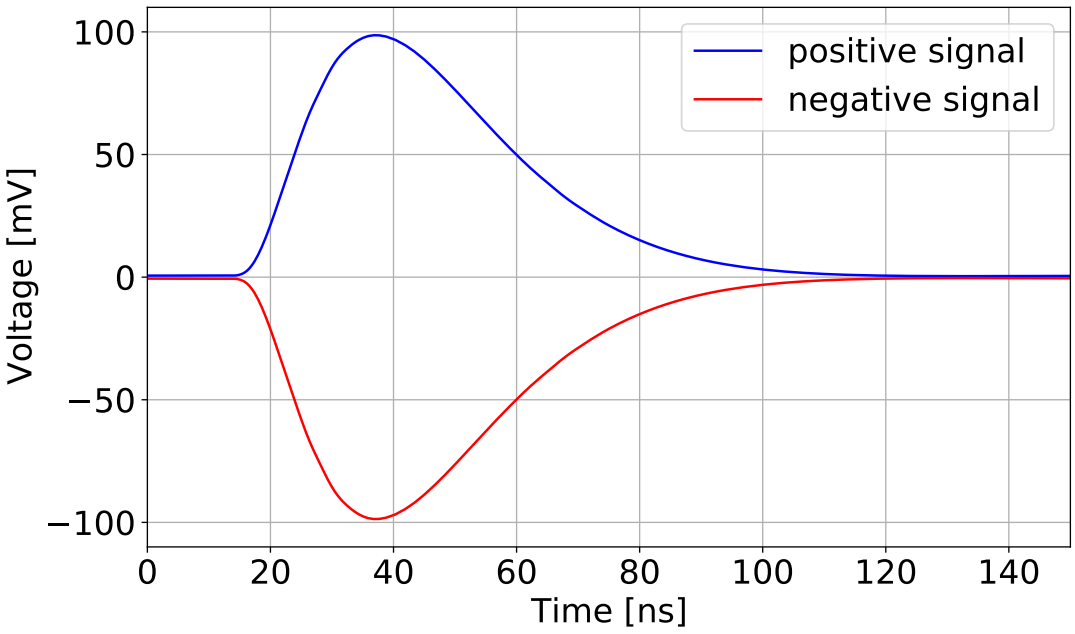


Figure 3.5: Shaper output of SNAP128A in simulation

(negative) signals. The comparator output is sampled by 127 MHz clock and the sampled 127 Mbps binary information is stored in the ring buffer. In this thesis, each sample is named as a "frame". The ring buffer has a depth of 2048. This offers a maximum trigger latency of 16 µs.

Upon the arrival of the Belle II Level-1 trigger signal, continuous frames with selectable length (L) and latency are output from all 128-channel ring buffers. The 128 channel $\times$ L frame data are recorded in a 128 channel $\times$ 1024-depth FIFO (First-In First-Out). The 128-channel hit information from the FIFO output is serialized and to be transmitted together with 14-bit header data from a differential output port (D_FPGA_D) with 127Mbps data rate. D_FPGA_D is a Low-Voltage Differential Signaling (LVDS) output. The data structure of SNAP128A output is shown in Fig. 3.7. At first it outputs a 3'b110 delimiter followed by 1-bit error flag and the least significant 10-bit address in the ring buffer where the first frame (frame 0) data was stored. Then, SNAP128A outputs the hit information in the order of frame until the selected number of frames are output. In each frame, the data in channel 128 is output first and channel 0 comes at the end.

The 127MHz clock of SNAP128A is provided from input pads, D_CLK127M, in the LVDS standard. The trigger signal is input from the D_TIMING pad also in the LVDS standard and should be synchronized with the D_CLK127M clock. The D_TIMING signal determines also the timing of the internal test-pulse generation and soft-reset assertion. For this reason, 3 continuous bits are sent to D_TIMING to distinguish the type of commands, with "100" for trigger, "110" for generating a test pulse, and "101" for the soft reset. At the timing of receiving a "110" pattern, SNAP128A generates an internal test pulse in an analog input with

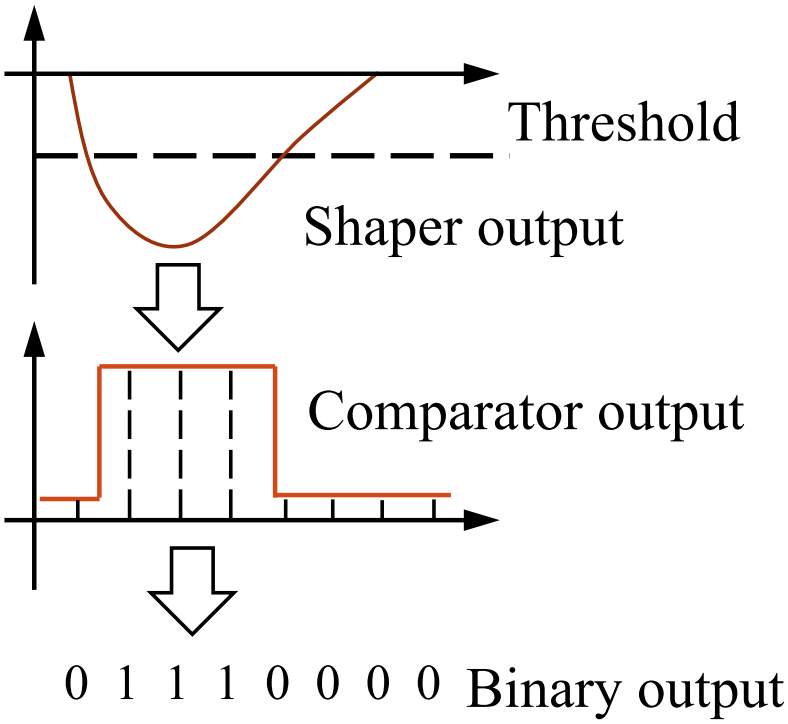


Figure 3.6: Schematic for binary readout. In this example, the comparator is set to negative polarity, such that the comparator output 1 when the shaper output is below the comparator threshold.

Delimiter 3'b110	Error flag (1 bit)	Ring buffer address (10 bit)	Hit data (frame 0) ch. 127~ch.0 (128 bit)	Hit data (frame 1) ch. 127~ch.0 (128 bit)	.....

Figure 3.7: Output hit information (D_FPGA_D) structure of SNAP128A.

an input charge selected among 5,000, 10,000, 15,000, or 20,000 electrons. The input charge and the analog channel is selected by slow control registers. Different from the hardware reset signal, the soft reset signal only resets the error flag, data FIFO and ring buffer pointer to initial position, while leaving the registers for slow control untouched.

The slow control (register access) for SNAP128A is performed using two signals, D_MSCK and D_MSIO. The former one is the clock signal and the latter one is the data signal. Given the low frequency of D_MSCK, both D_MSCK and D_MSIO are single-end singals in the 1.8V Low Voltage CMOS (LVCMOS) standard. D_MSIO is a bi-directional signal with both write-in and readout signals integrated. D_MSCK and D_MSIO signal pair is a Inter-Integrated Circuit bus (I^2C-bus) and multiple slave chips can be controlled by one FPGA. An connection example is shown in Fig. 3.8, with both D_MSCK and D_MSIO signal branch at the front of each slave chip. The 8-bit chip address for each SNAP128A chips is assigned by connecting 8 bonding pads on the digital side to DVDD or DVSS. An example of register readout is shown in Fig.

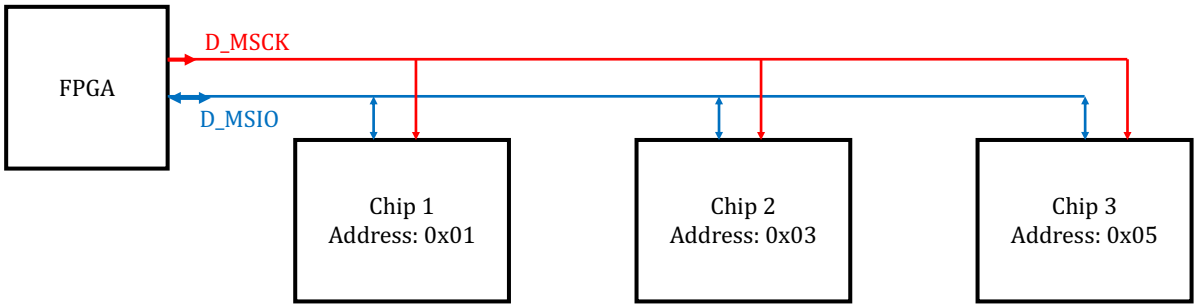


Figure 3.8: Structure of slow control connection for multiple slave chips.

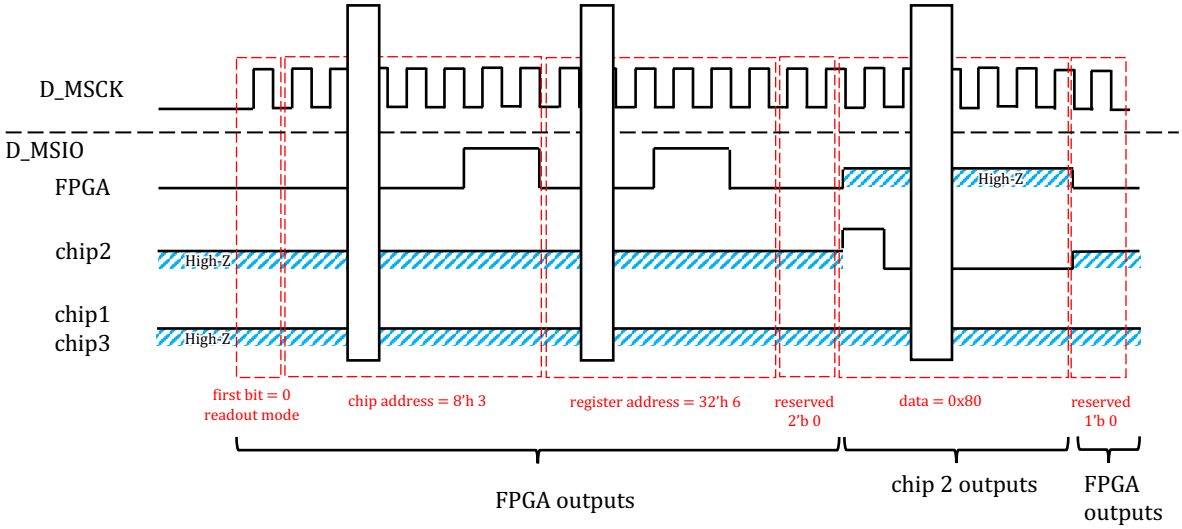


Figure 3.9: D_MSCK and D_MSIO signal when readout one register from one chip.

3.9. D_MSCK is kept at logic low by FPGA when no slow control is performed. SNAP128A samples the D_MSIO signal at the rising edge of D_MSCK. The first bit represents whether the access is the read mode (logic low) or the write mode (logic high), followed by 8-bit chip address and 32-bit register address. In the the read mode as shown in the figure, after the reserved bits, the D_MSIO output from the FPGA and other chips with different chip addresses turn to high-impedance (high-Z) status and only the target chip outputs the value from the register with the specified address. In the write mode, after the chip address, only the target chip continues receiving the remaining slow control commands and write the value to the specified register. If the chip address output from the FPGA is 0xFF, the specified register of all slave chips are open for write-in. This broadcasting function is used for configuring multiple chips at the same time.

Chapter 4

Performance evaluation of SNAP128A

The first prototype SNAP128A was delivered to KEK (Tsukuba), Japan in April 2021. This chapter describes the setup of the evaluation platform and the evaluation results.

4.1 Evaluation setup and check points

The photo and corresponding block diagram of the evaluation system is shown in Fig. 4.1. There are three main components in this platform: a PC, a Field-Programmable Gate Array (FPGA) evaluation board, and a test board on which the chip is integrated. The PC is connected to the FPGA evaluation board with an Ethernet cable for the SiTCP communication, and mainly responsible for controlling the chip and archiving the data received from the chip via the FPGA. The FPGA plays the role of communication bridge between PC and chip: translating the commands from PC to chip and decode the data from chip and send them to PC. The chip is glued on the test board and electrically connected to the board via the wire bonding. The test board provides power supply to the chip and I/O connectors for its

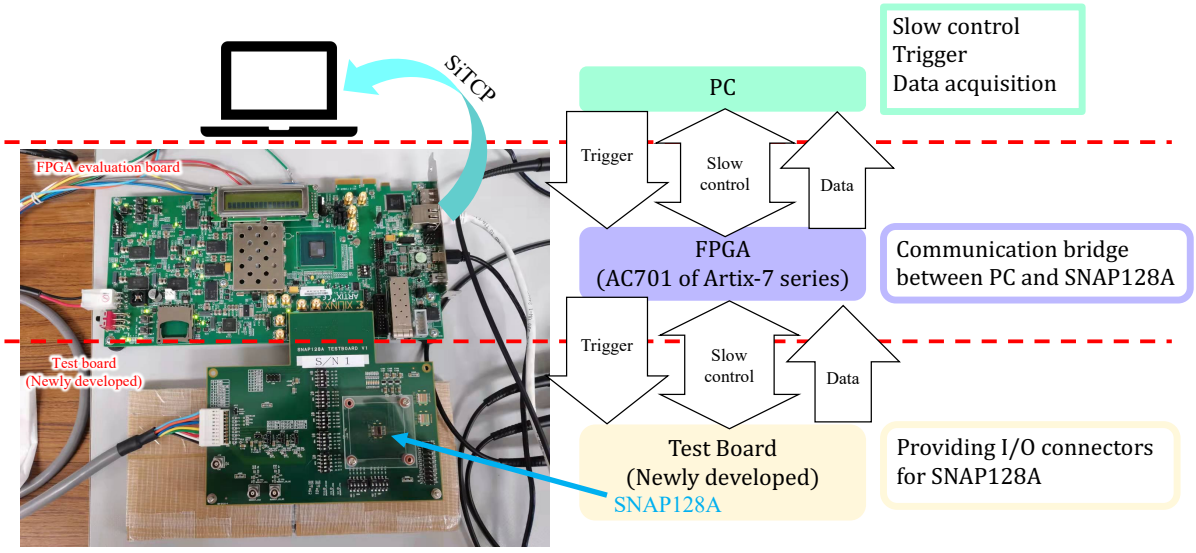


Figure 4.1: Setup of the evaluation platform for SNAP128A chip

communication with the upstream device the FPGA. The electrical connection between the test board and the FPGA is via a FMC connector. A detailed description of this evaluation platform is given in Section 4.2.

In the design phase of SNAP128, the main requirements to this chip can be summarized as the following three aspects, which are also the goals of this evaluation experiment:

- Power consumption smaller than 400 mW/chip.
- Capability to detecting both positive and negative signals
- Pulse width of shaper output smaller than 100 ns
- Pulse height of shaper output comparable to the simulation result
- Noise smaller than 800 electrons with detector capacitance at 15 pF
- Digital functionalities of the chip（signal output and slow-control）

The maximum power consumption is limited by the cooling system. The pulse width limit comes from the requirement that the TFP-SVD can tolerate a hit rate of $10\,\mathrm{MHz/cm^2}$. The noise limit comes from the requirement that the minimum S/N for seed strip in one cluster larger than 5. The detailed information and calculation can be found in Section 1.7.

After setting up the evaluation platform and confirmed its operation, the power consumption of the chip was measured (Section 4.3). Evaluation of pulse width, pulse height and noise characteristics require the reconstruction of the shaper output waveform from the comparator output scanning the comparator threshold. The reconstruction is performed by developed S-curve method. The details of the method is described in Section 4.4. To perform the measurement of all 128 channels within a reasonable time, the measurement is automated as described in Section 4.5 and measurement results of pulse width, pulse height and noise are shown in Section 4.8. In the characterization of the chip, some issues of the prototype chip were revealed. One of the big issues is the positive signal saturation, which is described in Section 4.6.

At the end of this chapter, a summary of the evaluated performance and possible improvements of SNAP128A is presented in Section 4.9.

4.2 Development of evaluation platform

4.2.1 Design and assembly of SNAP128 test board

The SNAP128 test board is newly developed for the performance evaluation of the chip. The full schematic and layout design of the test board is shown in Appendix A. In this section the key points of the design are described.

A simplified schematic of the test board is shown in Fig. 4.2. The power supply to SNAP128A on this test board is 1.8 V, 1.1 V, 0.9 V and 0 V for AVDD (DVDD), VM, AGND and AVSS (DVSS), instead of the ±0.9 V power supply to VDD and VSS as designed. The 0 V supplied to analog and digital circuit are connected, while the 1.8V power is supplied to analog and digital circuit separately. The 35 analog channels of SNAP128A are connected to capacitors with various capacitance to measure the the detector capacitance (C_{det}) dependence of the chip performance. In total, 35 capacitors are accommodated on the PCB, and 7 of

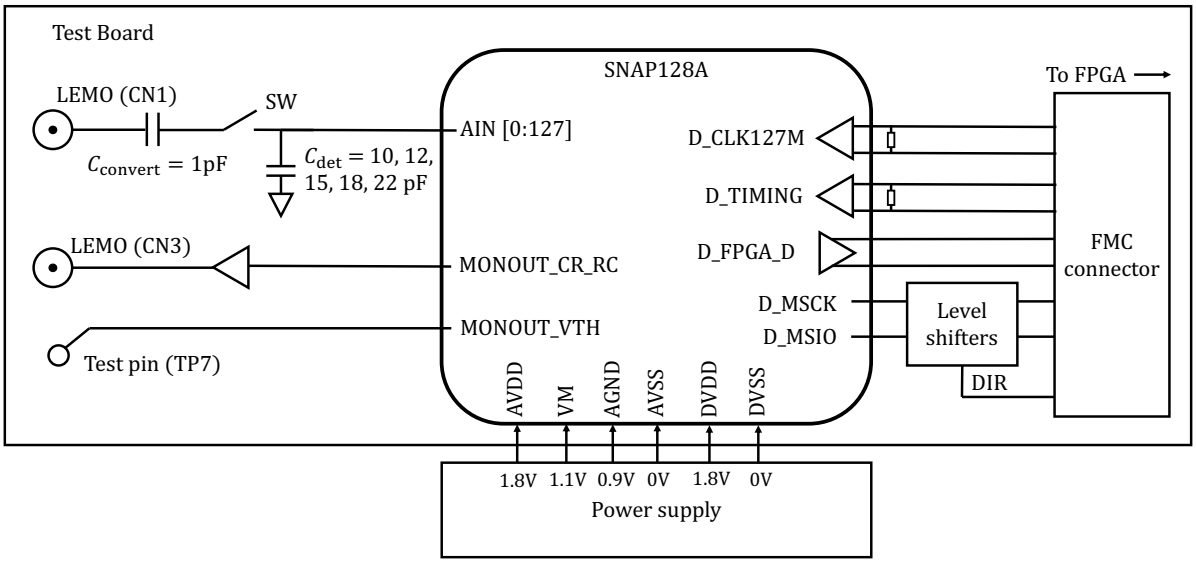


Figure 4.2: Simplified schematic of the SNAP128A test board.

them have the same capacitance either 10 pF, 12 pF, 15 pF, 18 pF or 22 pF. However, due to narrow space nearby the chip and the difficulties in wire bonding, only 5 capacitors for each capacitance could be connected to the analog inputs of SNAP128A. In addition to the internal test pulse generated inside SNAP128A, external test pulse can be injected via a LEMO connector, with a 1 pF capacitor C_{convert} in between. The shape of the external test pulse is supposed to be a step signal. Assuming the signal amplitude of U, the signal charge Q input into the chip is $U \cdot C_{\text{convert}}$. The CR_RC shaper output of a selected channel can be monitored by the oscilloscope through another LEMO connector and the comparator threshold of that channel to be measured via a test point. For the digital side, the LVDS differential clock signal D_CLK127M and trigger signal D_TIMING are connected to an FMC connector, which is connected to the FPGA evaluation board, with 100 Ω termination resistor. The data output D_FPGA_D in the LVDS standard is connected to the FMC connector. The termination of the signal is in the FPGA input. Since the voltage levels of the FPGA banks (2.5V)* and SNAP128A (1.8V) are different, level shifters are mounted between SNAP128A and the FPGA for single-ended signals like slow control clock (D_MSCK) and data (D_MSIO).

The layout design and production of test board is done by GNomes Design Co., LTD. After the delivery, one SNAP128A chip is glued on the test board. Electrical connection between the chip and the test board is done by wire bonding. The K&S 4523A Digital manual wire bonder is used in the assembly. Photos of the test board after assembly is shown in Fig. 4.3, with the left one being the overview of the whole test board while the right one is zoomed around the chip area.

*According to reference [38], for the FPGA on AC701 evaluation board, internal termination resistor is available only when the power supply of the corresponding I/O bank is set to 2.5 V.

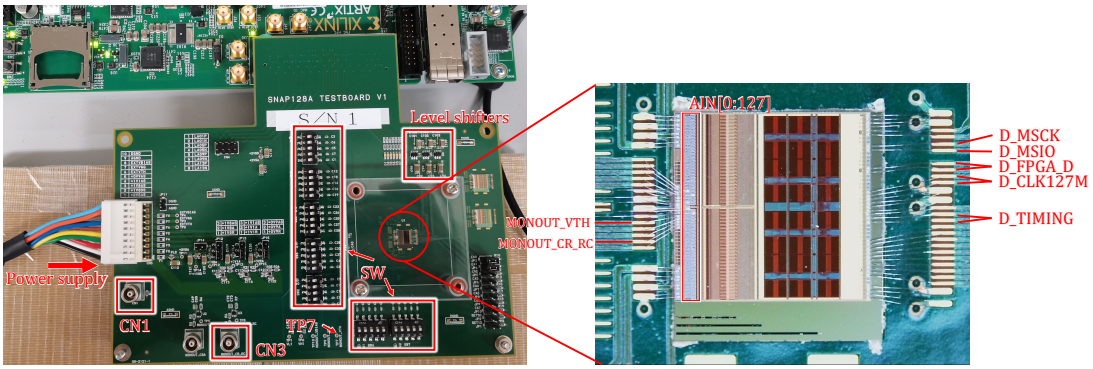


Figure 4.3: Photo of the test board. The left one is the overview and the right one is the zoom of the region around chip.

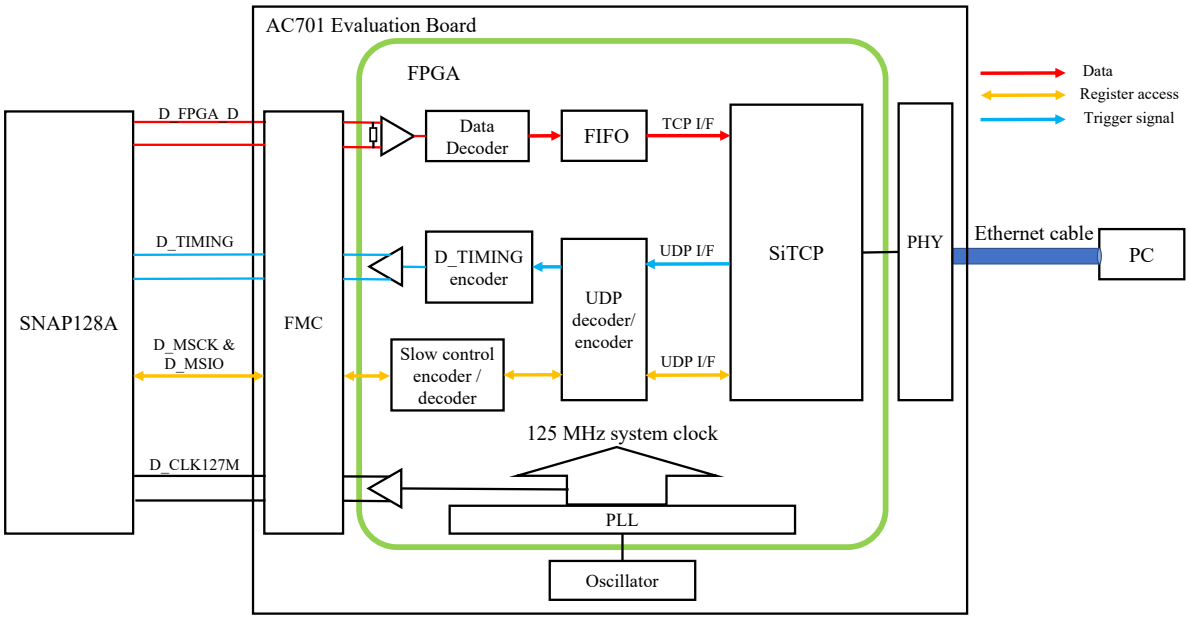


Figure 4.4: Structure of readout firmware

4.2.2 Development of readout firmware

The FPGA plays the roles of communication bridge between SNAP128A and PC. The AC701 Evaluation Board by Xilinx^{TM}, which accommodates Artex-7 FPGA (XC7A200T-2FBG676C), is chosen for its large number of high speed general purpose I/O resources via the FMC connector, enabling the FPGA connecting to at least 14 SNAP128A chips simultaneously.

The firmware of the FPGA was developed. The block diagram of the firmware is shown in Fig. 4.4. While 127MHz clock is planned to be used in the experiment, the 125MHz clock was used in the test setup because it can be generated by the Phase Lock Loop (PLL),

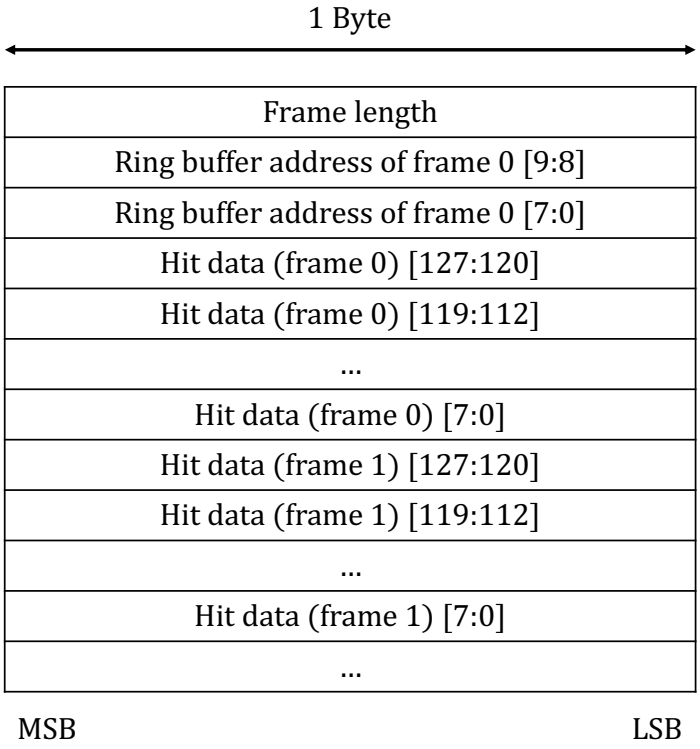


Figure 4.5: Data structure sent to PC via the TCP connection

from the 200MHz Oscillator (`OSC`) on the AC701 evaluation board. This clock signal is also sent to the SNAP128A chip as the system clock in the chip. The communication between the FPGA and the PC is done using the `SiTCP` [39] library, with both Transmission Control Protocol (TCP) and User Data Protocol (UDP) communication protocols available. The TCP is used in transmitting data from the FPGA to PC and UDP is used in issuing trigger signals and accessing registers. To improve the reliability of UDP communication, the UDP decoder returns a UDP packet to PC to acknowledge the packet reception at every transmission from the PC.

The `Data Decoder` module starts decoding the SNAP128A output after detecting the hear "110" in D_FPGA_D signal. The 1-bit output signal is paralleled into 8-bit data and stored in the `FIFO`. The `Data Decoder` stops decoding after receiving the expected length of data frames. The expected length is set in advance and is the same as the length of frames to be output from SNAP128A upon receiving one trigger signal. The `SiTCP` module reads in the data stored in `FIFO` byte by byte and send them to the PC. The data structure sent to the PC is shown in Fig. 4.5.

The `D_TIMING encoder` module sends D_TIMING signals with a specified interval for specified number. There are four commands in the `D_TIMING encoder` module: "trigger", "test pulse". "soft reset" and "test pulse + trigger". In the "test pulse + trigger" command, the encoder module sends the test pulse signal (110) followed by the trigger signal (100) 256 clocks after. The interval, number, and command of the D_TIMING signals are selected by the slow-control access to the FPGA using the UDP communication. In continuous operation, the

FPGA keeps sending triggers and receiving data from SNAP128A. The Ethernet communication sometimes becomes unstable and in that case the data in the `FIFO` are not read out. If the triggers are kept sent to the SNAP128A, the `FIFO` gets overflow and the data is lost. To avoid this problem, the `D_TIMING encoder` stops sending the trigger if the `FIFO` becomes almost-full. When the internet connection is recovered and a free space is made in the `FIFO`, the encoder resumes to send the trigger signals.

When a register access request is on, the PC firstly sends the request type (write or read), target chip address and register address information to the FPGA. This information is decoded by the `UDP decoder` module and sent to the `Slow control encoder / decoder` module. After that, the `Slow control encoder / decoder` encodes this information into D_MSIO signal and send it to the SNAP128A. If the access is "write", the module sends the write value to D_MSIO. If the access is "read", the module receives the read value from the D_MSIO and sends it to the `UDP encoder`. The `UDP encoder` sends this value to PC afterwards. In this register access process, the corresponding D_MSCK signal is also generated by the `Slow control encoder / decoder` module. The slow control waveform is shown in Fig. 3.9.

4.2.3 Development of software on the PC

The software running on the PC is developed to control the chip using the developed firmware mentioned above. This software mainly contains three classes: `Digitalregister`, `SNAPchip` and `dataTaking`.

The `Digitalregister` class mainly contains two method: `write_value()` and `read_value()`. Both of them generate the corresponding register access information, including the chip address and register address. In in the `write_value()` method case, above information together with the value to write is encoded into the UDP packet and sent to the FPGA. The `read_value()` method firstly send the above information directly to the FPGA and wait for the return packet from the FPGA to get the readout value of the target register.

In the `SNAPchip` class, one `Digitalregister` is generated for each of the registers inside one SNAP128A. The `SNAPchip` class mainly realizes the methods that are possible by one or multiple register access of one chip such as setting the length of frames to be readout upon receiving one trigger, setting the trigger latency and setting the VTH DAC of one specific analog channel.

The `dataTaking` class contains one `SNAPchip` object and can be extended to any number of `SNAPchip` objects if necessary. It realizes the method to send D_TIMING signals and receiving the data by listening the TCP connection with the FPGA. In addition, it initializes the SNAP128A chip(s) to make them ready for data taking. This class is designed for continuous data taking and provides the interfaces of all possible operations of the SNAP128A chips. Any data taking procedures mentioned below in this chapter call methods in this `dataTaking` class instead of the other two classes above.

4.3 Measurement of power consumption

As described in Section 4.2, 4 different powers are supplied to SNAP128A: AVDD (1.8 V), VM (1.1 V), AGND (0.9 V) and DVDD (1.8V). Each power is supplied by one P4K6-4 power supply ((Matsusada Precision)). In addition to voltage supply, the power supply also monitors the output current.

The current consumption in the power lines and power consumption in analog and digital circuits are summarized in Table 4.1. According to the current, the power consumption per chip is measured to be 329 mW, which satisfies the required 400 mW limit.

Power supply	Current (mA) or power (mW)
1.8V digital	97 mA
1.8V analog	43 mA
1.1V analog	70 mA
0.9V analog	0 mA
Power consumed by digital part	174.6 mW
Power consumed by analog part	154.4 mW
Total power consumption	329 mW

Table 4.1: Power consumption of one SNAP128A chip

4.4 Reconstruction of the CR-RC shaper output

4.4.1 Methodology

To measure the pulse height, pulse width, and noise of the CR-RC shaper output, it is required to reconstruct the shaper output waveform using the binary hit information of the comparator output. In this subsection, the methodology of shaper output reconstruction is explained using the negative output from the shaper as an example. Due to a unknown bug in the SNAP128A design, the positive polarity of comparator does not work properly. For this reason, the comparator is set to negative polarity in this thesis so that the comparator outputs the logic high when the shaper output is lower than the comparator threshold.

The waveform is reconstructed using the threshold scanning method as shown in Fig. 4.6. Firstly, we set the comparator threshold V_{TH} at an initial value. Then, 1000 sets of the test pulse (110) and trigger (100) signals are sent to the D_TIMING input to generate the internal test pulses and read out the corresponding data for 1000 times. With these 1000 test pulse events, the hit detection probability under the specific threshold V_{TH} at frame i, $P(V_{\mathrm{TH}}, i)$, is defined as the fraction of the events with the comparator output = H at the threshold and frame. Scanning the threshold from well below the shaper output to well above baseline of shaper output, the probability $P(V_{\mathrm{TH}}, i)$ changes from 0 to 100%. The shaper output at the frame i, $V_{\mathrm{out}}(i)$, is then evaluated as the threshold voltage V_{TH} at the transition, which gives $P(V_{\mathrm{TH}} = V_{\mathrm{out}}(i), i) = 50\%$.

Due to the existence of noise,the transition of $P(V_{\mathrm{TH}}, i)$ from 0 to 100% becomes slow. Assuming the fluctuation of the noise around the output follows a Gaussian distribution, V_{TH} dependence of $P(V_{\mathrm{TH}}, i)$ should be an error function::

$$P(V_{\mathrm{TH}}, i) = \int_0^{V_{\mathrm{TH}}} Gaussian(t|\mu(i), \sigma(i))\, dt = \int_0^{V_{\mathrm{TH}}} \frac{1}{\sqrt{2\pi}\sigma(i)} \exp\left(-\frac{(t-\mu(i))^2}{2\sigma^2(i)}\right) dt \quad (4.1)$$

The shape of $P(V_{\mathrm{TH}}, i)$ as a function of V_{TH} is called S-curve. By fitting the the measured probabilities $P(V_{\mathrm{TH}}, i)$ as a function of V_{TH} with the error function, the center value $\mu(i)$ and standard deviation $\sigma(i)$ are derived. The center value $\mu(i)$ is interpreted as the reconstructed shapre output at frame i, $V_{\mathrm{out}}(i)$ the standard deviation σ represents the noise of the channel.

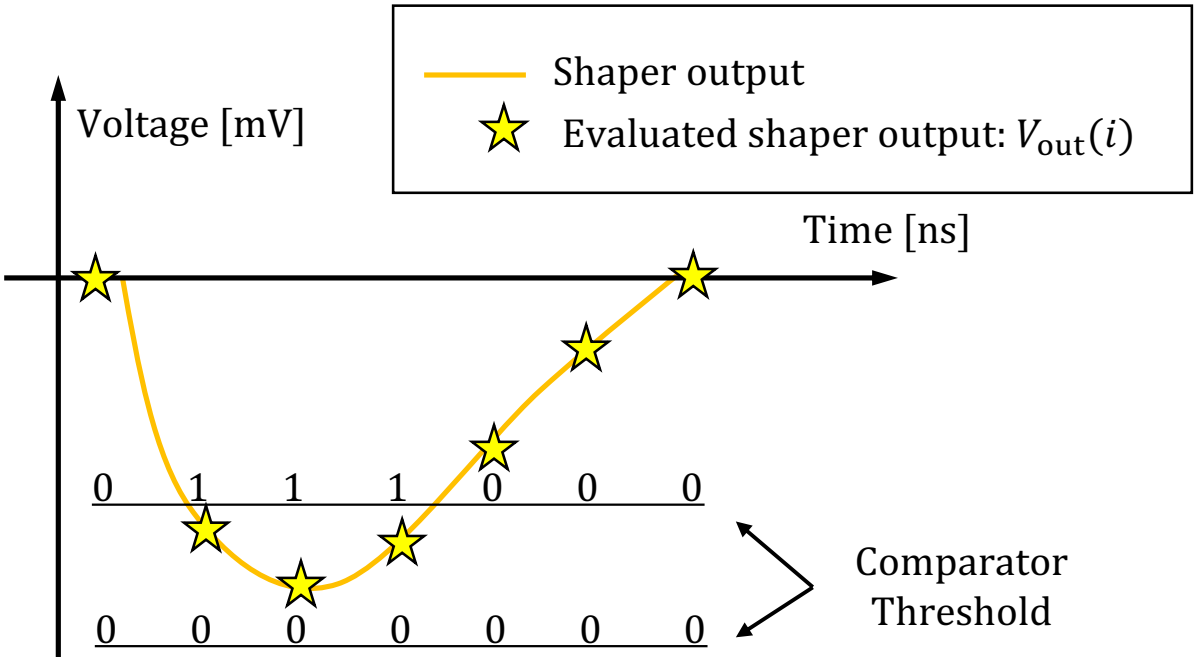


Figure 4.6: Schematic for threshold scanning method to reconstruct shaper output. The yellow star represents evaluated shaper output V_{out} of each frame. The black horizontal line represents the voltage of comparator output and the 0-1 number represents the expected comparator output at the corresponding threshold. By scanning the threshold from well below the shaper output to well above the shaper output baseline, the V_{out} can be determined for each frame. And the waveform is reconstructed by connecting the V_{out} of each frame.

4.4.2 Reconstruction of negative waveform

An example of reconstructed waveform is shown in Fig. 4.7. In the top plot, the data points represent the measured $P(V_{\text{TH}}, i)$ as a function of V_{TH} and the corresponding fitting results with the error function. The error bar of each data point is calculated by

$$\sqrt{\frac{P(V_{\text{TH}}, i) \cdot (1 - P(V_{\text{TH}}, i))}{1000}} \tag{4.2}$$

assuming a binomial distribution with $n = 1000$. In the bottom plot, the reconstructed shaper output, which is the center value $\mu(i)$ as a function of frame i (= time), is shown. The red, green and blue circle represents the frame 0, 6 and 8 whose S-curve fitting is shown in the top plot.

Comparison of reconstructed negative waveform and simulated shaper output under the same input charge (10,000 electrons) and detector capacitance input (12 pF) is shown in Fig. 4.8. The simulation used here is schematic-level without considering the parasitic capacitance and resistance. The pulse widths of the simulated and reconstructed waveforms matches well. The measured pulse height is only about 70% of the simulation. This small pulse height possibly comes from a larger feedback capacitance than designed in the CSA circuit due to

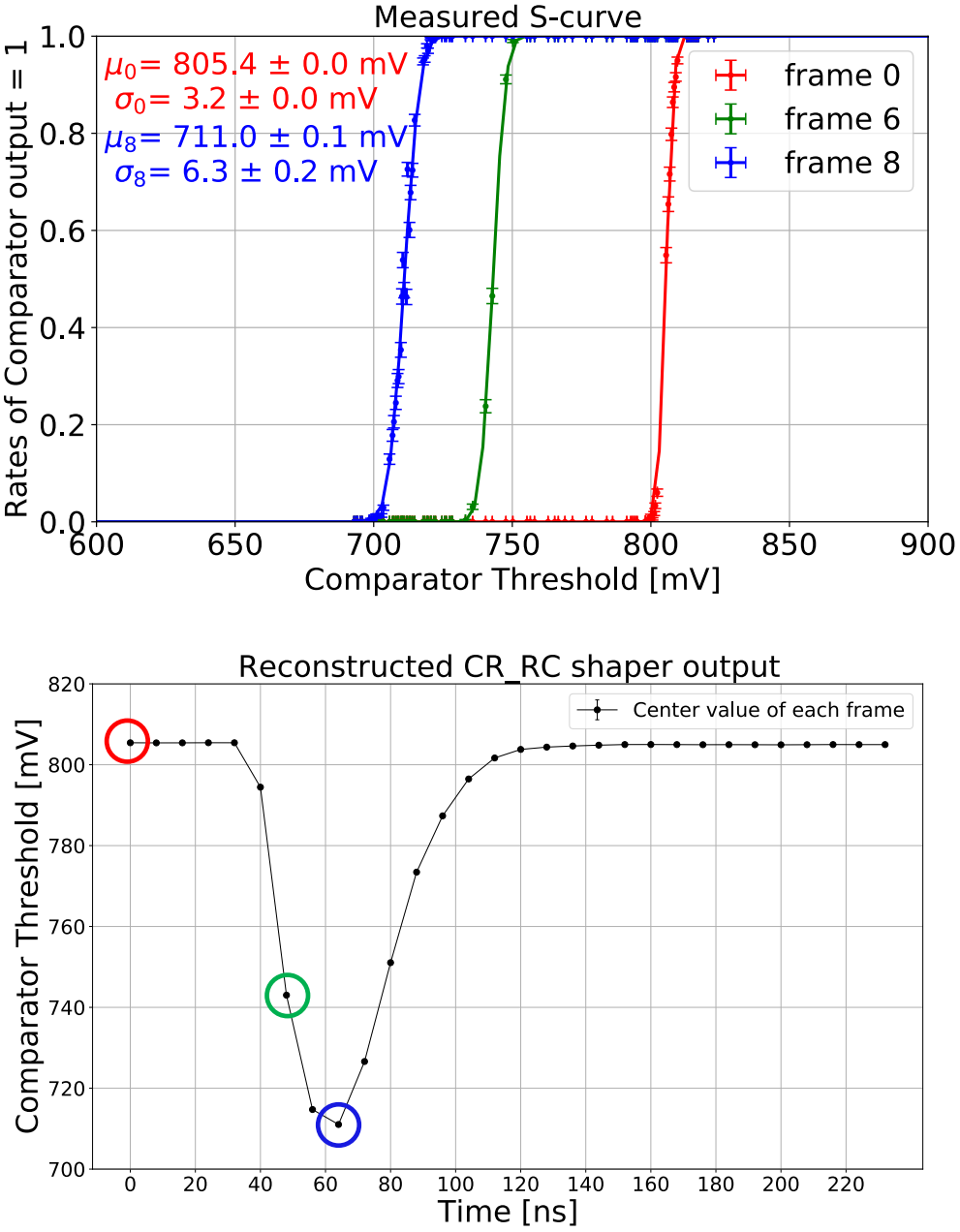


Figure 4.7: Measured S-curve for frame 0, 6 and 8 (top) and corresponding reconstructed waveform (bottom). The top plot shows the measured $P(V_{\mathrm{TH}}, i)$ as a function of V_{TH}, as well as their fitting result to the error function. The bottom plot shows the reconstructed shaper output by connecting the μ of each frame derived in the S-curve fitting (top plot). The red, green and blue circle represents the frame 0, 6 and 8 whose S-curve fitting is shown in the top plot.

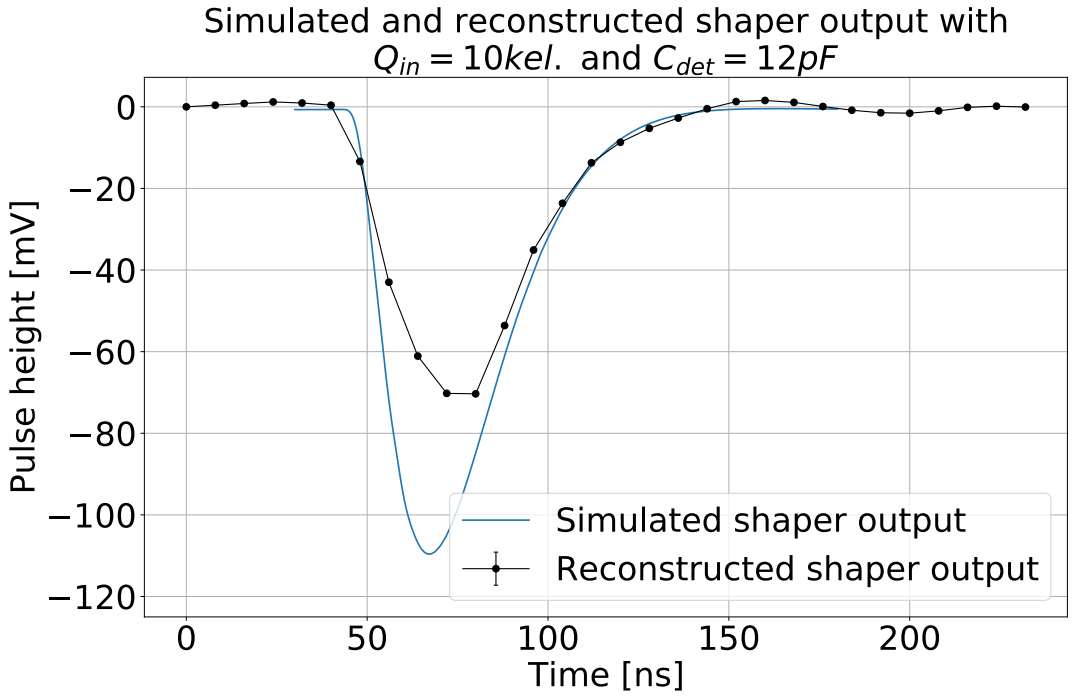


Figure 4.8: Comparison between reconstructed negative waveform (black) and simulated shaper output (light blue). Both of them are measured / simulated with the input charge Q_{in} being 10,000 electrons and detector capacitance input (C_{det}) being 12 pF.

the parasitic capacitance inside the SNAP128A chip. Even though the pulse height is smaller compared to simulation, it is still acceptable in the detector operation.

To quantitatively evaluate the performance of each analog channel, the pulse height, pulse width and noise are measured using the reconstructed waveform. For the negative signals, the pulse height is defined to be

$$\text{pulse height} = |\mu(0) - \mu(i_{\text{min}})| \tag{4.3}$$

where i_{min} represents the frame in which the resulting $\mu(i)$ becomes minimum. The pulse width is defined as

$$\text{pulse width} = t^l_{1/4} - t^e_{1/4} \tag{4.4}$$

where $t_{1/4}$ represents the timing of shaper output being equal to the 1/4 pulse height. The earlier timing is called $t^e_{1/4}$ while the latter timing is called $t^l_{1/4}$. Because the timing with 1/4 pulse height is in the middle of two frames, the linear interpolation of these two frames is used to calculate $t_{1/4}$. The noise is defined as:

$$\text{noise level } [e^-] = \sigma_0[\text{mV}] \frac{Q_{in}\ [e^-]}{\text{pulse height [mV]}} \tag{4.5}$$

where σ_0 is error function sigma at frame 0 derived in the S-curve fitting, in the unit of mV. Q_{in} is the input charge of the test pulse in the unit of number of electrons (e^-).

The measurement results of the pulse width, pulse height, and the noise are described in Section 4.8.

4.5 Automation of shaper output reconstruction

In the threshold scanning, the comparator threshold is measured manually every time changing the DAC setting, due to the bad linearity between comparator threshold and DAC value (to be shown in this section). To automate the threshold scanning process, the calibration of DAC is performed before the threshold scanning by measuring the corresponding voltage of each DAC value for each channel.

4.5.1 Development of calibration system

The block diagram of the calibration system is shown in Fig. 4.9. The PC firstly sets the DAC value of comparator threshold and then the comparator threshold is measured from the MONOUT_VTH monitoring pad by the GL240 logger. The voltage of each DAC is measured for 5 seconds with a sampling frequency of 20 Hz, with 100 datapoints measured for each DAC in total. The measured voltage and the timestamp of measurement are recorded in the SD card of GL240 logger. The timestamp of the start and end time of the 5 second measurement are be stored in PC as well. The PC loops over 8-bit DAC value 0-255 in each analog channel. This measurement takes about 45 hours in total. After the whole measurement, the voltage and corresponding timestamp recorded in the SD card are copied to the PC and analyzed.

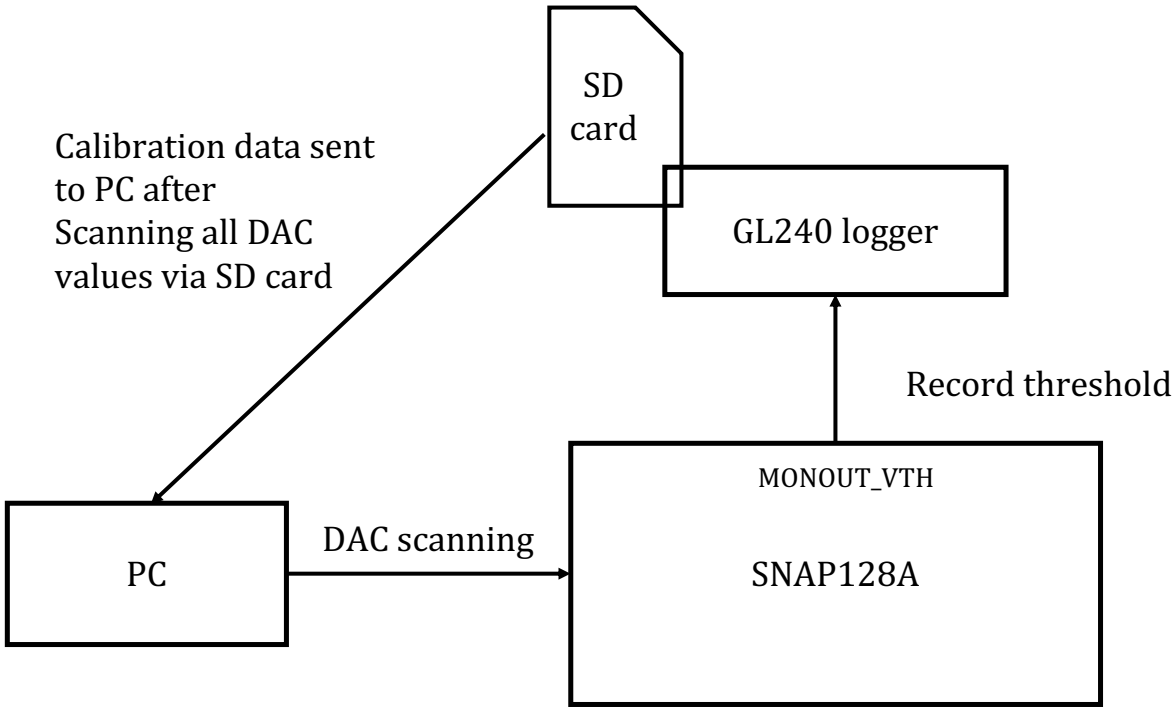


Figure 4.9: Block diagram and of DAC calibration system

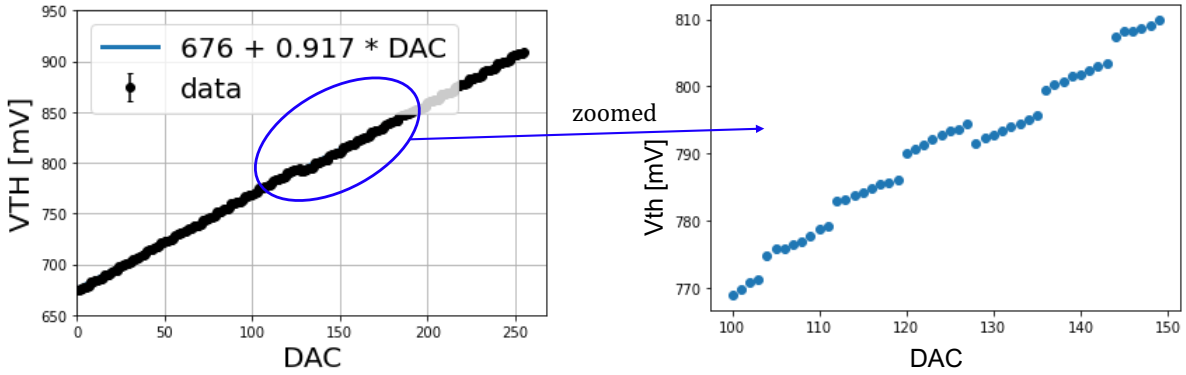


Figure 4.10: Linearity of DAC, which is to be improved

The clock (timestamp) of PC and GL240 should be synchronized before the measurement. However, it is found that the clock in GL240 can deviate from the clock of PC for about 1 second every 24 hours. For this reason, the first and last 1 second data in the 5 second measurement are abandoned to avoid the possible bias from other DAC settings.

4.5.2 Result of calibration

The average value and standard deviation of the measured voltage is calculated. Figure 4.10 shows an example of the average voltage at each DAC. Even though we confirm the linearity of the DAC output in the large scale, the fine structure of the measured DAC voltage is far from satisfactory, in which one can observe that the behaviour of the last 3 bits of DAC is different from the other 5 bits.

Figure 4.11 shows the standard deviation of measured voltage of each DAC. The overall standard deviation is below 0.5 mV, indicating a good stability of DAC.

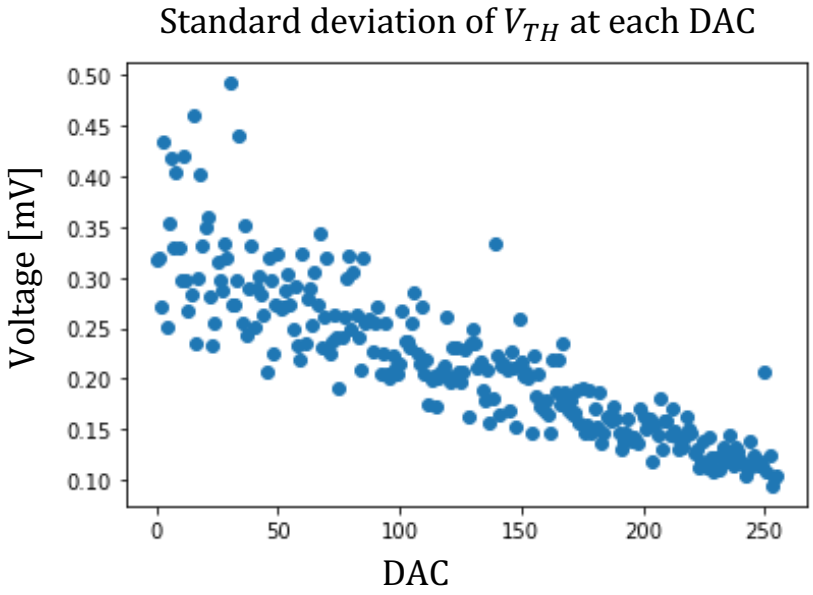


Figure 4.11: Standard deviation of measured voltage at each comparator threshold DAC.

4.6 Investigation of positive signal saturation

4.6.1 Experiment phenomenon

Comparison of reconstructed positive waveform and simulated shaper output is shown in Fig. 4.12. The reconstructed waveform keeps flat at a pulse height of about 20 mV until the waveform decays, indicating that the waveform is saturated. To locate the cause of the saturation problem, the shaper output of analog channel is directly monitored using an oscilloscope. The observed waveform is shown in Fig. 4.13. In the shaper output, such saturation phenomenon is not observed. Therefore, the saturation must happen inside the comparator.

The pulse height as a function of input charge is measured to investigate the area that is affected by the saturation. The result is shown in Fig. 4.14. The positive signal corresponds to the positive input charge and positive pulse height while the negative signals corresponds to negative input charge and negative pulse height. The internal test pulse generated inside SNAP128A and external test pulse generated by a function generator were measured separately. The external test pulse is input into SNAP128A from a LEMO connector on the test board (see Fig. 4.2). The pulse height when input charge is 0 is fixed to 0. In the area about 20 mV below the baseline, the pulse height increase linearly as the increase of input charge. This area is called no saturation area. However, the linear relationship in this area does not pass the origin point and has a positive intercept of 10–20 mV. In the area from -20 mV to +10 mV relative to the baseline, the pulse height still increase linearly as the increase of input charge, but the slope is being relaxed. This area is called partial saturation area. At about +10 mV above the baseline, the signal height is fully saturated and the pulse height does not increase even though the input charge increase. For this reason, this area is called full saturation area.

The slope is affected even at the baseline ($Q = 0$), indicating that with saturation, the noise, and the pulse height could be under-estimated. To improve the problem in the next

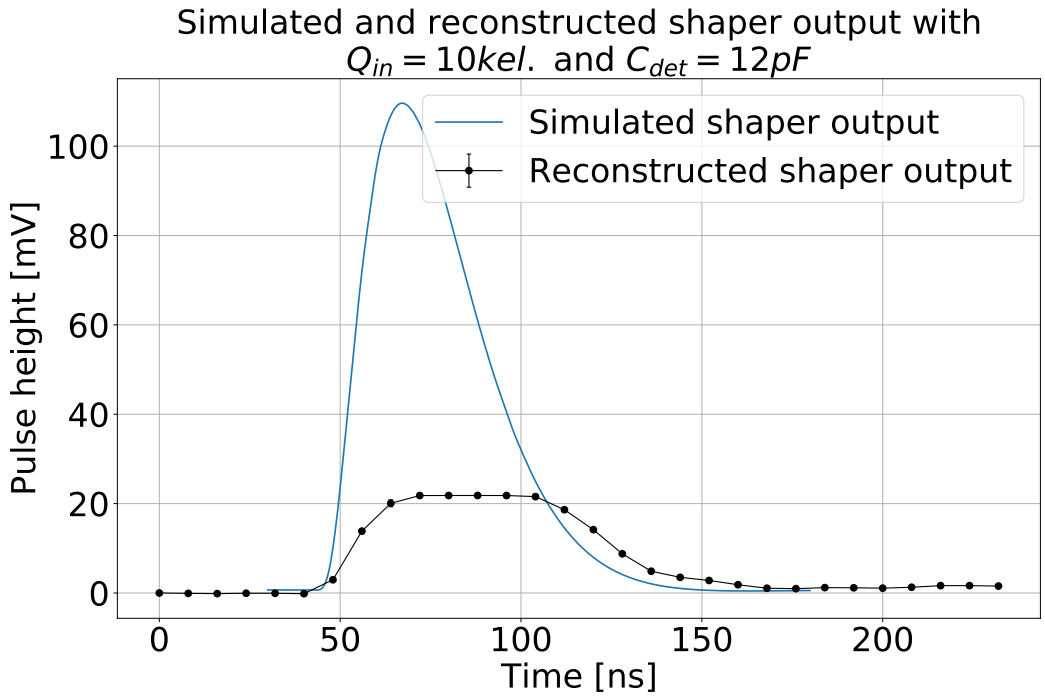


Figure 4.12: Comparison between reconstructed positive waveform (black) and simulated shaper output (light blue). Both of them are measured / simulated with the input charge Q_{in} being 10,000 electrons and detector capacitance input (C_{det}) being 12 pF.

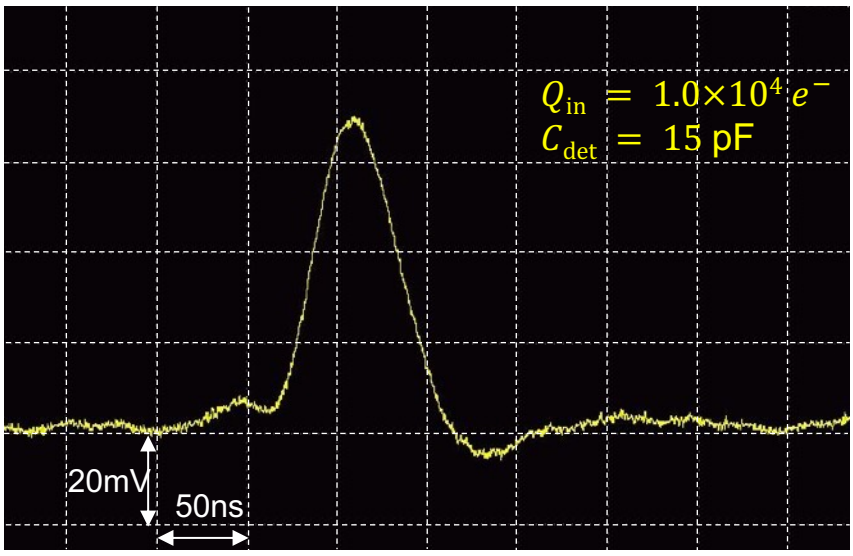


Figure 4.13: Oscilloscope output of positive signal

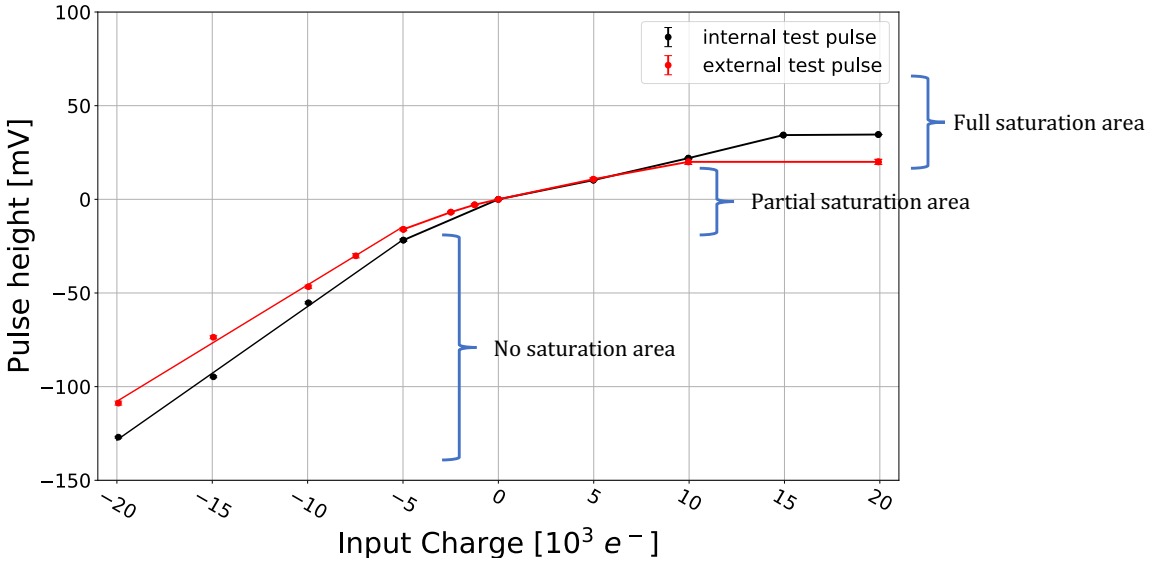


Figure 4.14: Pulse height as a function of input charge. Positive signals corresponds to positive input charge and positive pulse height, while negative signals corresponds to negative input charge and negative pulse height. 0 pulse height represents the baseline of shaper output. The internal test pulse is generated inside SNAP128A while external test pulse is generated by a function generator and input into SNAP128A via a LEMO connector.

prototype production, a simulation study was carried out to understand the mechanism of the saturation and propose counter-measures.

4.6.2 Working principles of Comparator

The schematic of the comparator in SNAP128A is shown in Fig. 4.15. The shaper output and comparator threshold is first input into a amplifier to amplify the differential signal between shaper output and comparator threshold. The differential output of the first stage amplifier is then input into a current mirror for further amplification and converting the output to single-ended signal. The amplifier output is then sent to an Field Effect Transistor (FET) inverter and output from a hysteresis. The FET inverter is part of the high-speed digitizer circuit which improves the slew rate of the comparator output. The hysteresis is to reduce the fluctuation of comparator output.

4.6.3 Simulation study of comparator behaviour

This simulation is carried out using the cadence virtuoso IC617 environment.

Simulated shaper output and comparator threshold are inputted into the comparator to study its response. Unexpected behavior of the comparator is found when the baseline of shaper output is raised by 100 mV. The comparator output when comparator threshold is 70 mV and the baseline of shaper output set to be 0 mV and 100 mV is shown in Fig. 4.16. When the baseline is at 0 mV, the comparator responses as our expectation. It outputs logic

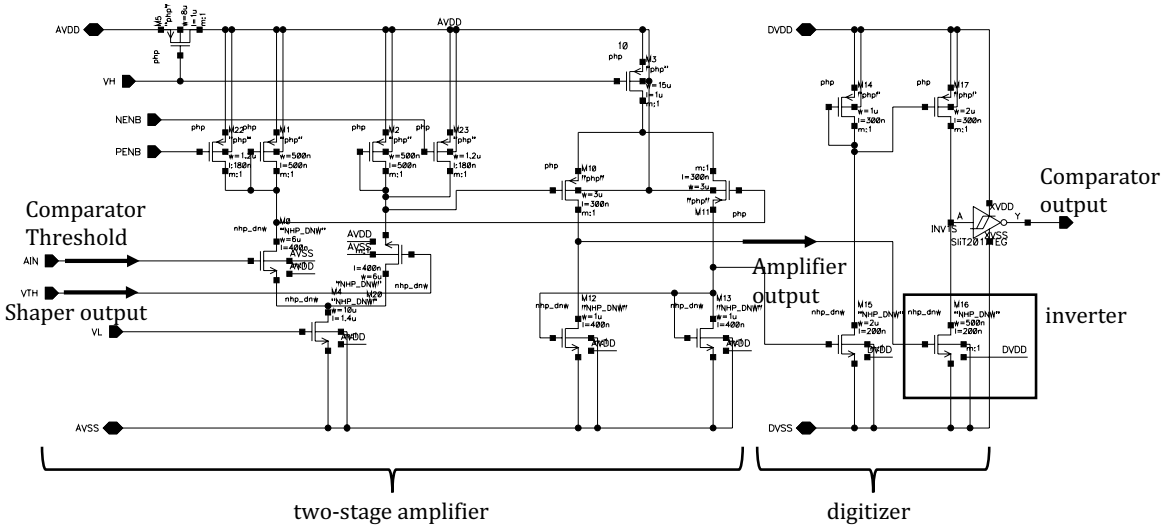


Figure 4.15: Schematic of Comparator in SNAP128A.

high when the shaper output is lower than the comparator threshold and outputs logic low when the shaper output is higher than the threshold. However, when the baseline is raised to 100 mV, the comparator output is kept logic-high even if the shape output is higher than the threshold.

We reconstruct the waveform using the simulated comparator output as what we did to the binary hit data in Section 4.4. The phenomenon mentioned above contains the fact that V_{out} (relative to the shaper baseline) is smaller when shaper baseline is 100 mV compared to that when shaper baseline is 0 mV. Let $P^{0(100)}(V_{\text{TH}}, j)$ be the $P(V_{\text{TH}}, j)$ when shaper baseline is 0 (+100) mV and $V_{\text{out}}^{0(100)}$ be the V_{out} when shaper baseline is 0 (+100) mV. For the frame at 40 ns (labeled as frame j), the top plot in Fig. 4.16 gives $P^{0}(V_{\text{TH}} = 70\text{mV}, j) = 0$, while the bottom plot gives $P^{100}(V_{\text{TH}} = 70\text{mV}, j) = 1$. Given the fact that $P(V_{\text{TH}}, j)$ is the monotonically increasing function of V_{TH}, and the equation $P(V_{\text{TH}} = V_{\text{out}}, j) = 0.5$, one could derive that

$$V_{\text{out}}^{100}(j) < 70\text{mV} < V_{\text{out}}^{0}(j) \tag{4.6}$$

indicating that the reconstructed shaper output when baseline offset is 100 mV is smaller than that when baseline offset is 0 mV at sample j. It is confirmed in the simulation that the comparator output when baseline offset is 100 mV is always not smaller than that when baseline offset is 0 mV, which means

$$P^{100}(V_{\text{TH}}, i) \geq P^{0}(V_{\text{TH}}, i),\ \forall V_{\text{TH}}, i \tag{4.7}$$

resulting in

$$V_{\text{out}}^{100}(i) \leq V_{\text{out}}^{0}(i),\ \forall i \tag{4.8}$$

Eq. 4.8 indicates that the reconstructed shaper output is saturated when baseline is at 100 mV. An example of shaper output reconstruction using the simulated comparator output is shown in Fig. 4.17. It can be observed from Fig. 4.17 that the reconstructed waveform when shaper baseline is 100 mV is saturated.

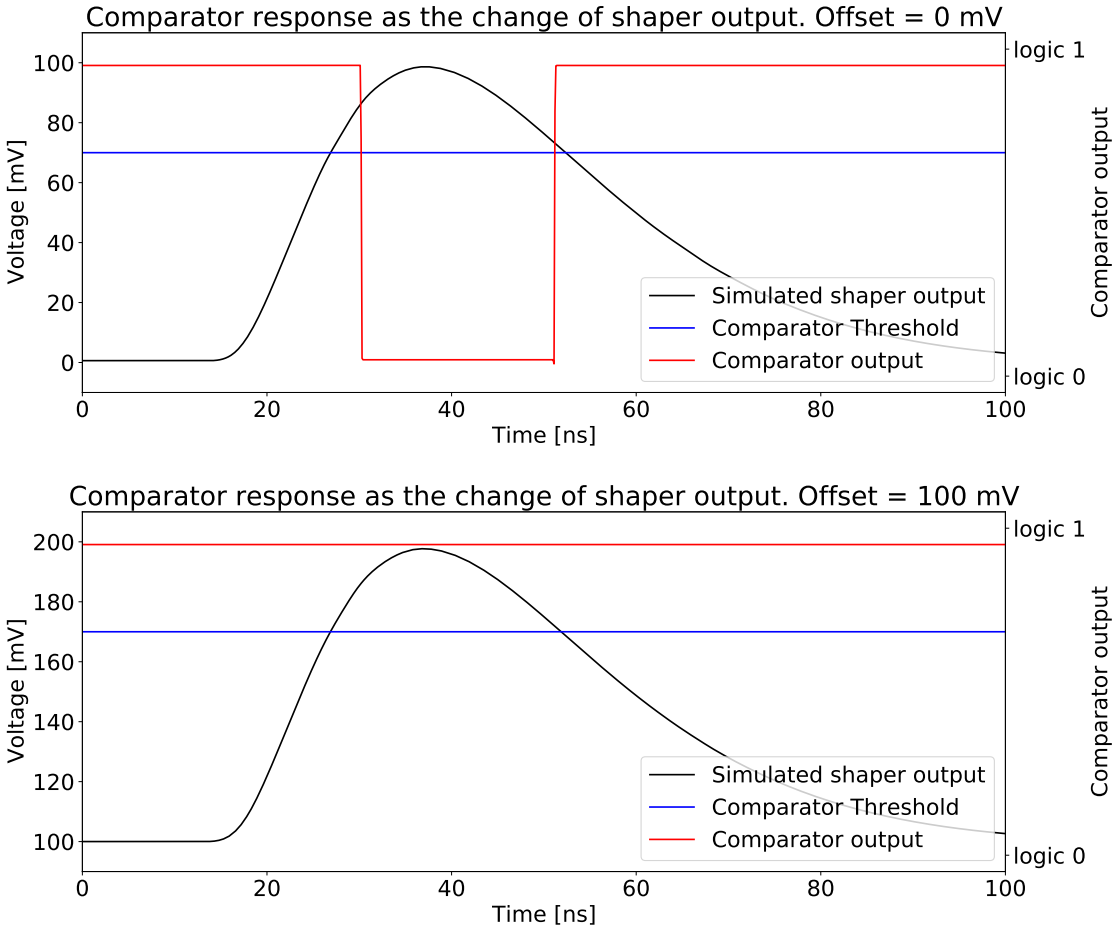


Figure 4.16: Comparator response as the change of shaper output. The comparator threshold is set at 70 mV above the baseline of shaper output, with the baseline being 0 mV (100 mV) for the plot above (below).

This paragraph describes in detail how this waveform is reconstructed. To reconstruct the shaper output, the comparator output is sampled at 8 [ns] $\times\, n,\ (n = 0, 1, ..., 12)$, simulating the measured data sampled with the 125 MHz clock. For each frame, the comparator output is simulated at 20 different comparator thresholds for both offset being 0 mV and 100 mV. The thresholds ranges from -5 mV below the baseline to 95 mV above the baseline, with a step of 5 mV. These voltages are labeled as $V_1, V_2, ..., V_{20}$. $P(V_{\mathrm{TH}} = V_i, j)$ is equal to the comparator output for frame j when $V_{\mathrm{TH}} = V_i$. If $P(V_{\mathrm{TH}} = V_i, j) = 0$ while $P(V_{\mathrm{TH}} = V_{i+1}, j) = 1$, $V_{\mathrm{out}}(j)$ is defined to be $(V_i + V_{i+1})/2$. By plotting $V_{\mathrm{out}}(j)$ as a function of time, the shaper output reconstruction is finished.

As a staged conclusion, the saturation comes from the fact that shaper output does not output logic low even if the shaper output is over the threshold. Further simulation study reveals the possible mechanism of this phenomenon, the relative low amplification factor of the amplifier and a relative high logic transition threshold in the inverter inside the comparator.

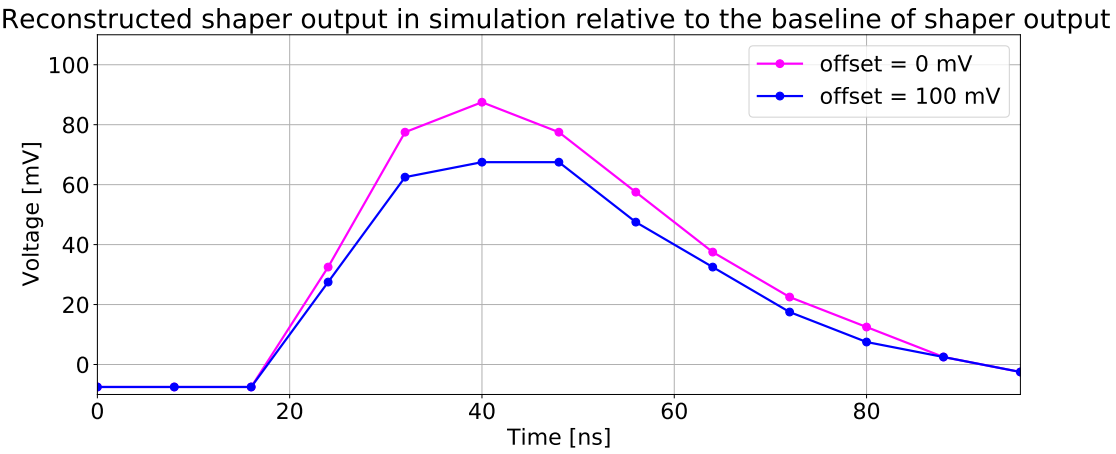


Figure 4.17: Reconstructed shaper output in simulation relative to the baseline of shaper output.

The FET inverter output as a function of the amplifier output, which is also the FET inverter input, is shown in Fig. 4.18. The FET threshold is defined to be the voltage of amplifier output above which the output of comparator transitions from logic high to logic low. The amplifier output raise from 0 mV as the increase of shaper output. It is observed that the maximum amplifier output is only slightly higher than the FET threshold at the peak of shaper output. As the baseline of shaper output raise by 100 mV, which means the common mode of comparator input raise by about 100 mV, the amplifier output decrease even though the differential input of amplifier is the same, and for this reason, the comparator output does not transition from logic high to logic low even if the shaper output is above the comparator threshold.

From the above study, it can be concluded qualitatively that the direct cause of the saturation in the comparator is due to the problem of comparator, keeping output logic high even if the shaper output is larger than the threshold. The reason for the comparator problem lies in the relative low amplification factor for the amplifier and the relative high threshold for FET inverter.

4.6.4 Counter-measures to saturation problem in this experiment

By comparing the maximum amplifier output at different offset of shaper output shown in Fig. 4.18, it was found that the maximum amplifier output is larger for smaller offset of the shaper output. It indicates that the decrease in the baseline voltage of the shaper output could suppress the saturation effect. The chip schematic shown in Fig. 3.4 indicates that the baseline of shaper output is determined by the AGND voltage, which is nominally set to 0.9 V. In this experiment, the AGND voltage can be adjusted by the external power supply.

The reconstructed positive and negative shaper output when AGND is 0.8V is shown in Fig. 4.19. While the saturation phenomenon disappears, ringing after the signal peak is observed in the reconstructed shaper output, which is not observed when AGND is 0.9 V. This ringing is not observed in the simulation and the cause is still under investigation. To avoid both

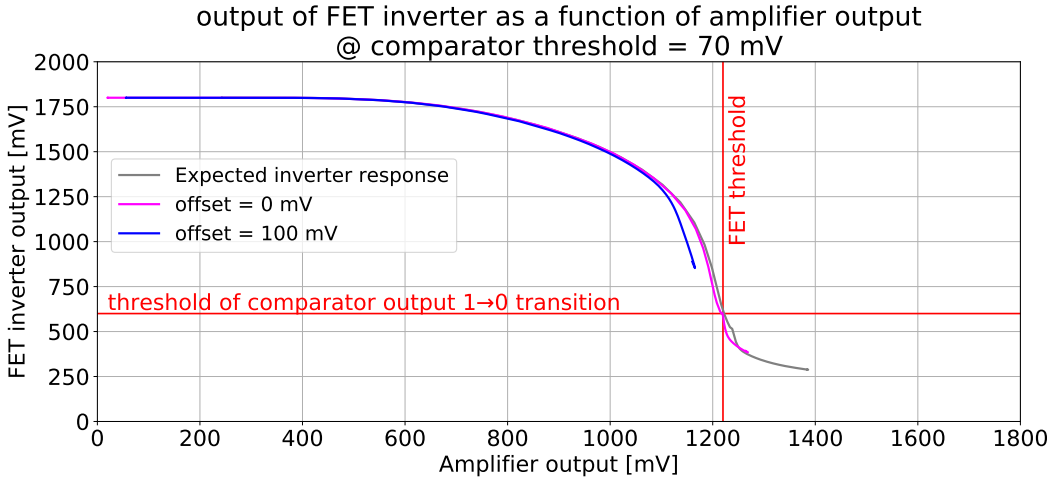


Figure 4.18: FET inverter output as a function of the amplifier output. The threshold of FET output below which the comparator output transitions from logic high to logic low is at 620 mV. The "FET threshold", being 1230 mV, represents the voltage of amplifier output above which the comparator output transitions from logic high to logic low.

saturation and the waveform ringing in noise measurement, a tuning of AGND is necessary and is described in detail in Section 4.7.

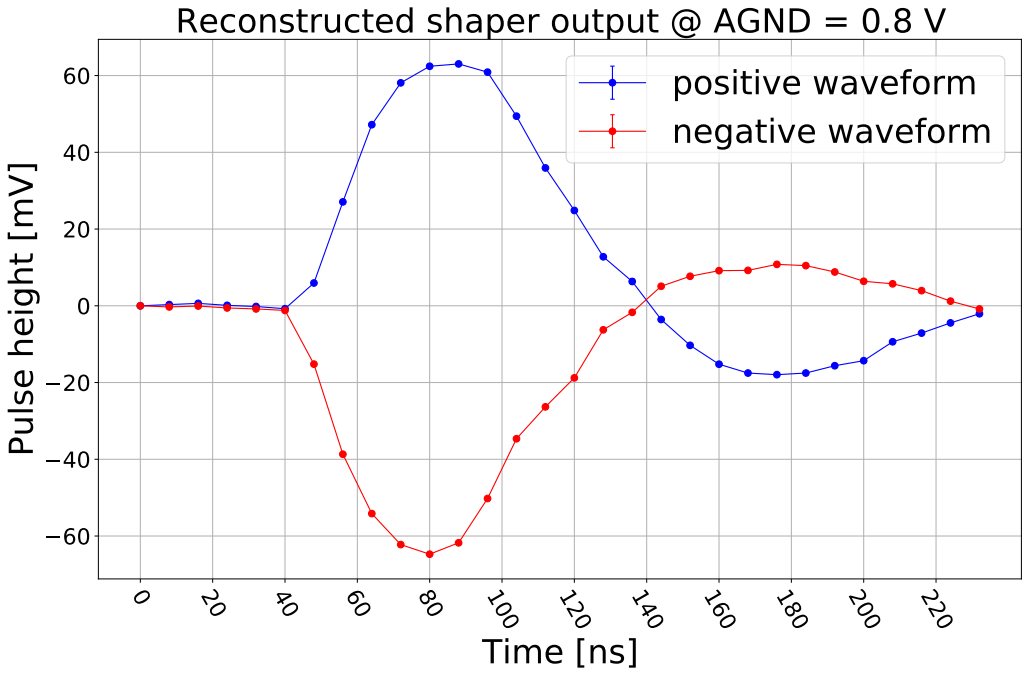


Figure 4.19: Reconstructed shaper output when AGND is 0.8 V. No saturation phenomenon is observed but ringing appears after the signal peak.

4.7 Tuning of AGND in noise measurement

From previous sections, it is understood that when AGND is 0.9 V, the shaper output baseline is saturated and thus the noise is under-estimated. On the other hand, when AGND is 0.8 V, the noise in the unit of e^- is over-estimated due to the waveform ringing. This is because that when ringing happens, the increase speed of pulse height as the increase of input charge becomes slow. Figure 4.20 shows the pulse height as a function of input charge for a channel with waveform ringing. The intercept of the fitted linear function is below 0 V, indicating that the measured pulse height is under-estimated. According to Eq. 4.5, a under-estimated pulse height results in an over-estimated ENC.

It is also found that the intercept mentioned above (called pulse intercept in this thesis) is a good indicator of the baseline saturation and ringing phenomenon. When the saturation happens, the pulse intercept is larger than 0 as shown in Fig. 4.14. On the other hand, when waveform ringing happens, the pulse intercept is lower than 0 V as shown in Fig. 4.20. For these reasons, we can conclude that when the pulse intercept is close to 0 V, the bias from saturation and ringing to the noise measurement is minimized, and we should tune the AGND to a certain value such that the pulse intercept is consistent to 0 V to perform noise measurement.

Due to the voltage drop inside the chip, the AGND voltage is different for different channels within one chip. And because of the huge amount of time needed, it is hard to find the optimal AGND of every channel. In the noise measurement performed in this thesis, as to be described

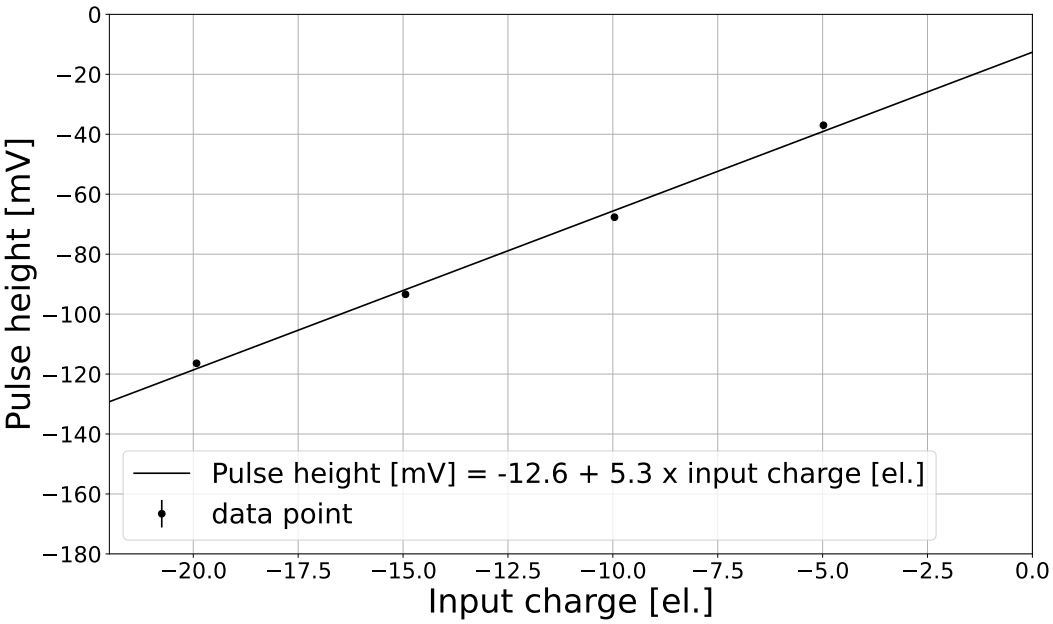


Figure 4.20: Ringing channel

in Section 4.8, the noise of 128 channels are measured using the following method. At first, we find an AGND which makes intercepts of most channels close to 0 V. Using the AGND, we measure the noise of all channels as explained in Section 4.4.

These channels are divided in to 6 groups with different detector capacitance (0, 10, 12, 15, 18 and 22 pF). The noise at each detector capacitance is given by the averaged noise in each group. If the distribution of the pulse intercept of all measured channels peaks at 0 V, we declare that the averaged noise is not biased. Further more, for the group with 0 pF detector capacitance, the noise level as a function of the pulse intercept is fitted to a linear function, with slope referred to as S. Using the standard deviation of the pulse intercept distribution of all measured channels (referred to as ΔI), the systematic uncertainty in the noise measurement for groups with non-zero detector capacitance is defined to be

$$\Delta\text{ENC(sys.)} = |S| \cdot \Delta I \tag{4.9}$$

4.8 Measurement of pulse width, pulse height and noise

The measurement is performed with AGND set to 0.89 V. The pulse height as a function of input charge of a typical channel is shown in Fig. 4.21. A zero-consistent pulse intercept is observed in this plot, indicating that the noise measurement is not biased by saturation and waveform ringing.

Using the automated threshold scanning system, the waveforms of 128 channels in one chip are measured.

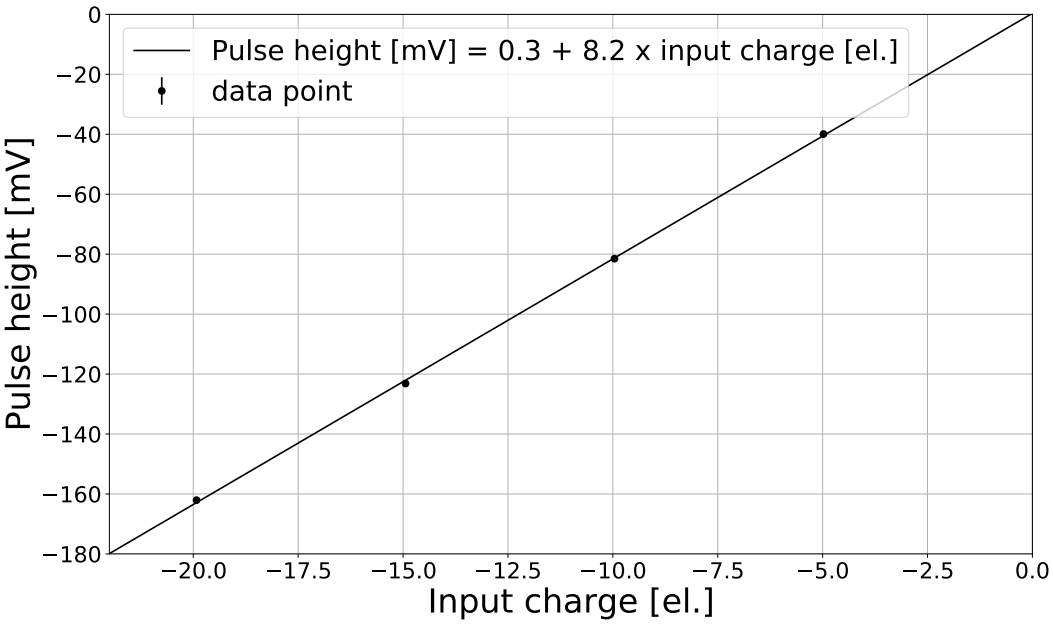


Figure 4.21: Pulse height as a function of injection charge by tuning AGND to 0.89 V. The intercept of fitting result is consistent to 0.

However, problems are found in the measurement of some channels and those channels are removed from data analysis to be described below. In 25 channels, the comparator threshold DAC failed to cover the baseline of the shaper output and thus failed to measure the noise of those channels. 18 broken channels with unhealthy shaper output (like Fig. 4.22) are found and they are also excluded. The mechanism for these unhealthy channels is still under-investigation, hypothesis are proposed that powers/bias voltage supplied to these channels does not meet the design value due to the voltage drop inside the chip.

After the data selection, 85 channels remained for further analysis to derive the pulse width, pulse height and noise. Figure 4.23 shows that the intercept distribution peaks near 0 V, thus the noise measurement is not biased.

Figure 4.24 shows the distribution of pulse width of these 85 channels. The average pulse width is 56.2 ns with a standard deviation of 6.3 ns. It has a good agreement with the simulation result which gives 52 ns.

Figure 4.25 shows the measured pulse height as a function of detector capacitance. The center value of each data point is the mean of the pulse heights measured in multiple channels, while the standard deviation of each data point is calculated by

$$\sqrt{\frac{\sum_i (\text{pulse height}_i - \text{mean pulse height})^2}{n-1}} \tag{4.10}$$

where n is the number of channels at each detector capacitance. At detector capacitance of 15 pF, the measured pulse height is 73 ± 2 mV, which is only about 70% of the simulation. It

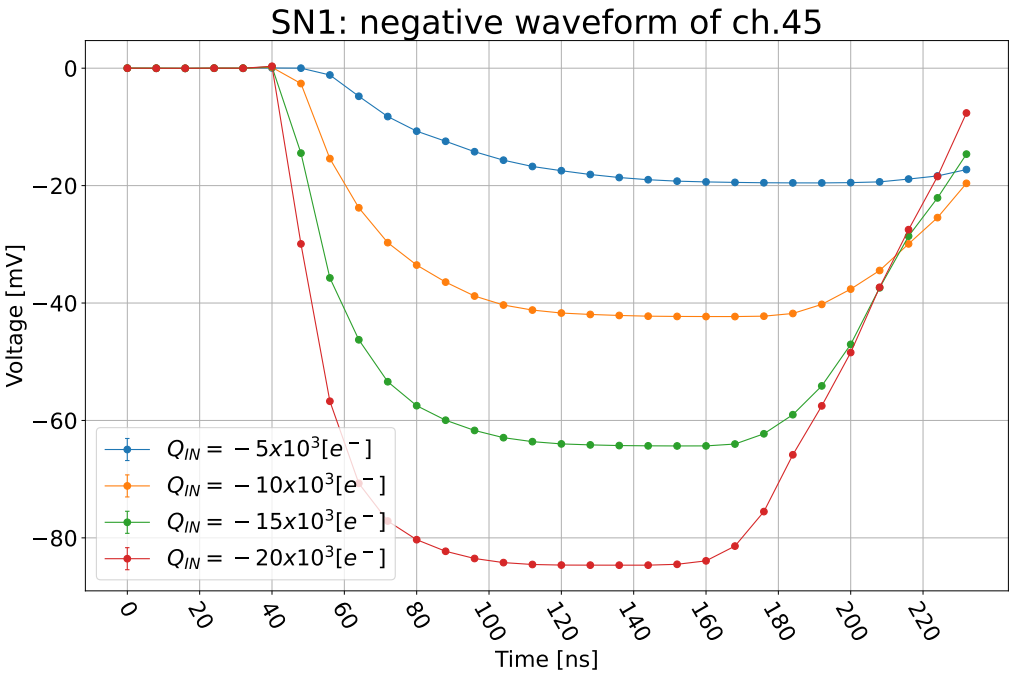


Figure 4.22: Waveform of broken channels.

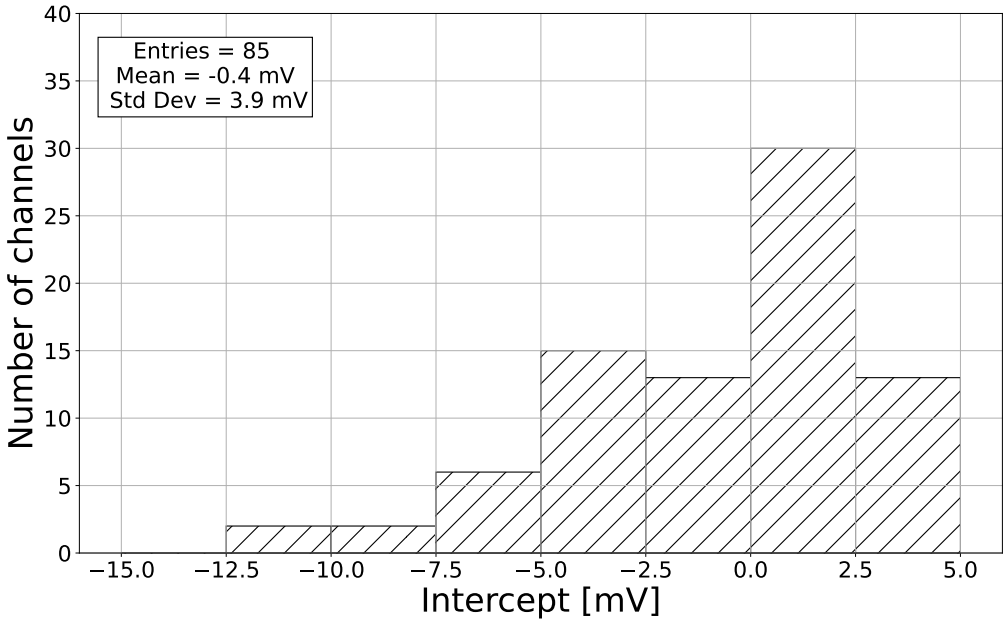


Figure 4.23: Distribution of intercept in the fitting of pulse height as a function of input charge.

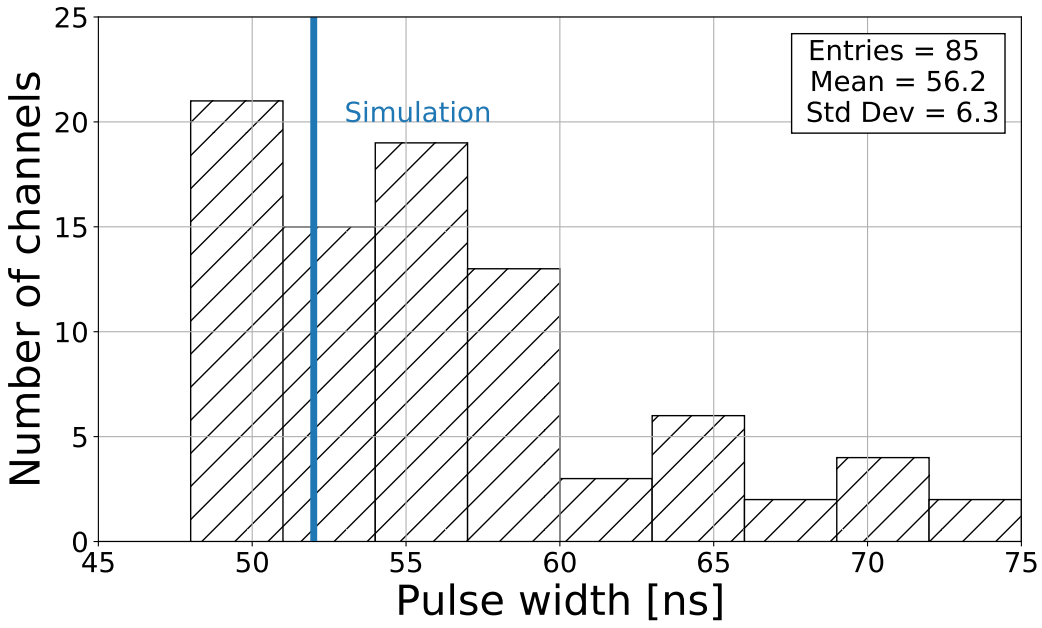


Figure 4.24: Pulse width distribution

should be acceptable in real operation.

Figure 4.26 shows the measured noise as a function of detector capacitance. The center value and standard deviation of each data point is calculated using the the measured noises in multiple channels. This standard deviation is interpreted as statistical uncertainty. The measured noise at detector capacitance of 0 pF (no detector capacitance) is about 300 electrons which has good agreement with the simulation result. However, the noise at the detector capacitance of 15 pF is about 1200 electrons, which is larger than our requirement of 800 electrons, and the result is larger than the simulation expectation by about 60%.

To estimate the systematic uncertainty in this noise measurement, noise of channels with 0 pF detector capacitance as a function of pulse intercept is fitted to a linear function and the result is shown in Fig. 4.27. The slope S is measured to be -6 e^-/mV. With the ΔI being 3.9 mV derived from Fig. 4.23, the systematic uncertainty is calculated to be 23 e^- by Eq. 4.9.

One of the sources, which cause the discrepancy between the measurement and simulation in the pulse height and noise results, is believed to be the parasitic capacitance on the test board, which is not taken into account in the detector capacitance calculation while it is estimated to be about 3 pF or more. While the addition contribution to the detector capacitance may explain the discrepancy in the noise, it is difficult to estimate the capacitance precisely in the current setup. We should improve the test board setup for the next board development, so that we reduce the parasitic capacitance on the board and measure the capacitance with an LCR meter.

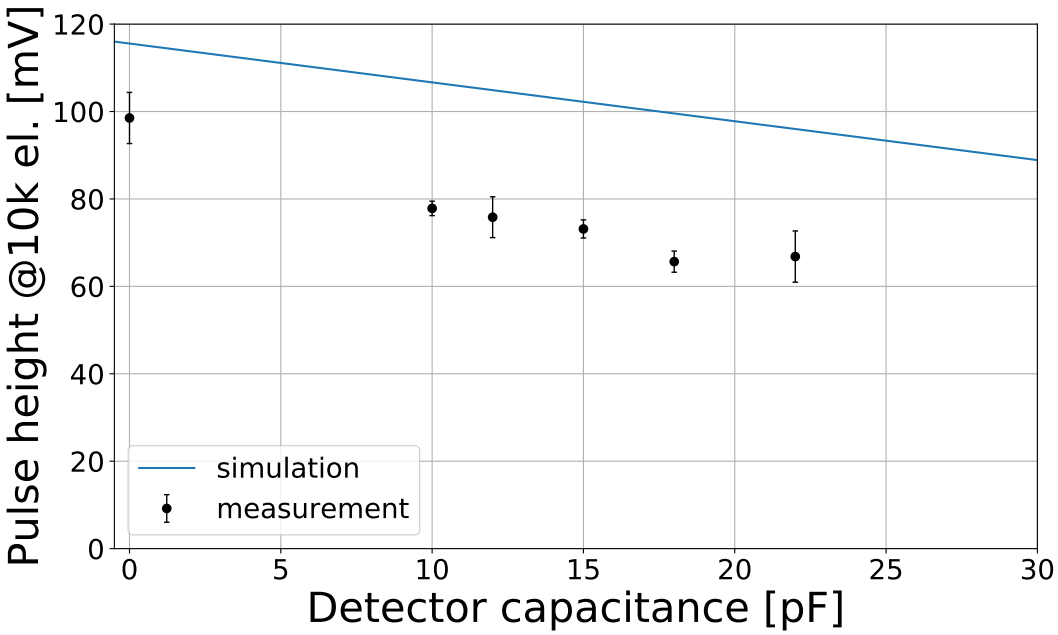


Figure 4.25: Pulse height as a function of detector capacitance

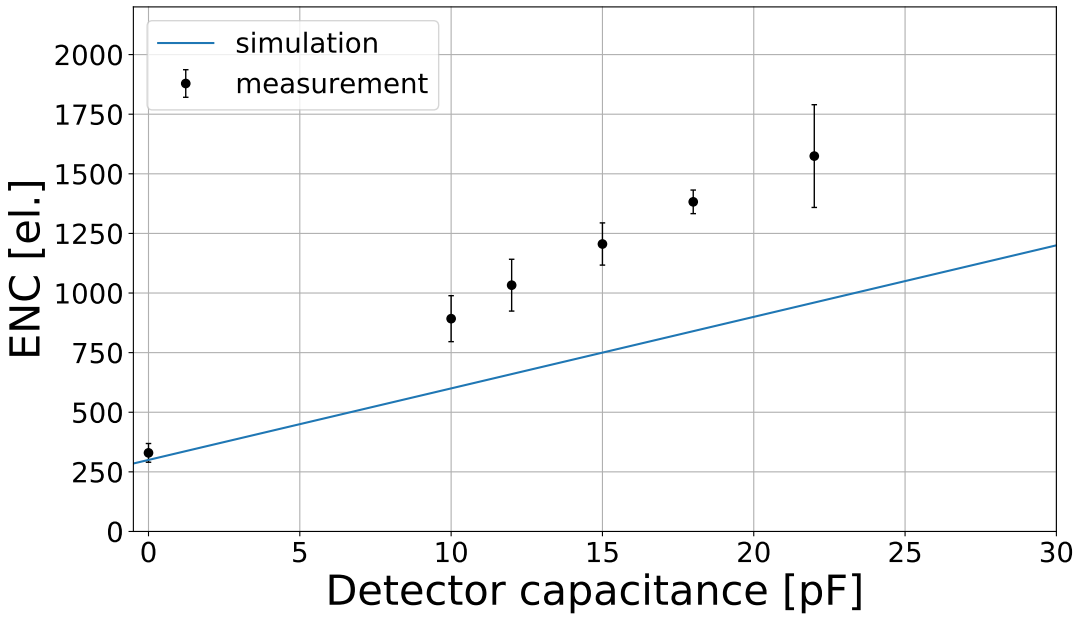


Figure 4.26: Noise as a function of detector capacitance. The error bar in the plot represents only the statistical uncertainty.

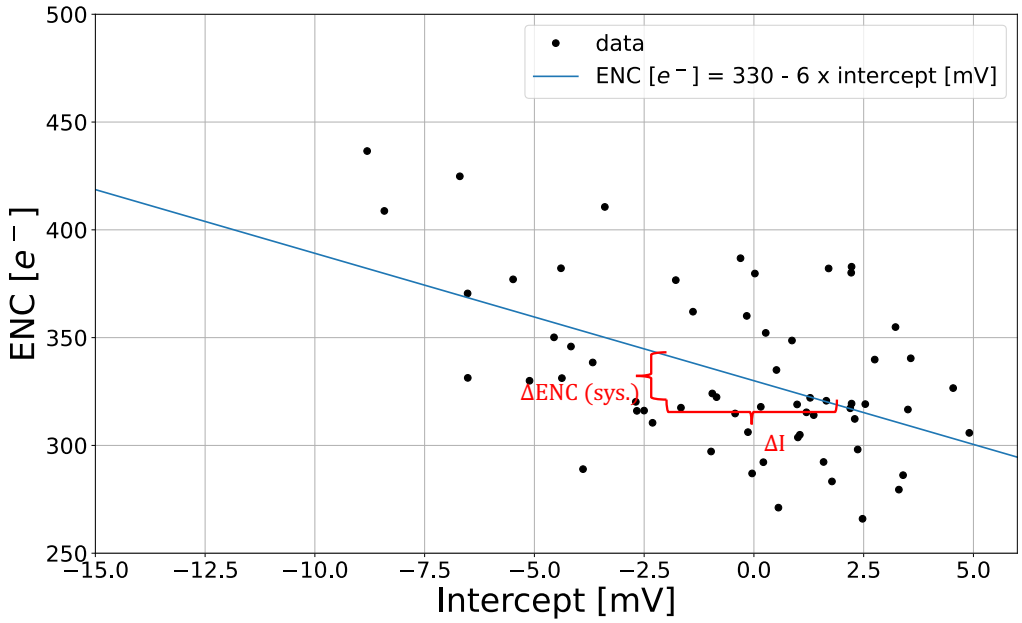


Figure 4.27: Noise level as a function of pulse intercept for channels with 0 pF detector capacitance. The data points are fitted to a linear function for the estimation of systematic uncertainty for noise measurement in channels with non-zero detector capacitance.

4.9 Summary and possible improvements

In this performance evaluation the entire system was developed from the sketch, including the test board, firmware of the FPGA, and the DAQ/slow-control software on the PC. The waveform of both positive and negative shaper output was reconstructed using the binary hit information from SNAP128A. The power consumption is measured to be 329 mW/chip, which meets the 400 mW/chip requirement. For the negative signal, the measured pulse width agrees well with the simulation. The measured pulse height at target detector capacitance (15 pF) is about 70% of simulation which is still acceptable. The measured noise for negative signal at the target detector capacitance is about 1200 e^-, which is over the requirement of 800 electrons and is about 60% larger than the simulation expectation. It is possible that this large noise is due to the parasitic capacitance on the test board, which could be about 3 pF or more. The measurement of negative signals and chip power consumption is summarized in Table 4.2. For the positive signal, saturation of reconstructed shaper output is observed and the mechanism of saturation was qualitatively studied using the cadence virtuoso IC617 simulation environment. While the saturation issue and large-noise issue are discovered by the performance evaluation, the successful reconstruction and measurement of negative shaper output indicates that this chip can be assembled with a TFP-DSSD sensor and measure the noise when connecting the analog input channel to sensor and measure particles.

In the next version of SNAP128 prototype, the saturation problem will be solved by improv-

	Design requirement	simulation	Measurement
power consumption	<400 mW/chip	-	329 mW/chip
pulse width	<100 ns	52 ns	56.2 ± 6.3 ns
pulse height @ C_{det}= 15 pF (input charge = 10,000 e^-)	-	102 mV	73 ± 2 mV
noise level @ C_{det}= 15 pF	<800 e^-	750 e^-	1205 ± 88 (stat.) ± 23 (sys.) e^-

Table 4.2: Design requirement, simulation and measurement result of negative signal

ing the comparator design as discussed in Section 4.6. In addition, the noise will be evaluated more precisely by using a new test board which has much smaller parasitic capacitance and also try to measure it with an LCR meter. Moreover, for better signal-to-noise ratio, the noise will be reduced by relaxing the pulse width and power consumption requirements, as well as reducing the target detector capacitance with shorter sensor strips. Assuming the measured noise to simulated noise ratio 1.6 will be kept in the next version of the chip, to suppressed the noise below 800 e^-, the noise at simulation should be less than 530 e^-. By a naive calculation assuming $Q_{\mathrm{noise}} \propto 1/\tau$, where τ is the shaping time of CR-RC circuit, extending the shaping time to about 80 ns can reduce the noise below 500 e^-. Linearity of DAC will also be improved such that the DAC calibration can be skipped.

Chapter 5

Setup of TFP-SVD test module

5.1 General ideas and plan

In TFP-DSSD performance evaluation, the full depletion voltage, leakage current at an environment temperature of 25 °C and the noise of readout chips connected to the sensor are evaluated. A test module of the TFP-SVD is developed for these evaluations. The prototype sensor and SNAP128A chips are integrated on the module. The design is also intended to be used in the beam test for further performance evaluation like sensor efficiency and signal charge measurement using cosmic ray and accelerator beams.

A block diagram of readout and trigger system for the test module targeting for the beam test is shown in Fig. 5.1. A dedicated test board is developed on which the TFP-DSSD sensor and the SNAP128A chips are implemented. The analog inputs of SNAP128A are connected to the TFP-DSSD readout strips to detect the signal from TFP-DSSD. The same as the SNAP128A evaluation, the slow control commands of SNAP128A chips are issued by a PC and the hit information collected from the SNAP128A chips are send to PC for archiving. And the FPGA plays the role of communication bridge between PC and SNAP128A chips. In addition to the usual trigger for noise measurement which is issued by the PC, a new trigger issued by the scintillator can be used in the beam test. By now, the development of the test board, firmware on the FPGA and software on the PC is finished, while the scintillator trigger system is still under construction.

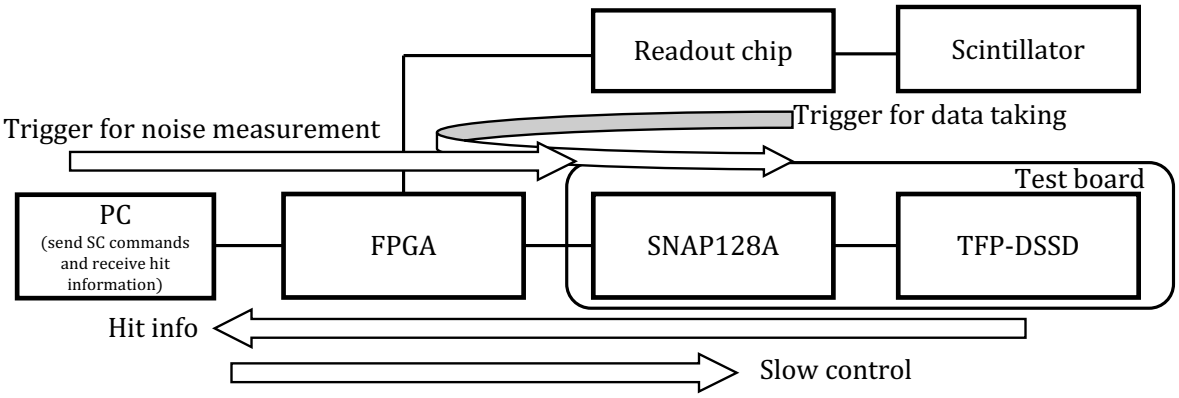


Figure 5.1: Setup of TFP-SVD readout and trigger system

The following is the list of the plans that are completed in this work:

step 1 Assemble SNAP128A chips and TFP-DSSD sensor onto the test board

step 2 Wire bonding between SNAP128A chips and test board

step 3 Measurement of full depletion voltage of TFP-DSSD and checking of chip status on the TFP-SVD prototype

step 4 Wire bonding between SNAP128A analog input and readout strips of TFP-DSSD

step 5 Evaluation of SNAP128A performance after connecting analog input to readout strips of the sensor

The development of test system is described in this chapter, while the results for full depletion voltage and chip noise connected to the sensor in step 3 and step 5 are mentioned in the next chapter. The development of TFP-SVD test board is described in Section 5.2. The wire bonding that happened in step 2 and step 4 is described in Section 5.3. The development of readout firmware and software is described in Section 5.4. As the last part of this chapter, the status of the chip on the TFP-SVD prototype and their availability for noise measurement connected to the sensor is summarized in Section 5.7.

5.2 Design of TFP-SVD test board

The full schematic design and outlook design of TFP-SVD test board is shown in Appendix B. Here in this section, the key points of design are mentioned. The simplified schematic of TFP-SVD test board is shown in Fig. 5.2.

The bias ring on P-side and N-side of the TFP-DSSD sensor is connected to the PGND and NGND, respectively, with the wire bondings. Voltage (V_{bias}) between the NGND and PGND is applied to fully deplete the TFP-DSSD sensor. PGND (NGND) is the ground for all chips that are responsible for reading out the P-side (N-side) signal of TFP-DSSD sensor. The ground for chips connected to FPGA (FPGA_GND) is defined to be 0 V.

Eight SNAP128A chips are placed on the front side of the board to readout signals from P-side strips of TFP-DSSD, while 6 SNAP128A chips are placed on the back side of the board to readout the signals from N-side strips of TFP-DSSD. The analog input pads are electrically connected to TFP-DSSD readout strips by wire bonding, and the strip pitch of the sensor and pitch of the SNAP128A analog inputs are adapted by pitch adapters. Differential and single-ended isolators are placed at the boundaries of the three grounds. The differential isolators are for the clock (D_CLK127M), trigger (D_TIMING), and binary output (D_FPGA_D) signals. The single-ended isolators are for slow control signals D_MSCK and D_MSIO. Given that the D_MSIO signal is responsible for both write in and read out data from SNAP128A chips, the single-ended isolators are bi-directional and the direction is controlled by FPGA. Test pins for monitoring the comparator threshold for each chip are placed at the left and bottom edge of the board.

The layout design and production of test board was also performed by GNomes Design Co., LTD. After the delivery of the test board to KEK, Tsukuba (Japan), two pitch adapters, one TFP-DSSD sensor and 14 SNAP128A front-end ASICs are glued on the test board and a photo is shown in Fig. 5.3. In the top photo, the P side chips are named as P1 to P8 from left to right. In the bottom photo, N side chips are named as N1 to N6 from bottom to top.

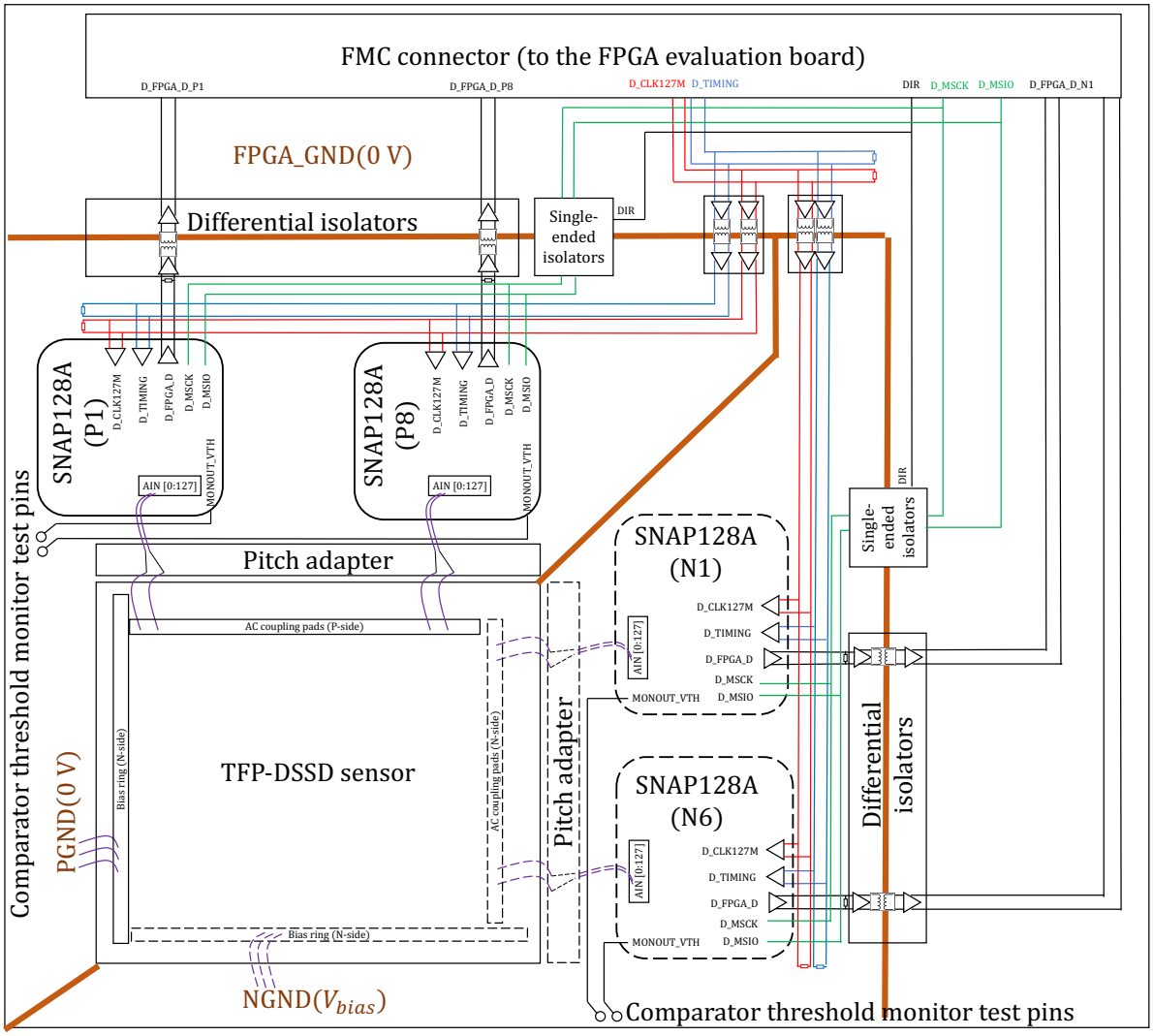


Figure 5.2: Schematic of TFP-SVD test board. The dotted parts are in the back side of the board. Three grounds are configured in this board with PGND and FPGA_GND at 0 V while NGND at +20 V to apply bias voltage to the TFP-DSSD sensor. The dark orange line is the boundary of three grounds. The red, blue and green lines represent the D_CLK127M, D_TIMING and slow control signals (D_MSCK and D_MSIO), respectively. The magenta lines represent the wire bonding.

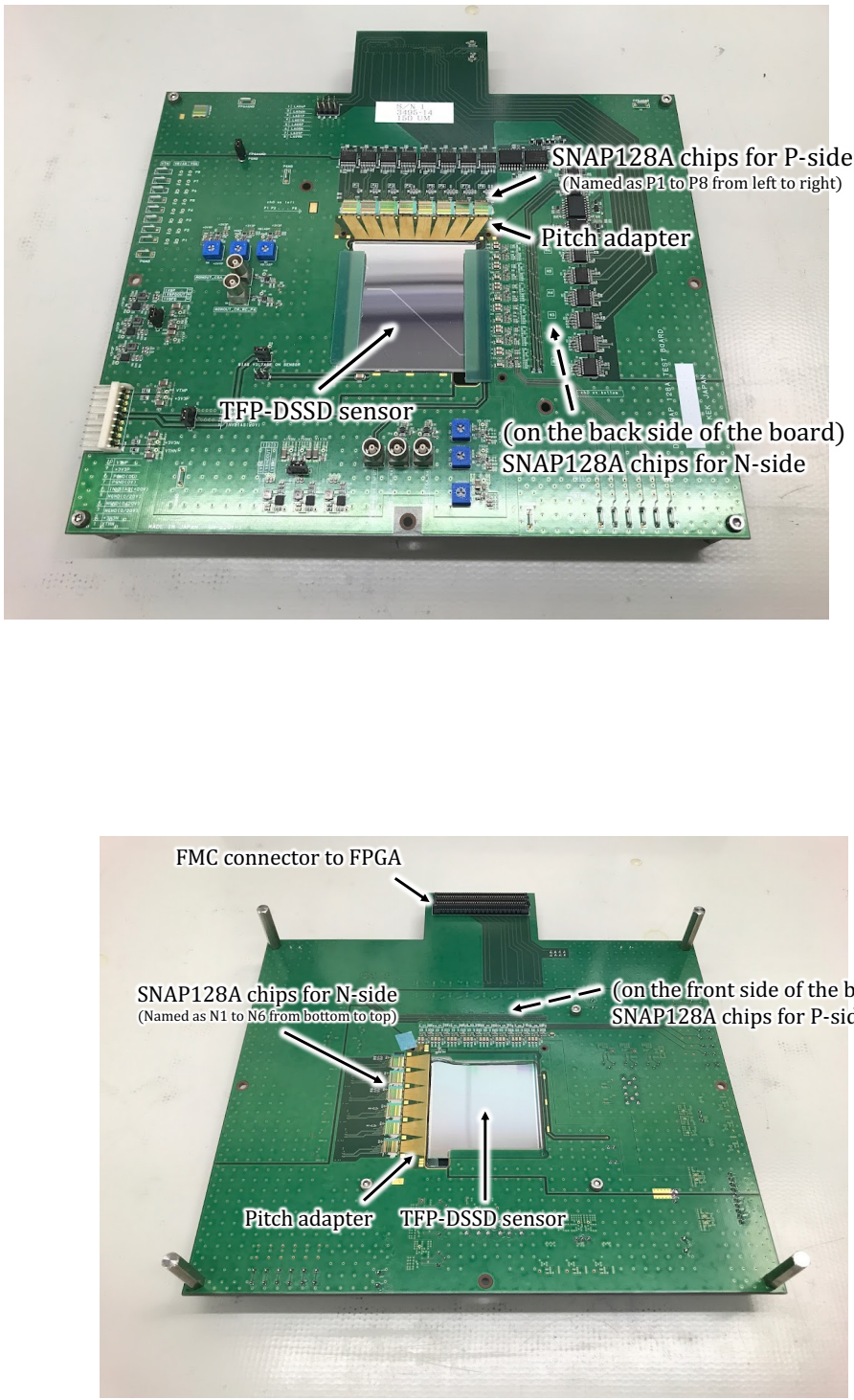


Figure 5.3: Photos of the assembled TFP-SVD test board. The top one is the front side while the bottom one is the back side. The dotted arrays refers to parts that are placed on the opposite side and invisible in the photo. In the top photo, the P side chips are named as P1 to P8 from left to right. In the bottom photo, N side chips are named as N1 to N6 from bottom to top.

5.3 Wire bonding

The necessary wire bonding in the setup of TFP-SVD prototype is shown in Fig. 5.4. From left to right are the bonding of SNAP128A digital side, SNAP128A analog side, TFP-DSSD readout strips and TFP-DSSD bias ring, with 294, 2100, 1792 and 6 wires to be bonded in total, respectively. Since the bonding pads of TFP-DSSD readout strips are in a zigzag arrangement, two layers of wire bonding is necessary. As for the bonding of SNAP128A analog, the innermost layer bonding includes analog power connections and monitor signals like MONOUT_VTH, while the outer two layers are the analog signal inputs of 128 channels, which is also in a zigzag arrangement on the SNAP128A chip. Due to the huge amount of wire bonding, the REBO-7S automatic wire bonder (Fig. 5.5) is used in this work.

In the step 2 described in section 5.1, only the wire bonding of of the SNAP128A digital, innermost layer of SNAP128A analog and the TFP-DSSD bias ring was performed. After that, the function of DAQ system was tested, and the full depletion voltage of the sensor was measured (Section 6.1). The noise of SNAP128A chips without the sensor connection were measured to confirm the working status of the chips.

After the noise measurement, wire bonding of the TFP-DSSD readout strips and the 128 channels of one chip on the P side and the first 64 channels of 4 chips on the N side (reason for this is in Section 5.7) was performed to measure the SNAP128A noise when connected to TFP-DSSD sensor, and the result is shown in Section 6.2. In the second time of wire bonding, a 95% success rate of wire bonding was achieved, with about 340 SNAP128A channels connected to TFP-DSSD sensor. The number of the connected channels is corresponding to about 12.5% (33.3%) of total readout strips in the P (N) side of the sensor. Figure 5.6 and Fig. 5.7 shows the photo of wire bonding of TFP-DSSD readout strips and SNAP128A analog, respectively.

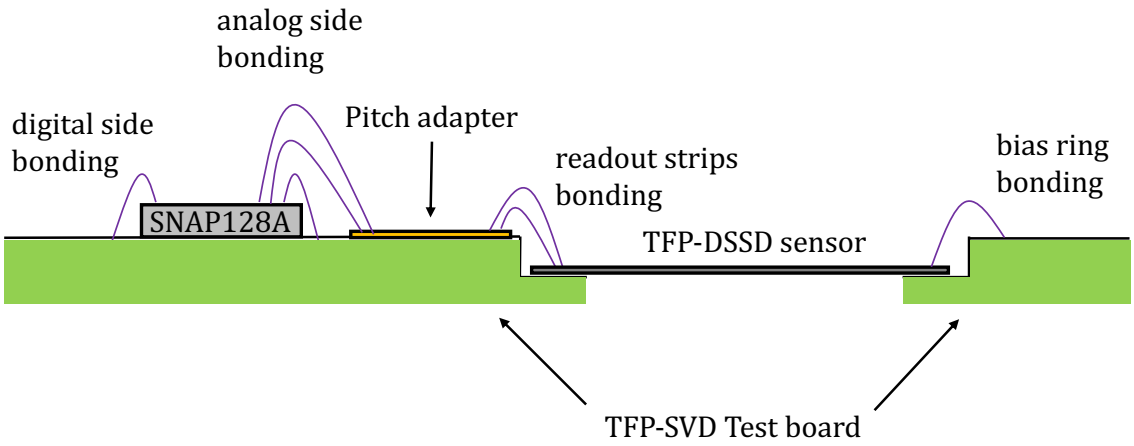


Figure 5.4: Illastration showing the wire-bonding locations in TFP-SVD test module.

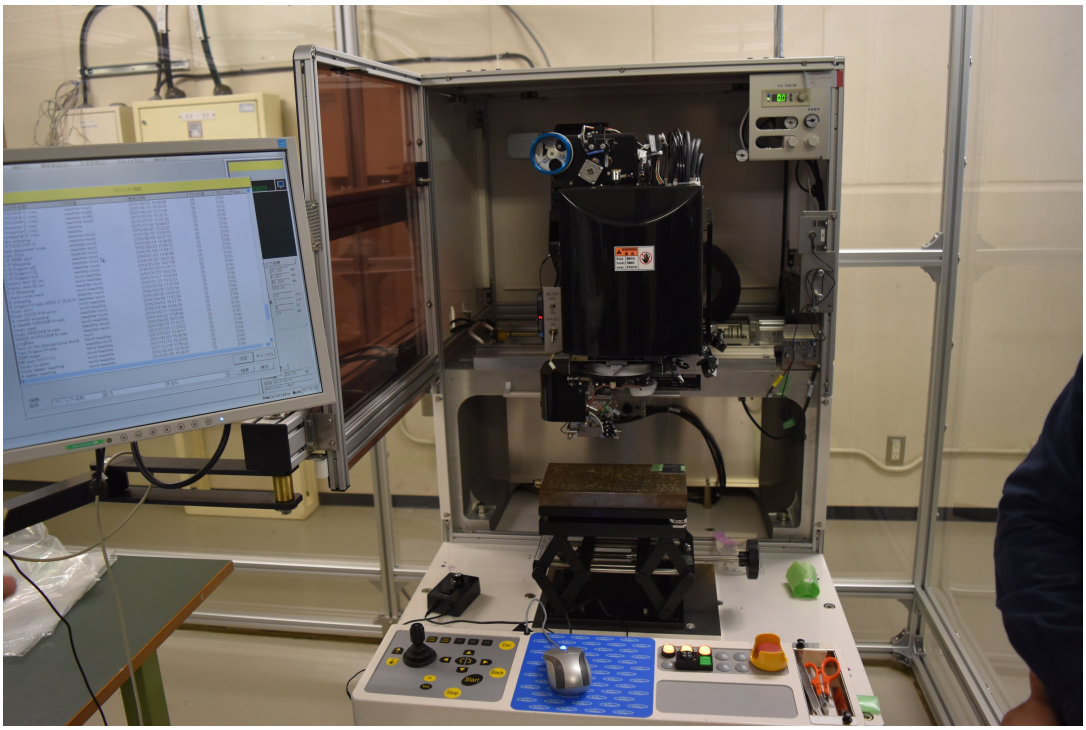


Figure 5.5: REBO-7S automatic wire bonder

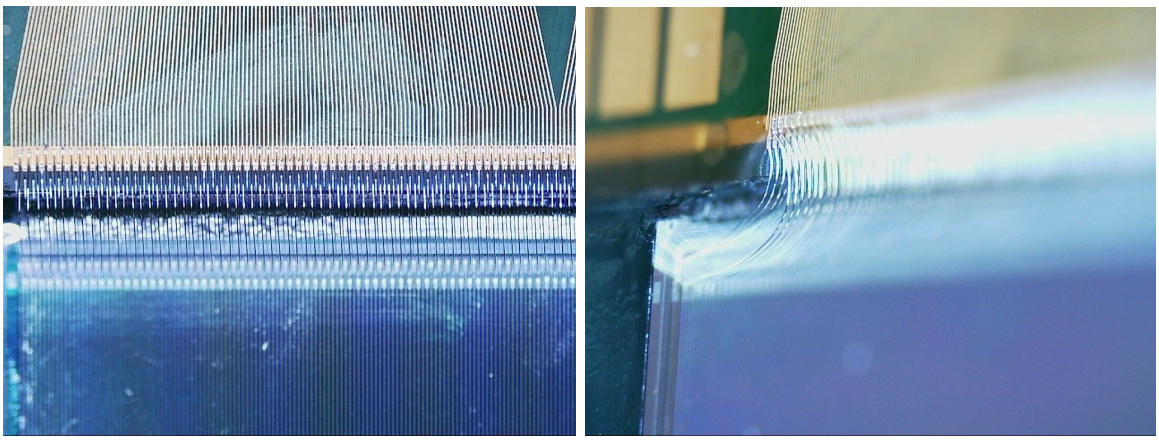


Figure 5.6: Wire bonding of TFP-DSSD readout strips. The left one is the top view while the right one is the left-side view.

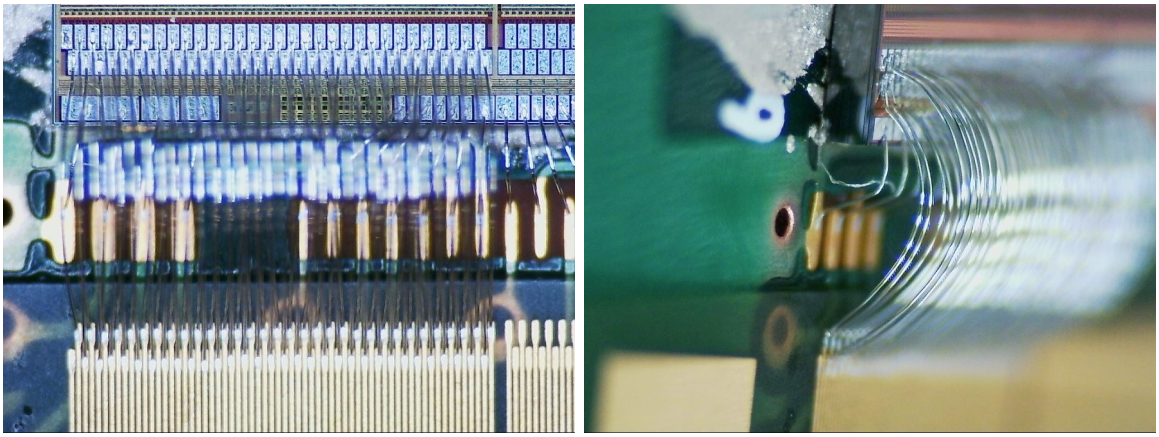


Figure 5.7: Wire bonding of SNAP128A analog. The left one is the top view while the right one is the left-side view.

5.4 Development of readout firmware

Given the larger data size and complexity brought by reading out data from 14 SNAP128A chips, the firmware was updated and the structure of the new firmware is shown in Fig. 5.8. Comparing with the firmware for reading out only one SNAP128A described in Section 4.2.2, the new firmware has sub-FIFOs (`FIFO 1`, `FIFO 2`, ... `FIFO 14`) for buffering the data from each chip and a selector that serialize the data from 14 chips to send them to PC via the SiTCP. In addition, to reduce the data size and improve the transmission speed, a zero suppression algorithm is applied in the `Data Decoder` module. The circuits that generate D_TIMING, D_CLK127M and slow control signals are the same as the old firmware.

The block diagram of `Data Decoder` with zero suppression algorithm implemented is shown in Fig. 5.9. This module outputs the data only from the channels that has at least one logic high. The output of this module is named as one chip segment whose structure is shown in Fig. 5.10. The header of the data received from SNAP128A (D_FPGA_D) is first send to the `parallelizer` which parallelizes the serial data to 8-bit data and send them to the downstream FIFO. The hit data of 128 channels are cached in a Block Random-Access Memory (`BRAM`). While writing hit data into the `BRAM`, the `Channel looper` module records the channels that has at least one logic high in a frame (e.g. channel 0 and channel 125 in Fig. 5.9). After the data are written in the `BRAM`, the `channel looper` loops over all the memorized channels and reads out the hit data of these channels to `parallelizer` module via a `MUX`. For example, when the loop reaches the channel 125, this channel number is stored in the `parallelizer` And at the same time, the `MUX` is configured such that the output is equal to the input of channel 125. Then, the `BRAM` loops over all the cached frames and the hit information of channel 125

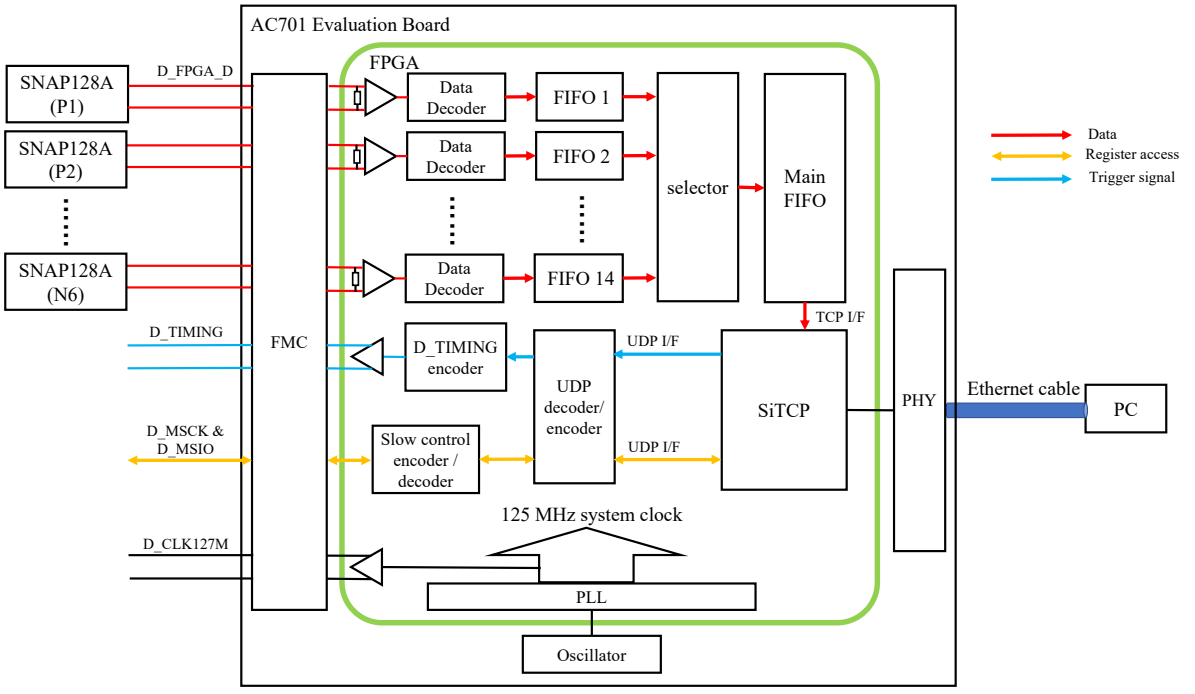


Figure 5.8: Firmware structure for sensor evaluation

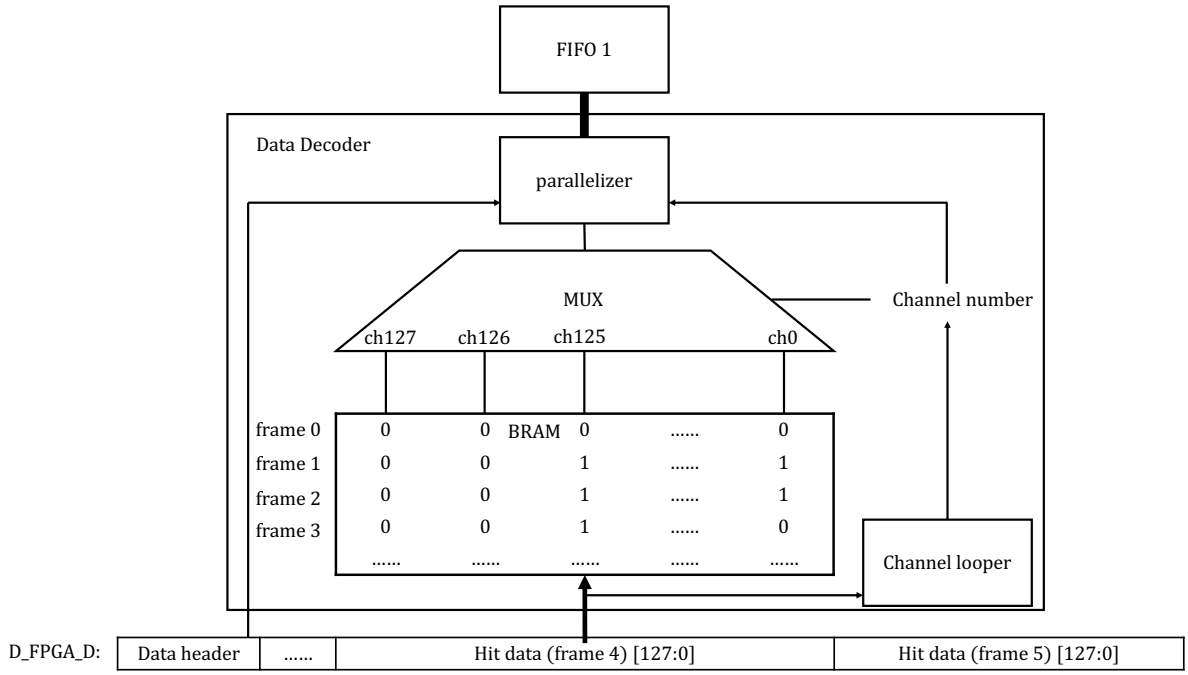


Figure 5.9: Block diagram of `Data Decoder`.

is sent to the `parallelizer` and parallelized into 8-bit signal and send to FIFO. If the total number of frames is not a multiple of 8, the remaining bits of the last byte is filled with 0. After looping over all the memorized channels, the `parallelizer` sends 8'b1000,0000 to FIFO as the end of the chip segment.

When data of each chip are cached into the FIFO, the `selector` in Fig. 5.8 loops over the FIFOs and send the data cached in FIFO to the `main FIFO` and then passed to PC via SiTCP. The `selector` module has a mask function, which skips the FIFOs of the specified chips. The masking status of each chip is stored in a register in FPGA which can be accessed by PC via the UDP interface of SiTCP.

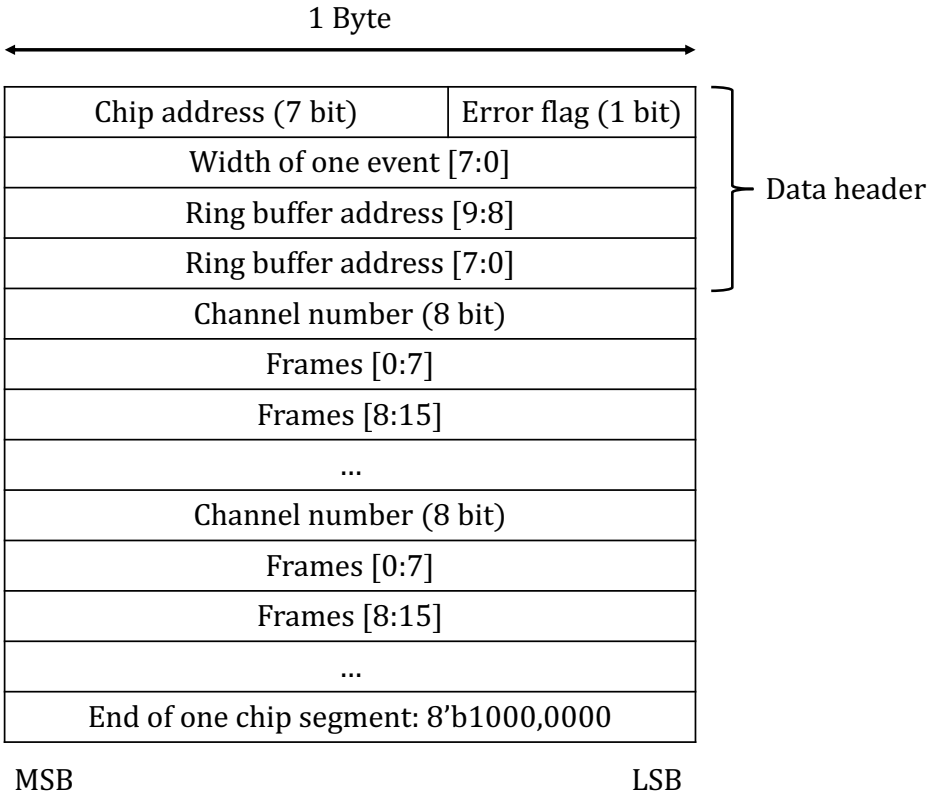


Figure 5.10: Structure of chip segment.

5.5 Development of readout software

In addition to more `SNAPchip` objects in the module, this module also implemented a `SNAPchip` whose chip address is set to 0xFF, for broadcasting register access. This function makes use of the property of SNAP128A that when the chip address is 0xFF, all chips are open for register write-in.

5.6 Upgrade of comparator threshold DAC calibration

To shorten the calibration time and to calibrate 14 SNAP128A chips at the same time, the calibration of the comparator threshold DAC was upgraded. The 10-channel GL240 logger in Fig. 4.9 is replaced with the 20-channel GL840. In addition, the GL840 is also able to connect to the PC through a Local Area Network (LAN) and send the real-time measured voltages to the PC. With voltage can be measured in real-time, the calibration time of each DAC bit is shorten to 1 second, and the total calibration time is reduced from 45 hours to 9 hours.

5.7 Chip status on the TFP-SVD prototype

Before the delivery of the SNAP128A, only sight examination is performed thus bad chips are mixed in. To exclude those bad chips, the status of the chips glued on the TFP-SVD test

board should be examined before connecting them to the sensor. After wire bonding in step 2, the status of the chips is verified by an insulation test and a readout test.

The insulation test is to find if any signal line is short to the ground or other power supply lines. As a result, 2 chips on the P side (P7 and P8) are found to be short to the ground inside the chip. These two chips are then electrically disconnected from the test board.

The readout test is to see if the binary hit information can be properly read out and if shaper output can be properly reconstructed. In the test, a bug on the test board was found which results in 4 chips on the P side (P1, P2, P3, P5) cannot be read out by the FPGA. Further readout test was performed to the remaining one chip on the P side (P4) and 6 chips on the N side (N1, ..., N6) to test the performance of each readout channel. Having the results, we define "healthy channel" with the following criteria:

- The propability $P(V_{\mathrm{TH}}, i)$ is 100% at the maximum threshold in the DAC range, and 0% at the minimum threshold.
- Noise $< 800\ e^-$
- Pulse height > 40 mV with 10,000 e^- input charge
- Pulse width < 100 ns

The last criterion is introduced to reject channels with a waveform like Fig. 4.22. 128 channels of P4 chip is measured and 105 channels are classified to be healthy channels. Due to time constrain, only the first 64 channels on each N side chip is tested and we confirmed that all measured channels on N1, N2, N3, N5 chips are healthy channels. For all of the measured channels on the N4 and N6 chips, the waveform was not measured due to a bad S-curve measurement ($P(V_{\mathrm{TH}}, i)$ is kept at 0 even if the V_{TH} is high). The reason is still under investigation.

The status of each chip is summarized in Table 5.1. According to the chip status, we connect the 128 channels of P4 chip and first 64 channels of N1, N2, N3 and N5 chips to the sensor in the step 4 wire bonding (Section 5.3). Unfortunately, after the wire bonding, the wires on the P4 chips are broken becuase of an accident, thus only the noise of 4 N side chips is evaluated in step 5 (Section 6.2).

chip	status
P1	not available for bug on board
P2	not available for bug on board
P3	not available for bug on board
P4	105/128 channels are healthy (wire is broken)
P5	not available for bug on board
P6	not available for bug on board
P7	short to the ground internally
P8	short to the ground internally
N1	64/64 channels are healthy
N2	64/64 channels are healthy
N3	64/64 channels are healthy
N4	Bad S-curve measurement
N5	64/64 channels are healthy
N6	Bad S-curve measurement

Table 5.1: Status of 14 SNAP128A chips on the TFP-SVD prototype

Chapter 6

Performance evaluation of TFP-SVD prototype

After the assembly of TFP-SVD prototype, inverse bias voltage is applied to the TFP-DSSD and 256 channels of 4 SNAP128A chips on the N side are connected to the sensor. This chapter reports the full depletion voltage measurement of the TFP-DSSD prototype sensor in Section 6.1 and report the measurement of noise level of SNAP128A analog channels when connected to the sensor in Section 6.2. At the end of this chapter, a summary of current measurements and the future experiment are described in Section 6.3.

6.1 Measurement of full depletion voltage of TFP-DSSD

6.1.1 Principles of measurement

This thesis measures the full depletion voltage of TFP-DSSD sensor by measuring I-V curve, which is the leakage current as a function of the inverse bias voltage.

The schematic for measurement is shown in Fig. 6.1. Inverse bias voltage U_{bias} is applied between the n^+ strips and p^+ strips. As described in Chapter 3, each p^+ strip is all connected to a bias ring via a 10 MΩ bias resistor and the same for n^+ strips. Because the substrate of the sensor is n-type, as the increase of U_{bias}, the depletion area expands from around the p^+ strips to the n^+ strips inside the n bulk. And finally, the voltage at which the whole n bulk is depleted is the so-called "full-depletion voltage V_{dep}". The depth of the depletion area d shown in Fig. 6.1 is given by:

$$d = \sqrt{\frac{2\varepsilon_{\text{Si}}(U_{\text{bias}} + U_{\text{init}})}{eN_D}} \tag{6.1}$$

where ε_{Si} is the permittivity of Silicon. e is the elementary charge and N_D is the number density of donors inside the depleted region, $U_{\text{init}} \sim 0.5$ V is the initial voltage from built-in field without external bias voltage. U_{init} term is neglected below due to its relative small value. Due to the thermal motion, electrons inside the depletion region has the possibility to jump to the conduction band and electron-hole pairs are generated, which then drifts to the N and P side of the detector and forms the leak current. From this concept, the leakage current can be written in the following way:

$$I_{leak}(T) \simeq e\mu_{ep}(T)Ad = e\mu_{ep}(T)A\sqrt{\frac{2\varepsilon_{\text{Si}}U_{\text{bias}}}{eN_D}} \tag{6.2}$$

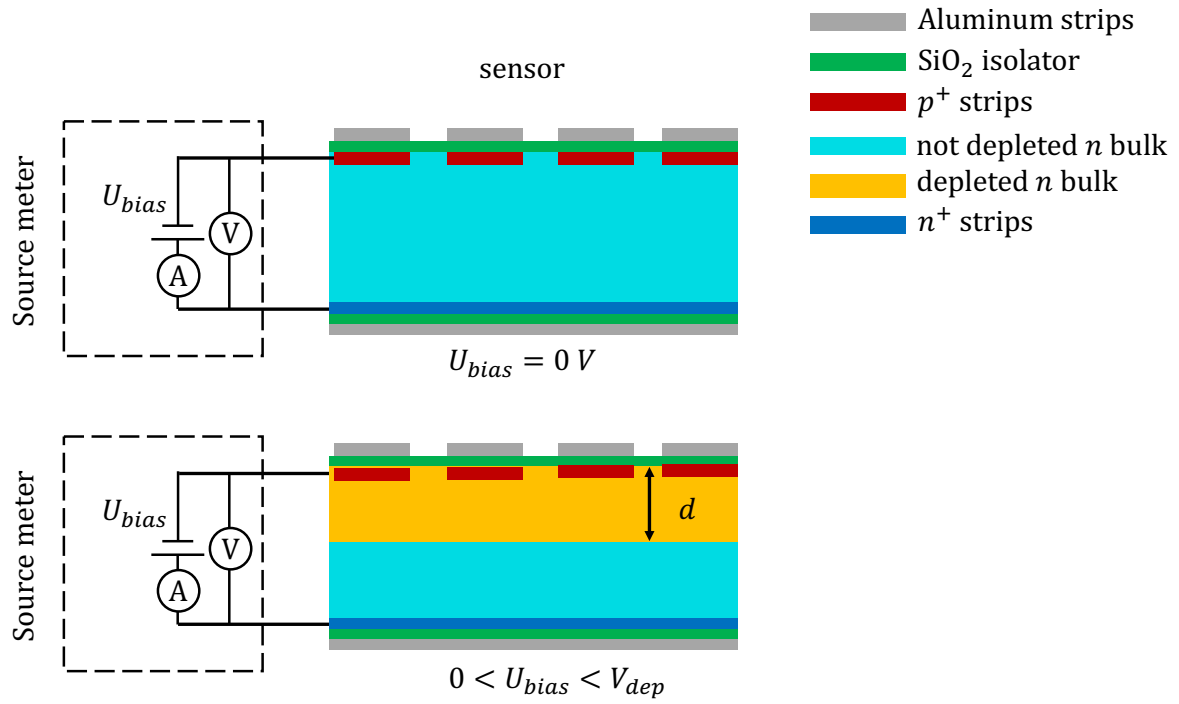


Figure 6.1: Setup of IV measurement. Bias voltage is applied between n^+ strips and p^+ strips. The depth d of the depletion region in n bulk is given in Eq. 6.2.

where A is the detector area and μ_{ep} represents the rate of the electron-hole creation, which depends strongly on the temperature. From Eq. 6.2, one can see that the squared leakage current is proportional to the inverse bias voltage before the n bulk is fully depleted:

$$I^2_{\text{leak}} \propto U_{\text{bias}}. \tag{6.3}$$

After the n bulk is fully depleted, the volume of the fully depleted region does not expand and thus the leakage current from the bulk of the sensor does not increase anymore. Even though the leakage current flows over the surface of the sensor still increases as the increase of the bias voltage, when bias voltage is equal to the full depletion voltage, one could observe a decrease in the $\frac{d}{dU_{\text{bias}}} I^2_{\text{leak}}$, or a positive peak in the $-\frac{d^2}{dU^2_{\text{bias}}} I^2_{\text{leak}}$ as a function of the U_{bias}. In this study, the full depletion voltage is measured by locating a bias voltage that gives the maximum $-\frac{d^2}{dU^2_{\text{bias}}} I^2_{\text{leak}}$.

The leakage current at different temperature T and T_0 can be expressed by [40]:

$$I = I_0 \left(\frac{T}{T_0}\right)^2 \exp\left[-\frac{E_g}{2k_B}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \tag{6.4}$$

where I and I_0 refers to the leakage current at a temperature of T and T_0, $E_g = 1.12$ eV is the effective energy gap. k_B is the Boltzmann constant.

6.1.2 Measurement setup and results

The setup of the measurement is the same as the one in Fig. 6.1, with the KEITHLEY 2612B source meter used for applying bias voltage and measuring leakage current. The sensor is fully shaded from the light. One Pt100 platinum resistance thermometers is applied to measure the environment temperature with the GRAPHTEC GL840 logger used for recording the measured results.

The leakage current is measured at different inverse bias voltage, ranging from 0 V to 18 V with a step of 1 V. At each voltage, the leakage current is measured every 10 seconds and lasted for 300 seconds. The temperature measurement is synchronized with the leakage current measurement. The measured leakage current is first calibrated to the corresponding leakage current at 25 °C using the Eq. 6.4. Figure 6.2 shows the relative leakage current measured as a function of time, with each line represents the measurement at different bias voltage. The 0 s in time axis represents the timing of changing the bias voltage. The relative leakage current is defined to be the current minus the average current in the last 100 seconds measurement at each bias voltage. The plot shows that after changing the inverse bias voltage, it takes about 200 seconds before the leakage current becomes stable for this sensor. For this reason, the leakage current at each bias voltage is measured as the average of only the data taken in the last 100 seconds, which starts 200 seconds after the change in the bias voltage.

The squared leakage current as a function of inverse bias voltage is shown in Fig. 6.3. Before the bulk becomes fully depleted, I_{leak} is approximately in a linear relationship with the increase of inverse bias voltage. The small non-linearity observed in the measurement of 0–3 V is probably caused by the complicate p^+-strip structure in the sensor, while Eq. 6.2 assumed that the p^+ doped area is a flat plane. In addition, the rapid temperature change during the measurement (the orange line in the plot) could also contribute to this non-linearity. This is because the dependence on temperature of surface leakage current component cannot be properly calibrated by Eq. 6.4.

Figure 6.4 shows the $-\frac{d^2}{dU_{\text{bias}}^2} I_{\text{leak}}^2$ as a function of the bias voltage, where $\frac{d^2}{dU_{\text{bias}}^2} I_{\text{leak}}^2$ is calculated by

$$\frac{d^2}{dU_{\text{bias}}^2} I_{\text{leak}}^2(U_{\text{bias}}) = \frac{I_{\text{leak}}^2(U_{\text{bias}} + 1\ V) + I_{\text{leak}}^2(U_{\text{bias}} - 1\ V) - 2 \cdot I_{\text{leak}}^2(U_{\text{bias}})}{(1\ V)^2} \tag{6.5}$$

$-\frac{d^2}{dU_{\text{bias}}^2} I_{\text{leak}}^2$ reaches maximum when $U_{\text{bias}} = 10$ V, which is the measured full depletion voltage. This result agrees with the calculation shown in Section 3. Given this result, the sensor operates at an inverse bias voltage of 20 V, with leakage current being about 5 µA.

The shot noise from the sensor leakage current can be expressed using the following formula [41]:

$$\text{ENC}_{\text{shot}} = \sqrt{\frac{\text{e}^2}{4} \cdot q I_s \tau} \tag{6.6}$$

where e is the Euler's number, q is the elementary charge, I_s is the leakage current that flows through one strip, τ is the shaping time of the CR-RC shaping circuit of readout electronics, which is about half of the pulse width measured in Section 4.8. Considering that the total leakage current is evenly distributed in each readout strip, the noise from the leakage current fluctuation is 41 e^- and 47 e^- for P and N side strips, respectively. This noise level is small enough to be neglected compared to the target 800 e^- noise limit. As mentioned in Section

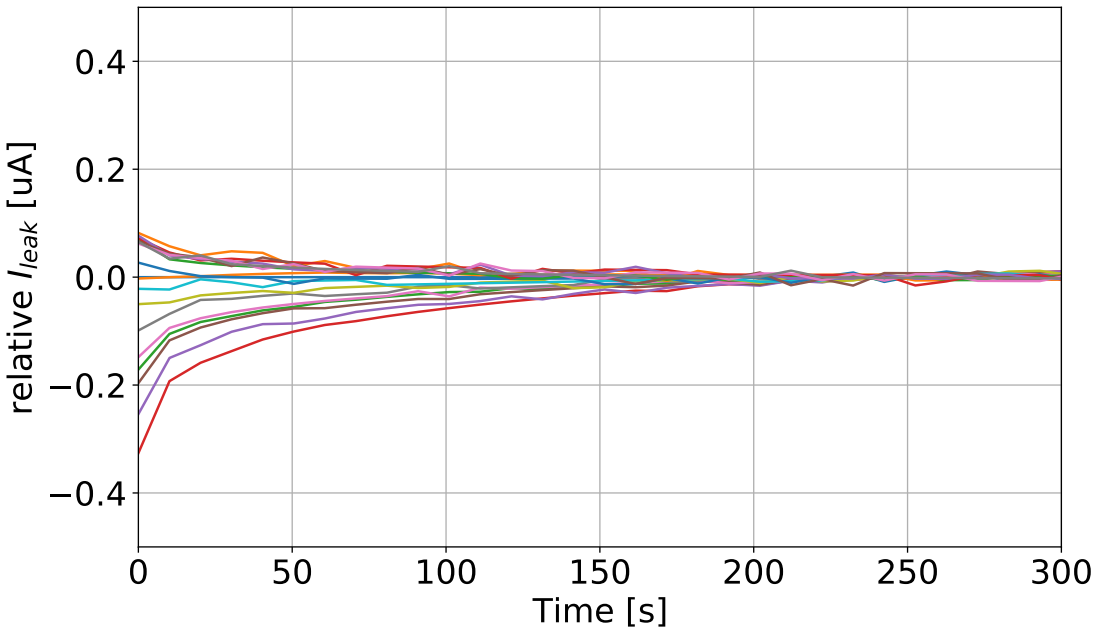


Figure 6.2: Change of relative leakage current as a function of time after changing the inverse bias voltage. The curve in different color represents measurement at different bias voltage setting. The relative leakage current is the current minus the average current in the last 100 seconds measurement at each bias voltage setting. This plot shows that it takes about 200 seconds after changing the bias voltage setting for the leakage current to become stable. The maximum of the absolute value of relative leakage current is about 0.3 µA.

1.7, the expected leakage current after 10 Mrad irradiation is about 450 µA, corresponding to a shot noise of about 380 e^-. The noise level uncertainty from the leakage current instability right after changing the bias voltage shown in Fig. 6.2 is calculated to be less than one electron, indicating that the leakage current instability does not need to be taken into account when performing noise measurement.

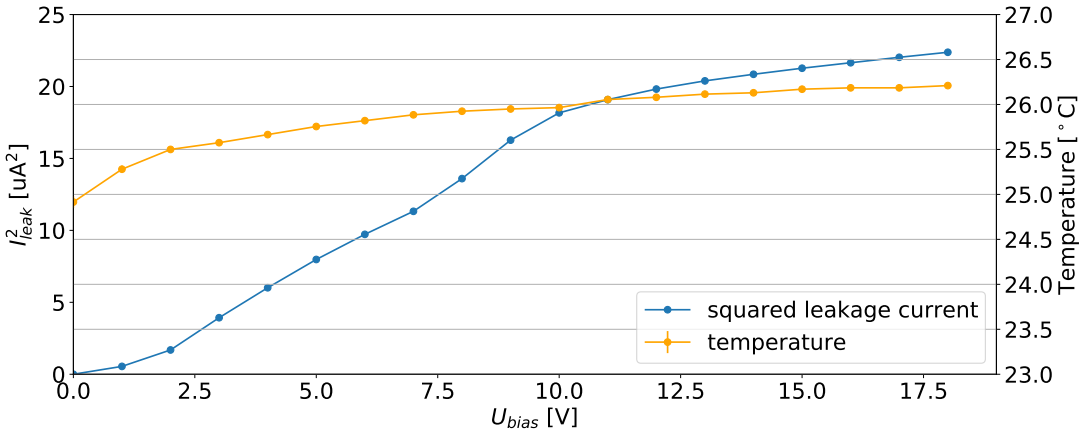


Figure 6.3: The blue line is the measured I^2_{leak} as a function of inverse bias voltage U_{bias}, ranging from 0 V to 18 V at a step of 1 V. The orange line is the average temperature during the 100 s measurement at each U_{bias}. The bar attached to the temperature represents the range of the temperature during the 100 s measurement.

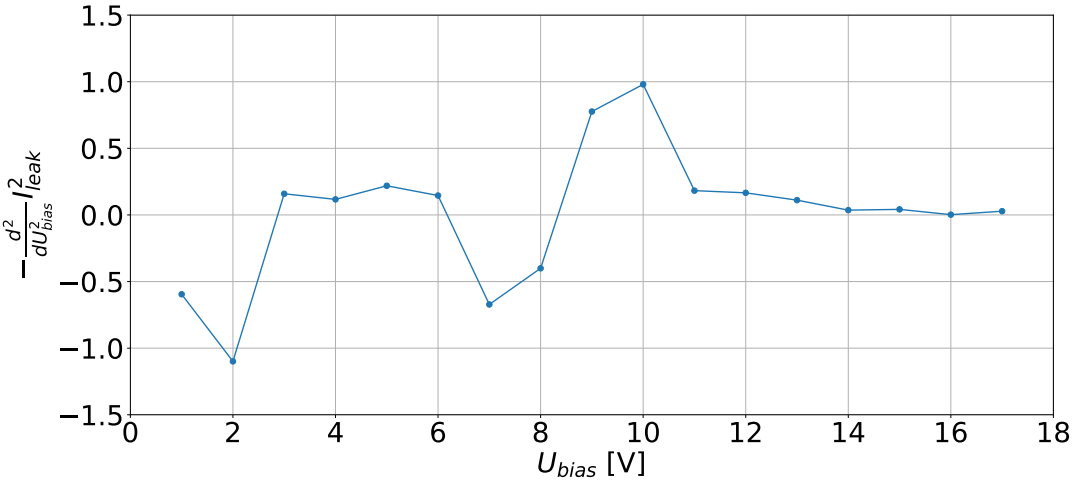


Figure 6.4: Measured $-\frac{d^2}{dU^2_{\text{bias}}} I^2_{\text{leak}}$ as a function of U_{bias}, ranging from 0 V to 18 V at a step of 1 V. $-\frac{d^2}{dU^2_{\text{bias}}} I^2_{\text{leak}}$ reaches the maximum when $U_{\text{bias}} = 10$ V, which corresponds to the full depletion voltage.

6.2 Noise level of SNAP128A with sensor connection

6.2.1 Measurement setup

The setup of the measurement is shown in Fig. 6.5. A bias voltage of 20 V is applied between the n^+ and p^+ strips, under which the TFP-DSSD sensor is fully depleted. Analog readout channels in SNAP128A are connected to the aluminum strips which are AC-coupled to the readout strips. The ground (VSS) of P side chips are connected to the negative of inverse bias voltage, while the ground of N side chips are connected to the positive of inverse bias voltage. In this experiment, only 128 out of 1024 readout strips on the P side and 256 out of 768 readout strips on the N side are connected to the SNAP128A.

As explained in Section 5.2, in this experiment, the noise of 256 channels on the N side chips connected to the sensor are evaluated and the distribution of these channels is shown in Fig. 6.6. For each of chip N2, N3 and N5, 64 continuous channels from 0 to 63 are connected to the sensor. For chip N1, 64 continuous channels from 1 to 64 are connected to the sensor, with channel 1 connected to the most left strip on the sensor in Fig. 6.6. For chip N4 and N6, no channel is connected to the sensor.

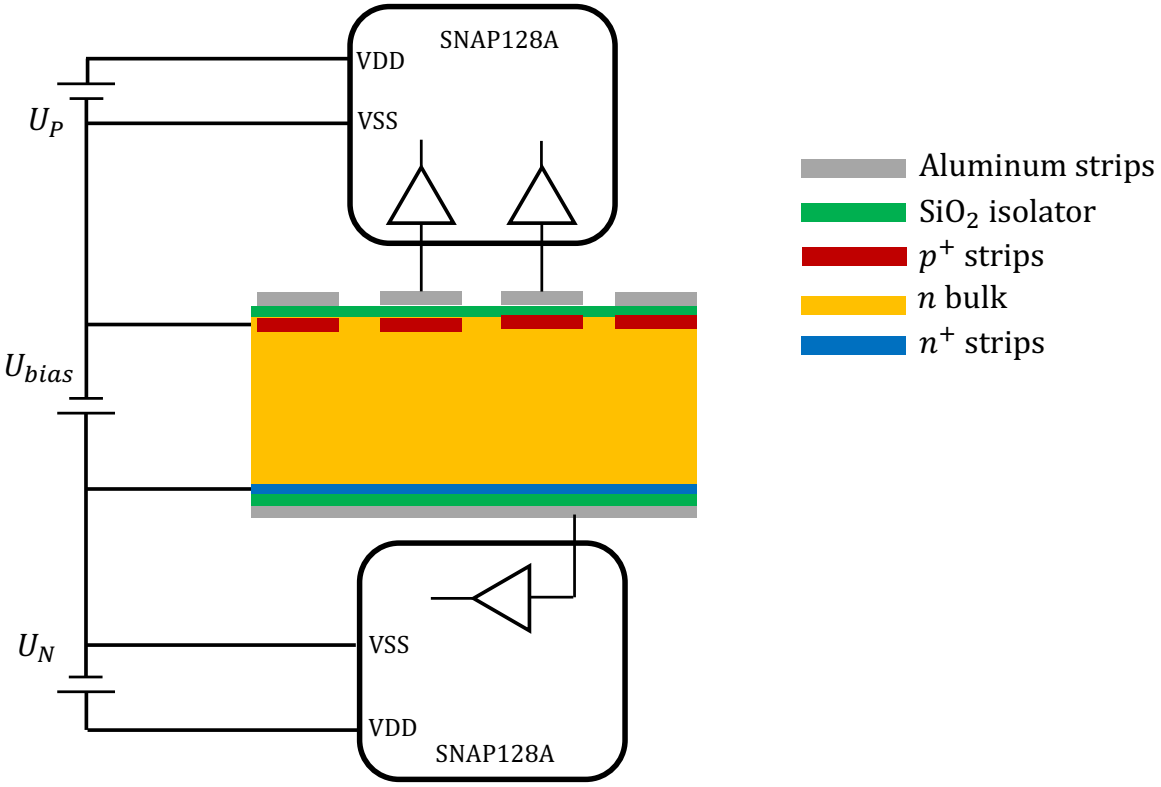


Figure 6.5: Setup of noise measurement when SNAP128A connected to TFP-DSSD readout strips. U_P and U_N represents the power supplies for the P and N side SNAP128A chips, respectively.

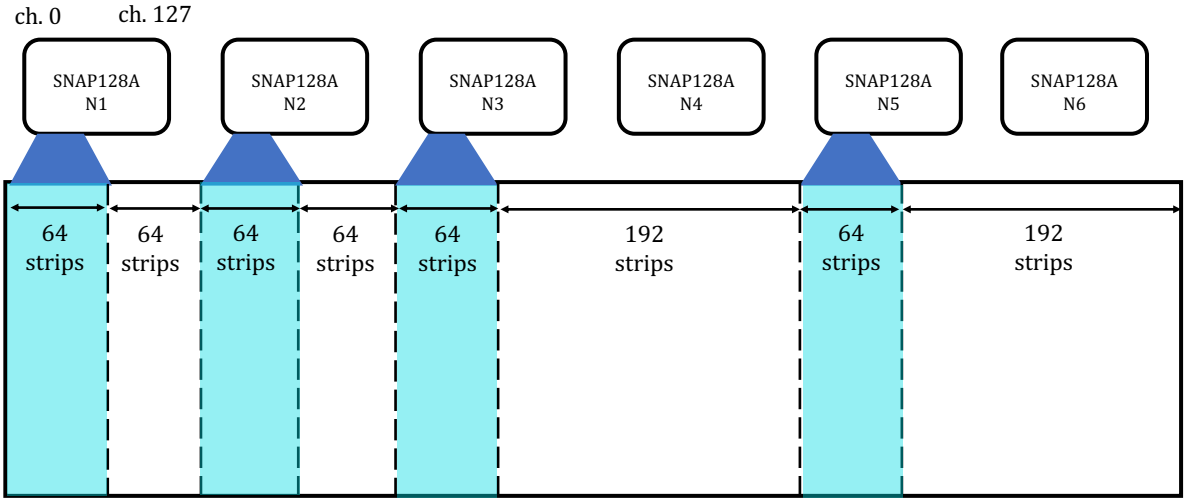


Figure 6.6: Connection map between the TFP-DSSD sensor and SNAP128A chips in the N-side. The light blue area represents the readout strips connected to SNAP128A while the white area represents the unconnected readout strips. The dark blue represents the connection between readout strips and analog input channels in SNAP128A. The number of readout channels counts from the left to the right, with channel 0 on the most left and channel 127 on the most right within one chip. The most left readout strip on TFP-DSSD sensor is connected to channel 1 of N1 chip.

6.2.2 Results and discussion

Following the analysis method mentioned in Chapter 4, the noise level of 7 channels in chip N1, N2, N3 and N5 are measured and the result is shown in Fig. 6.7.

The measured noise level of channel 0 in N1 chip, which is not connected to the TFP-DSSD sensor, is 400 electrons, being consistent with the measurement at $C_{\mathrm{det}} = 0$ pF shown in Fig. 4.26. The other channels shown in the plot are all connected to the sensor. A pattern that the noise level increases as the distance from the group of the unconnected strips decreases is observed. These unconnected aluminum strips are totally floating. They should be sensitive to incoming electromagnetic noise which can be propagated to other strips read out by the SNAP128A chips. For channel 10–63 in N1 chip, a trend that the noise level increase as the increase of the channel number can be seen, while for chip N2, N3 and N5, the noise level is lower in the middle and is larger on the left and right sides. For N1 chip, the floating strips exist only on the side with bigger channel number. On the other hand, for N2, N3 and N5 chips, the floating strips exist on both sides of the connected strips.

Even for the channels that should be most far away from the floating strips, their noise level is still much higher than the 800 e^- noise limit. The noise level of channel 30 of all chips is measured to be about 1700-2000 electrons and that of channel 20 of N1 chip is 1450 electrons. Two possibilities are proposed to explain this phenomenon. The first possibility is that the floating strips still affects channels not neighboring to the floating strips. The second possibility is that the inter-strip capacitance between two adjacent aluminum strips on the N side of the sensor is much higher than the designed 6.5 pF, resulting in a much higher noise

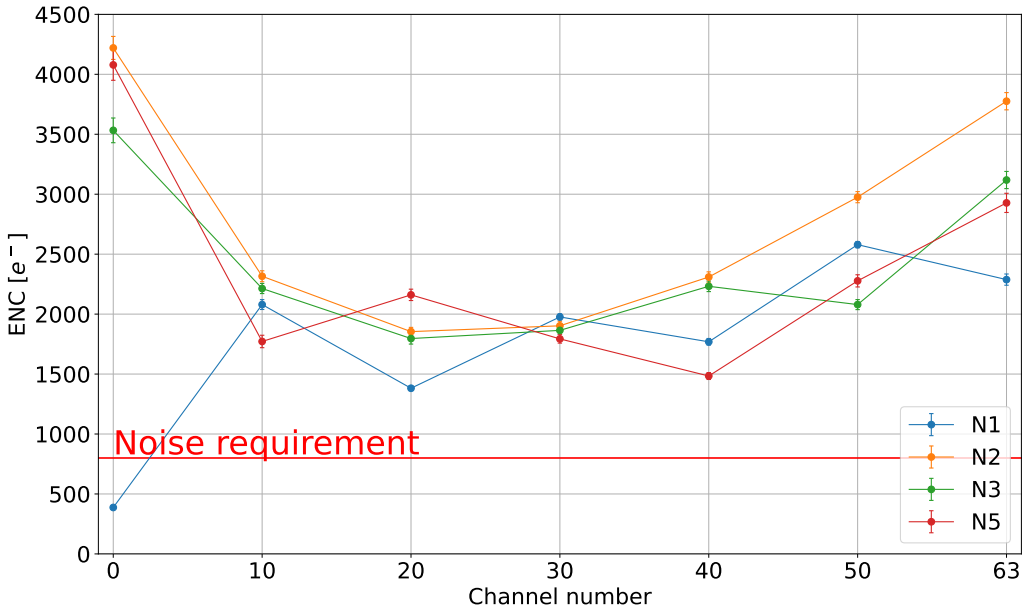


Figure 6.7: Noise level of 4 different SNAP128A chips. Except for channel 0 of N1 chip, the other channels shown in this plot are all connected to the TFP-DSSD sensor. For chip N1, the noise level increases as the increase of channel number. For chip N2, N3 and N5, the noise level is lower in the middle and is much larger on the left and right sides. The noise level of channel 30 for all chips is about 1700–2000 electrons, higher than the design requirement of 800 electrons.

from detector capacitance.

To verify these two hypothesis and reduce the noise level, in the next steps of the experiment, we plan to connect all the readout strips on the sensor to the SNAP128A, or connect them to the ground to eliminate the floating strips on the sensor. We also plan to perform a direct measurement of inter-strip capacitance of TFP-DSSD sensor [42].

6.3 Summary and remaining studies

In this experiment, the noise level of multiple SNAP128A chips are measured simultaneously, indicating a good performance of the upgraded performance evaluation platform, including the test board, firmware and software system. This platform is the cornerstone of the TFP-SVD evaluation experiment.

The full depletion voltage of the 150 µm thick TFP-DSSD prototype sensor is measured to be 10 V, which agrees with the expectation. Thus, the inverse bias voltage of the sensor in the following experiments is set to 20 V and the corresponding leakage current is measured to be 5 µA at an environment temperature of 25 °C. Given the measured shaping time of SNAP128A being about 27 ns, the shot noise from the fluctuation of leakage current is calculated to be

about 41 e^- and 47 e^- for P and N side, respectively. This noise contribution is small enough to be neglected compared to the 800 e^- noise limit.

The noise level of 7 channels in 4 different chips shows a pattern that the noise level is larger for strips close to the floating strips. However, even for the strips not neighboring to the floating strips, the noise level is about 1800 e^-, much larger than the noise limit. This remains to be the most important problem to be solved in the next stage of the evaluation. We are planning to measure the noise level with the floating strips eliminated and measure the inter-strip capacitance of TFP-DSSD sensor.

After the noise evaluation, the next step is the measurement of the sensor efficiency and signal charge using the cosmic rays and accelerator beams.

Chapter 7

Conclusion

7.1 Achievements

Despite the great success of the SM in describing most of the experimental results, it is considered not to be the ultimate theory and people are searching for new physics beyond the SM, especially the new physics whose energy scale is beyond TeV. The Belle II experiment, standing in the frontier of the particle physics experiment, searches for new physics by measuring observables precisely and seeking for deviations between theoretical prediction and experimental results. The Belle II aims to accumulate a large data set of $50\,\mathrm{ab}^{-1}$ and to make this target achievable in reasonable time span, the KEKB collider was upgraded to SuperKEKB, aiming to reach an instantaneous luminosity of $6 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

The high luminosity also results in the high beam background, which degrades the performance of the SVD due to the large hit occupancy and the radiation damage. The SVD occupancy at the target luminosity of the SuperKEKB was estimated as the MC simulation prediction scaled by data/MC ratios, which are the ratio between the measurement and simulation results under the known machine conditions. This thesis gave the first measurement of data/MC factor for the SVD luminosity background, which is evaluated to be 0.74. Based on this result, the beam background projection near the target luminosity is re-scaled, with occupancy, TID and NIEL of SVD Layer 3 sensor becoming 2.7%, 0.20 Mrad/smy and $4.6 \times 10^{11}\,\mathrm{neq}/(\mathrm{cm}^2\,\mathrm{smy})$, with a reduction of about 10% compared to the previous results. However, the ratio of occupancy limit 5.0% over the new expected occupancy 2.7% is about 1.9, still below the desired safety margin 5 and the motivation for the SVD upgrade does not change.

A better physics performance and stronger beam background tolerance of the SVD is expected at the future operation of the Belle II, the TFP-SVD upgrade plan is proposed to replace the current SVD and possibly the inner layers of the CDC. The first prototypes of the new TFP-DSSD sensor and new front-end ASIC SNAP128 is produced and the performance is being evaluated at KEK, Tsukuba (Japan).

A dedicated SNAP128A performance evaluation platform was established from the scratch. A testboard that provides the power supply and interface for its communication to readout FPGA was developed. The corresponding readout firmware and software was developed for controlling the chip and read out the binary hit information output from the SNAP128A.

The design of SNAP128 is to be iterated several times to optimize the performance in the future. As the first prototype, SNAP128A has already achieved various required performance. The power consumption is measured to be 329 mW/chip, smaller than the 400 mW/chip

requirement. For the negative signal the waveform is successfully reconstructed from the binary hit information and the pulse width is measured to be about 55 ns. The result is consistent with the simulation. The measured pulse height at target detector capacitance (15 pF) is about 70% of simulation and acceptable in the real operation. The measured noise for negative signal at the target detector capacitance is about 1200 electrons, which is over the requirement of 800 electrons and is about 60% larger than the simulation expectation. It is possible that this large noise is due to the parasitic capacitance on the test board. For the positive signal, saturation of reconstructed shaper output is observed and the mechanism of saturation was qualitatively studied with simulation. While the saturation issue and large-noise issue are discovered by the performance evaluation, the successful reconstruction and measurement of negative shaper output indicates that this chip can be assembled with a TFP-DSSD sensor and measure the noise level when connecting the analog input channel to sensor and detect particles.

To evaluate the performance of the TFP-DSSD sensor, a new testboard is developed to apply inverse bias voltage to the sensor and connect the sensor to the SNAP128A readout ASICs. The corresponding readout and controlling firmware and software are also upgraded for multi-chip controlling and readout.

The full depletion voltage of the 140 µm thick TFP-DSSD prototype sensor is measured to be 10 V, which agrees with the expectation. Thus, the inverse bias voltage of the sensor in the following experiments is set to 20 V and the corresponding leakage current is measured to be 5 µA at an environment temperature of 25 °C. The leakage current after 10 Mrad is estimated to be about 450 µA, corresponding to a shot noise of about 380 e^-. The noise level of 28 channels in 4 different chips is measured and shows a similar spatial dependence that the noise level is larger for strips close to the area of the unconnected strips. However, even for the strips far from the unconnected strips, the noise level is about 1800 e^-, much larger than the noise limit. This remains to be the most important problem to be solved in the next stage of the evaluation. We are planning to measure the noise level with the floating strips eliminated and measure the inter-strip capacitance of TFP-DSSD sensor.

7.2 Remaining studies

In order to achieve a better understanding of the performance of SNAP128A and TFP-DSSD sensor, further experiments need to be performed and are described in this section.

In the evaluation of the SNAP128A, we plan to reproduce the test board with a improved layout design such that the parasitic capacitance on the test board is reduced. With the new test board, a more accurate measurement of noise in SNAP128A can be derived.

In the next prototype of SNAP128, we will improve the chip design to reduce the noise and to avoid the positive signal saturation, which are two major problems found in this evaluation. We plan to move the target position of the inner most TFP-SVD layer a little bit outside, with which the requirements on the hit rate and beam background tolerance are released. Based on this, the time constant of the CR-RC shaper circuit can be larger. In addition, by making a sensor with smaller size, the inter-strip capacitance from the sensor is also smaller. With a larger time constant and smaller inter-strip capacitance, the noise in the readout ASIC can be suppressed. As for avoiding the saturation, a series of the comparator design with different working range of the shaper output is being prepared. We will try to find the most proper one for the SNAP128. We will also prepare a comparator with selectable polarities when dealing with positive and negative signal. Other problems found in this evaluation will also be

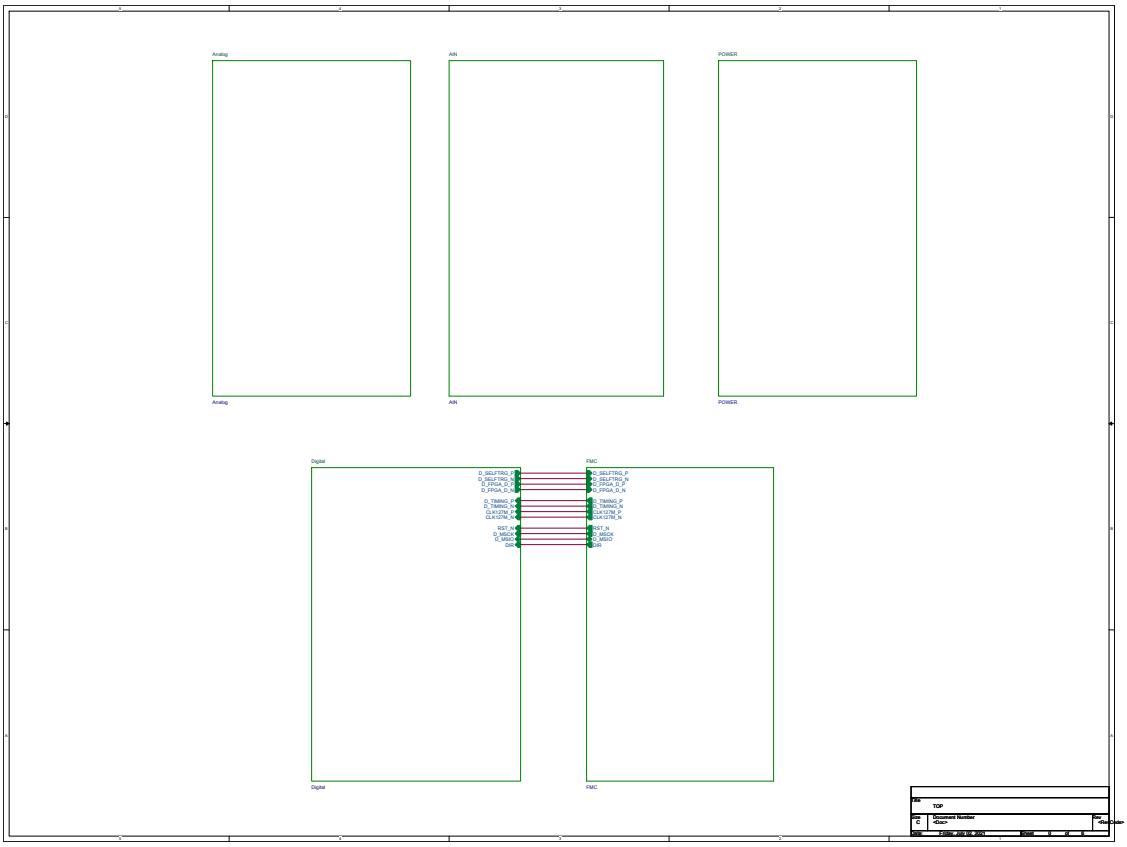
improved in the next design such as the non-linearity in the comparator threshold DAC.

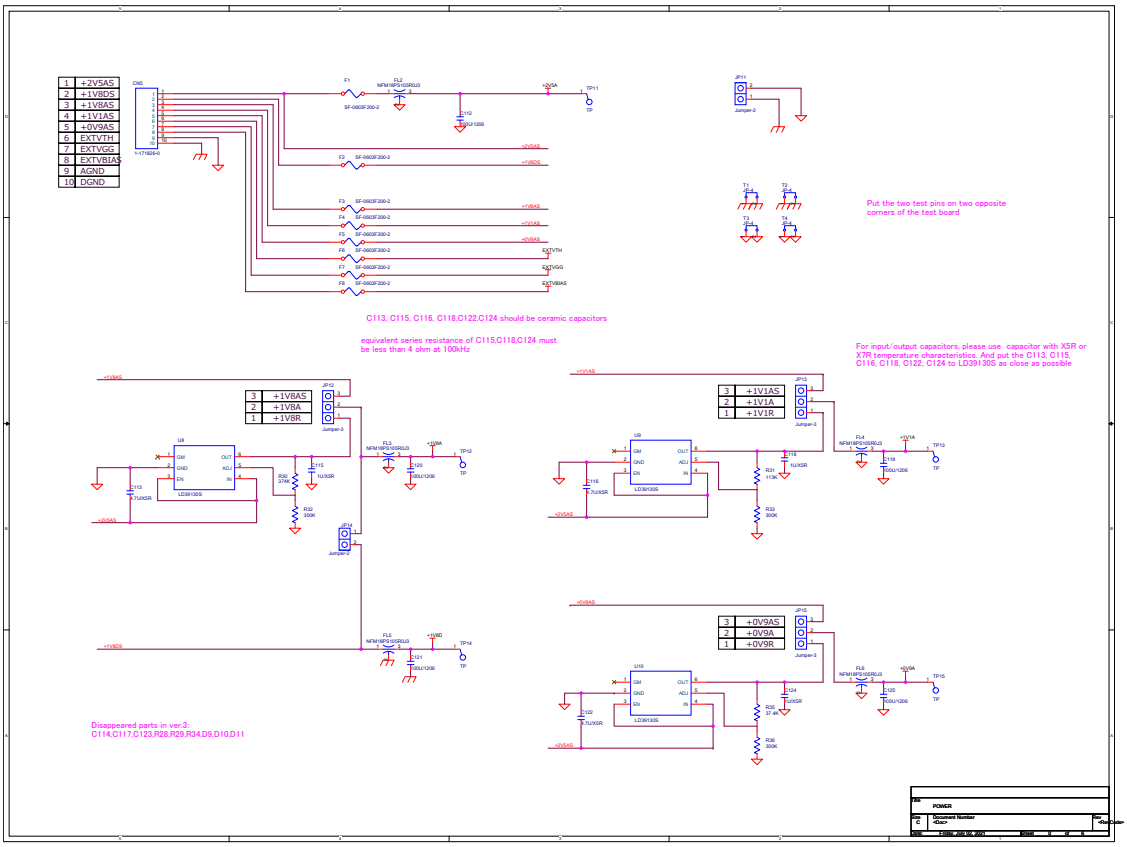
As for the sensor evaluation, the most important problem left is the evaluation of the noise of readout chip connected to the sensor. Firstly, we will connect all of the aluminum strips on the sensor to readout chip or to the ground to eliminate the unconnected strips and remeasure the noise. In the meantime, we will also measure the sensor inter-strip capacitance.

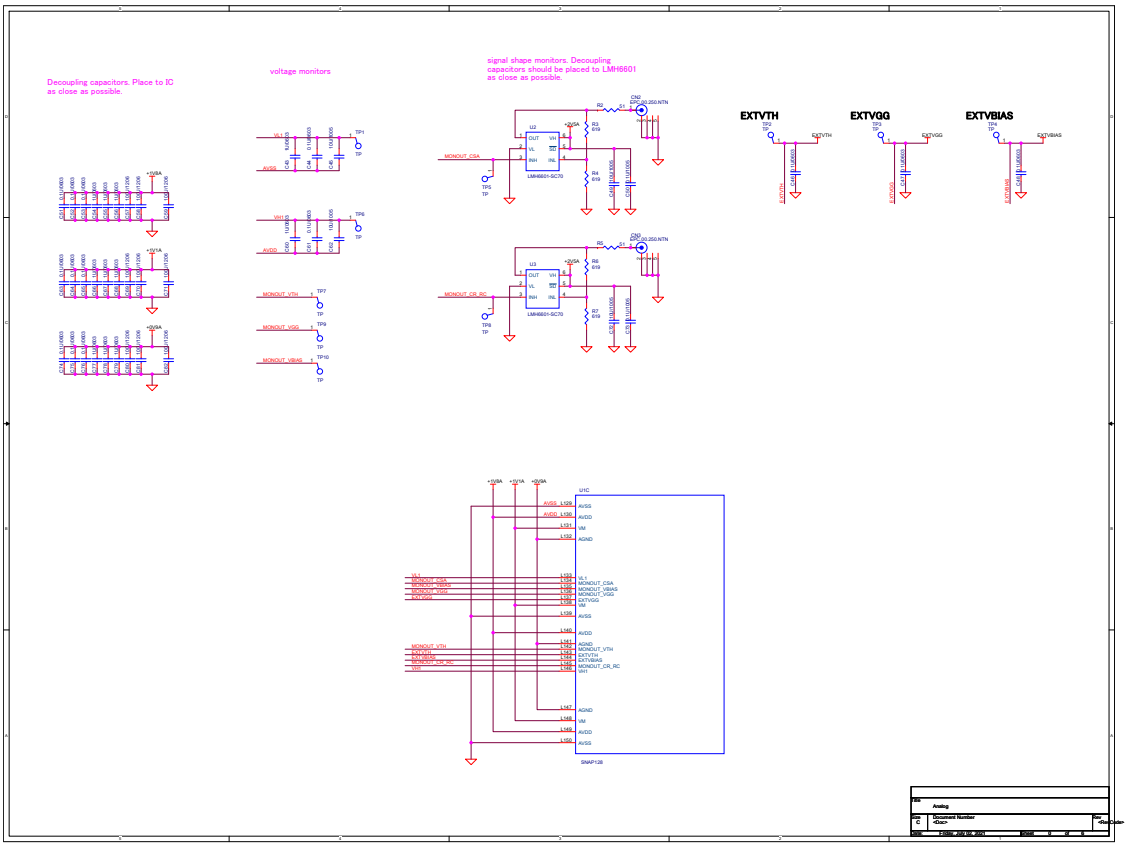
As a long term target of sensor evaluation, we will measure the detector efficiency and signal charge using the cosmic ray and accelerator beam.

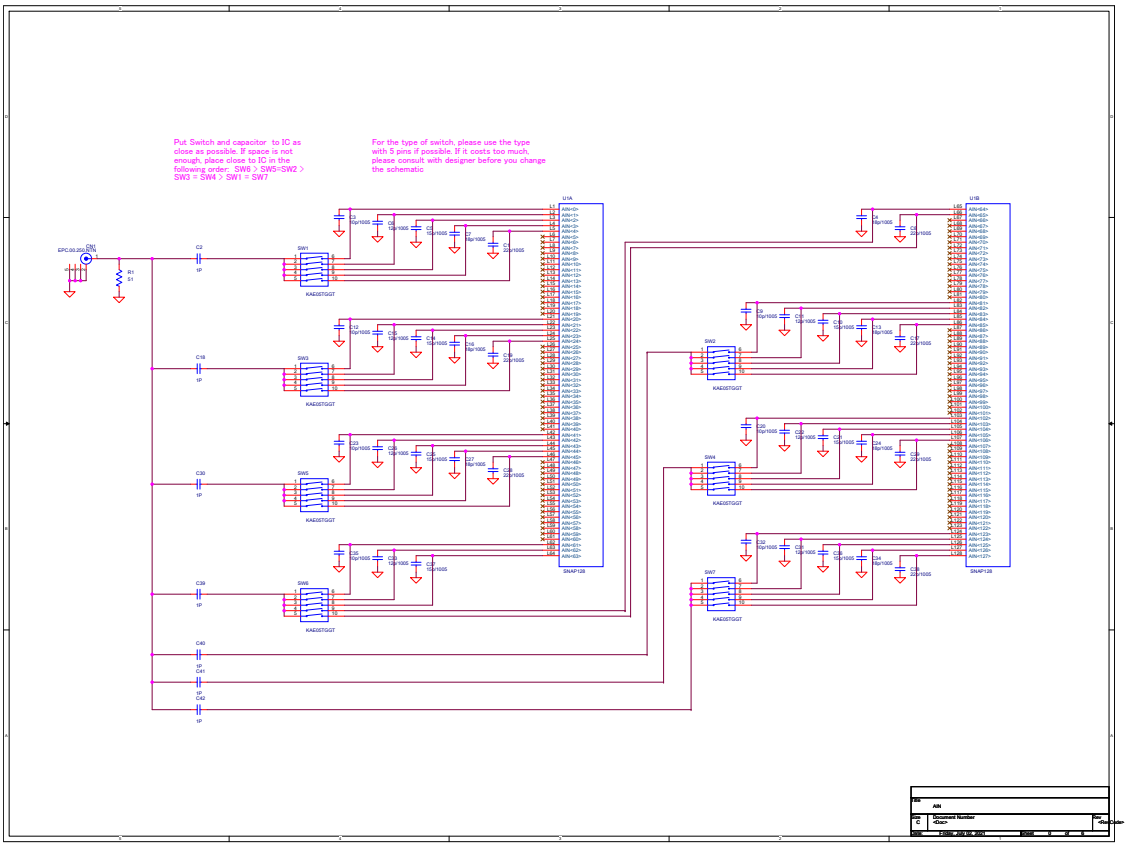
Appendix A

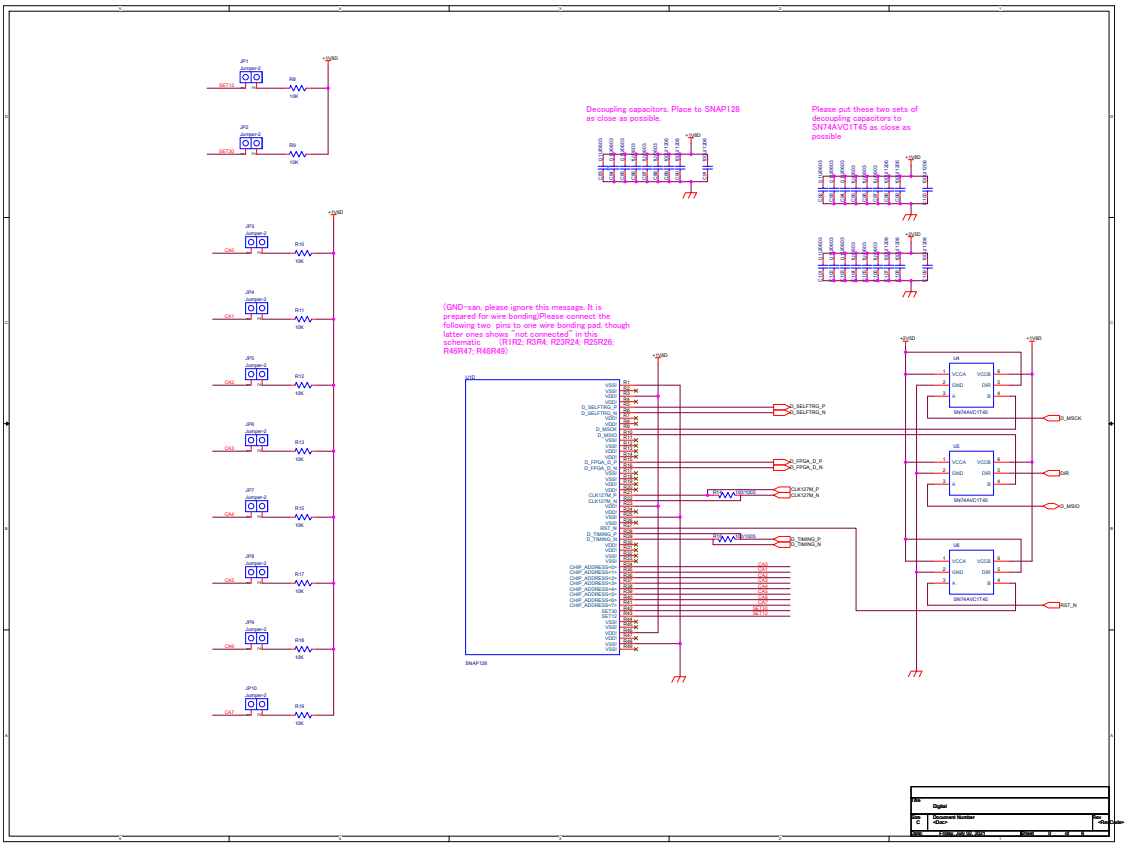
Design of SNAP128 test board

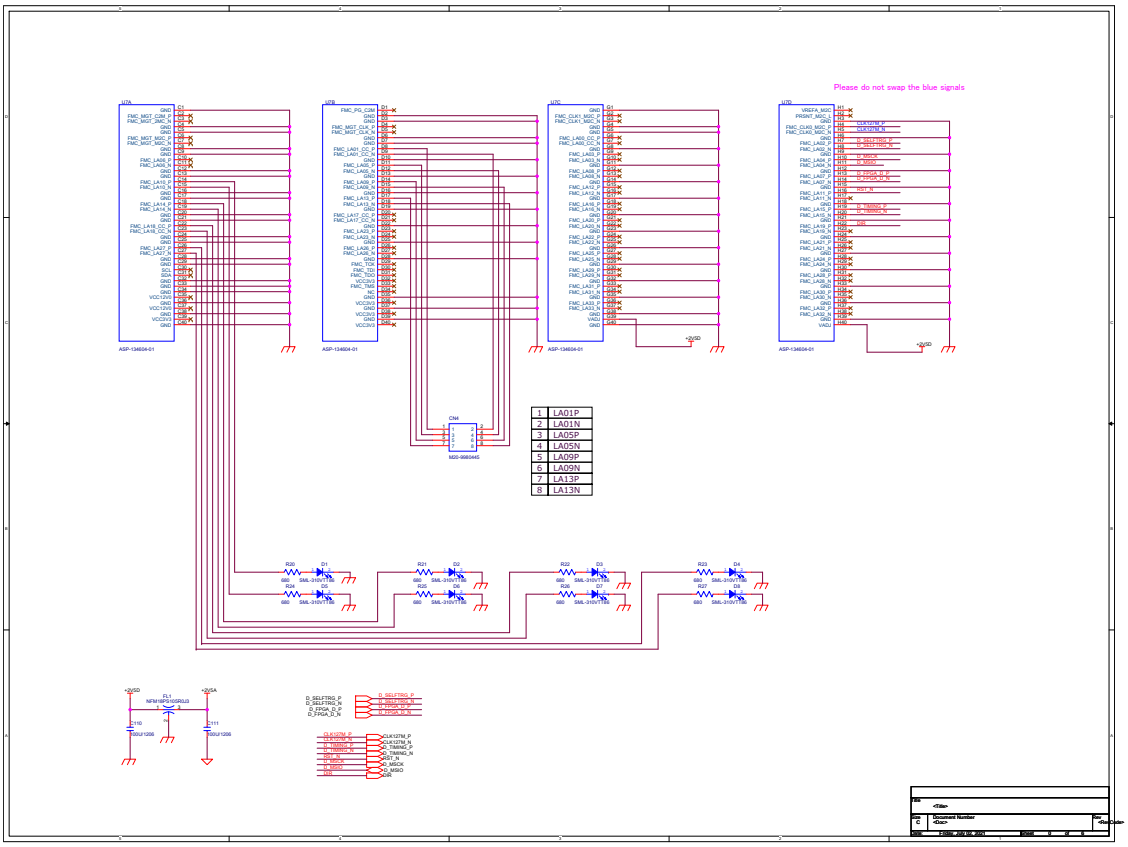



+2V5AS
+1V8DS
+1V8AS
+1V1AS
+0V9AS
EXTVTH
EXTVGG
EXTVBIAS
AGND
DGND
Put the two test pins on two opposite corners of the test board
C113, C115, C116, C118,C122,C124 should be ceramic capacitors
equivalent series resistance of C115,C118,C124 must be less than 4 ohm at 100kHz
For input/output capacitors, please use capacitor with X5R or X7R temperature characteristics. And put the C113, C115, C116, C118, C122, C124 to LD39130S as close as possible
+1V8AS
+1V8A
+1V8R
+1V1AS
+1V1A
+1V1R
+0V9AS
+0V9A
+0V9R
Disappeared parts in ver.3:
C114,C117,C123,R28,R29,R34,D9,D10,D11
POWER


Decoupling capacitors. Place to IC as close as possible.
voltage monitors
signal shape monitors. Decoupling capacitors should be placed to LMH6601 as close as possible.
EXTVTH
EXTVGG
EXTVBIAS
MONOUT_CSA
MONOUT_CR_RC
LMH6601-SC70
MONOUT_VTH
MONOUT_VGG
MONOUT_VBIAS
SNAP13B
Analog

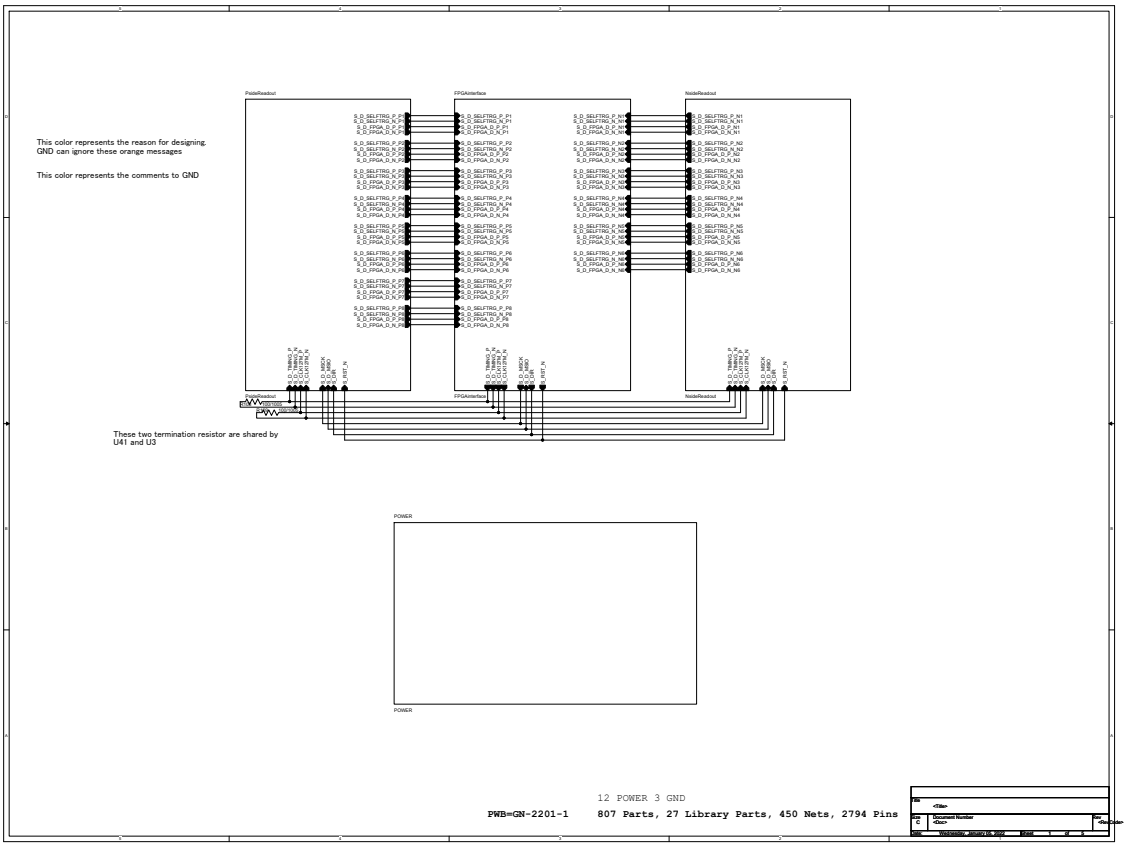

Put Switch and capacitor to IC as close as possible. If space is not enough, place close to IC in the following order: SW6 > SW5>SW2 > SW3 = SW4 > SW1 = SW7
For the type of switch, please use the type with 5 pins if possible. If it costs too much, please consult with designer before you change the schematic
U1A
U1B
SW1
SW2
SW3
SW4
SW5
SW6
SW7
KAE05TGGT
SNAP128
AIN
Document Number
<Doc>
<Rev Code>

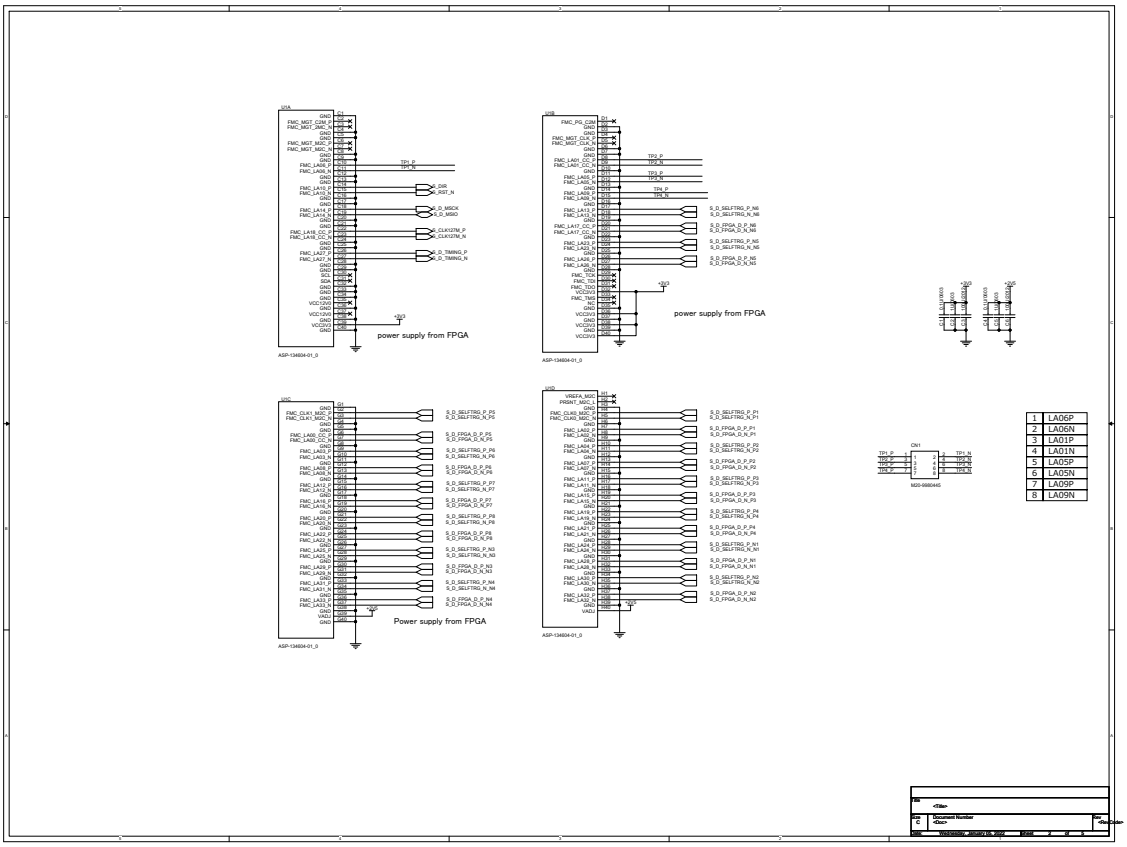

Decoupling capacitors. Place to SNAP128 as close as possible.
Please put these two sets of decoupling capacitors to SN74AVC1T45 as close as possible
(GND~san, please ignore this message. It is prepared for wire bonding!Please connect the following two pins to one wire bonding pad, though latter ones shows "not connected" in this schematic (R1R2; R3R4; R22R24; R25R26; R46R47; R48R49)
SNAP128
SN74AVC1T45
Digital

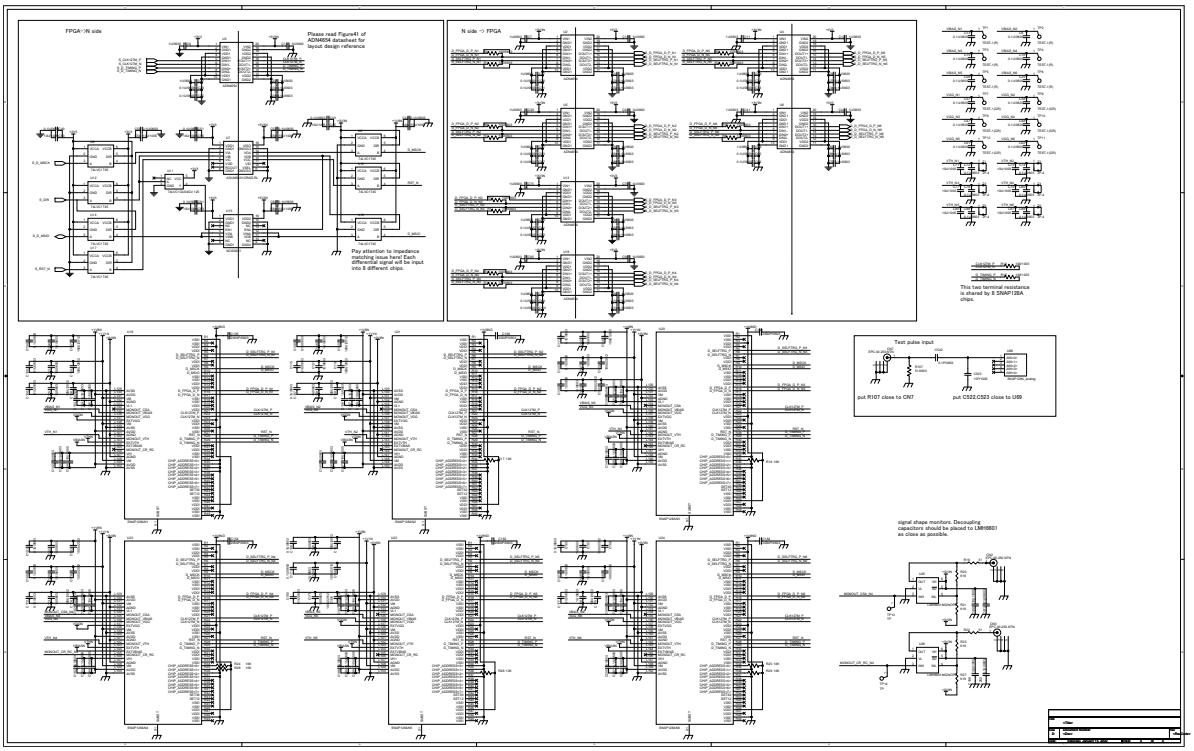

Please do not swap the blue signals
U2A
U2B
U2C
U2D
ASP-134604-01
CN4
MDD-068044S
1 LA01P
2 LA01N
3 LA05P
4 LA05N
5 LA09P
6 LA09N
7 LA13P
8 LA13N
FL1
NFM18PS105R0J3
C110
C111
100U/1206
D_SELFTRG_P
D_SELFTRG_N
E_FPGA_D_P
E_FPGA_D_N
CLK127M_P
CLK127M_N
SD_TIMING_P
SD_TIMING_N
SD_MSCK
SD_MSDO
SD_MSDI
Size
Document Number
Rev
Date
File
Title

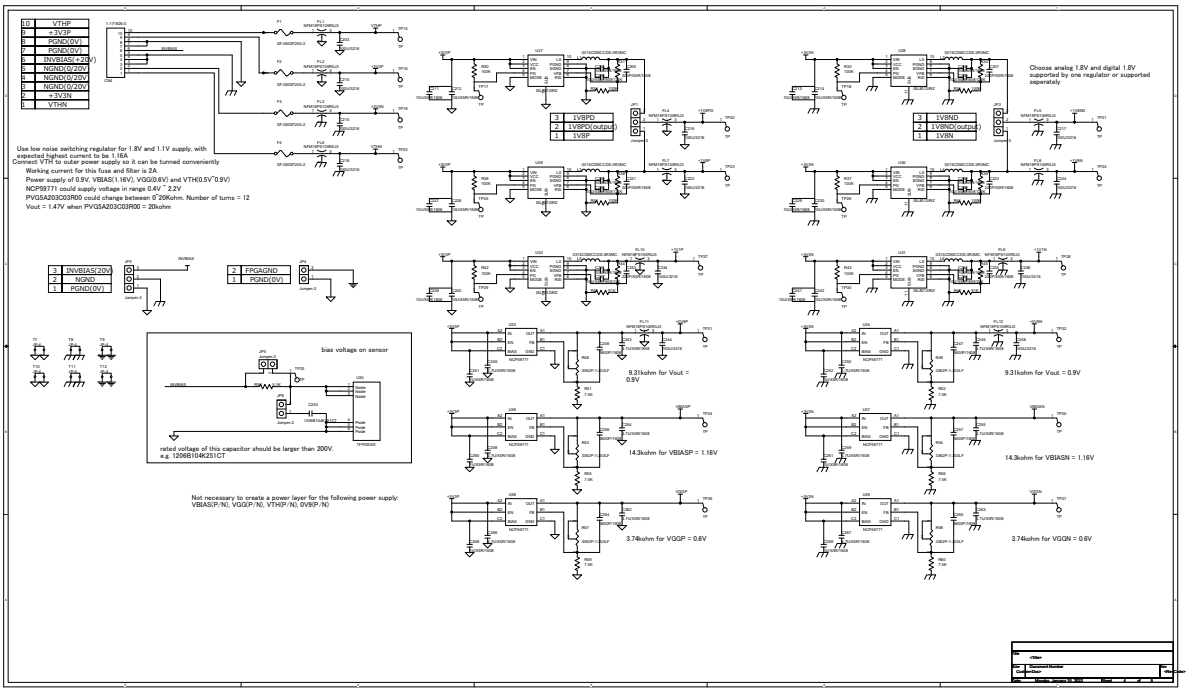
Appendix B

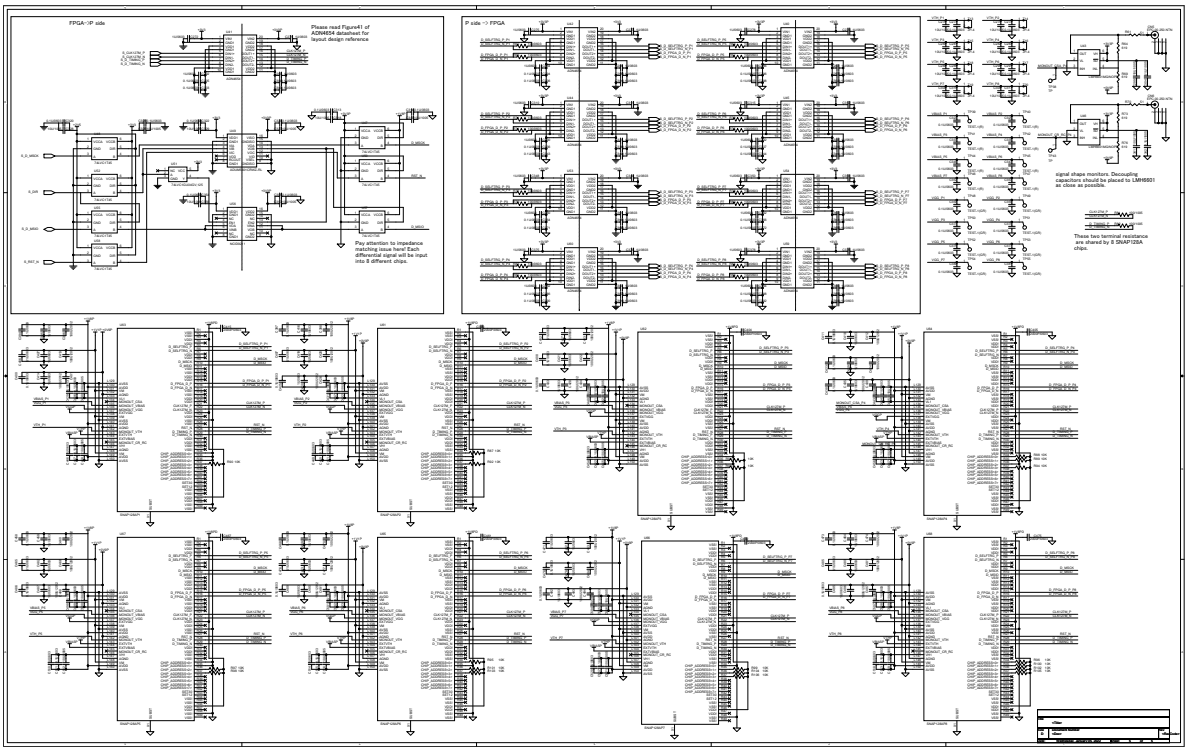
Design of TFP-SVD test board




power supply from FPGA
power supply from FPGA
Power supply from FPGA
1 LA06P
2 LA06N
3 LA01P
4 LA01N
5 LA05P
6 LA05N
7 LA09P
8 LA09N


FPGA□IN side
Please read Figure41 of ADN4604 datasheet for layout design reference
Pay attention to impedance matching issue here! Each differential signal will be input into 8 different chips.
N side -> FPGA
This two terminal resistance is shared by 8 SNAP128A chips.
Test pulse input
put R107 close to CN7
put C522,C523 close to U69
signal sheee monitors. Decoupling capacitors should be placed to LMH6801 as close as possible.


10 VTHP
9 +3V3P
8 PGND(0V)
7 PGND(0V)
6 INVBIAS(+2.2V)
5 NGND(0.2V)
4 NGND(0.2V)
3 NGND(0.2V)
2 +3V3N
1 VTHN
Use low noise switching regulator for 1.8V and 1.1V supply, with expected highest current to be 1.16A
Connect VTH to outer power supply so it can be tunned conveniently
Working current for this fuse and filter is 2A
Power supply of 0.9V, VBIAS(1.16V), VGG(0.6V) and VTH(0.5V~0.9V)
NCP59771 could supply voltage in range 0.4V ~ 2.2V
PVG5A203C03R00 could change between 0~20Kohm. Number of turns = 12
Vout = 1.47V when PVG5A203C03R00 = 20kohm
3 INVBIAS(20V)
2 NGND
1 PGND(0V)
2 FPGAGND
1 PGND(0V)
bias voltage on sensor
rated voltage of this capacitor should be larger than 200V.
e.g. 1206B104K251CT
Not necessary to create a power layer for the following power supply:
VBIAS(P/N), VGG(P/N), VTH(P/N), 0V9(P/N)
3 1V8PD
2 1V8PD(Output)
1 1V8P
3 1V8ND
2 1V8ND(Output)
1 1V8N
Choose analog 1.8V and digital 1.8V supported by one regulator or supported seperately
9.31kohm for Vout = 0.9V
14.3kohm for VBIASP = 1.16V
3.74kohm for VGGP = 0.6V
9.31kohm for Vout = 0.9V
14.3kohm for VBIASN = 1.16V
3.74kohm for VGGN = 0.6V


FPGA->P side
Please read Figure41 of AD9434 datasheet for layout design reference
Pay attention to impedance matching issue. Each differential signal will be input into 8 different chips.
P side -> FPGA
signal shape monitors. Decoupling capacitors should be placed to LMH6601 as close as possible.
These two terminal resistance are shared by 8 SNAP12BA chips.

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