Master's Thesis

Development of monitoring system and performance evaluation for Belle II data acquisition system
(Belle II データ取得システムの監視機構の開発および性能評価)

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Abstract

The Belle II experiment is a B-factory experiment hosted by KEK in Tsukuba, Japan. Belle II experiment is the successor of the Belle experiment, which observed CP violation in the B-meson system. Belle II experiment observes decay products of the B-meson pairs created by the SuperKEKB accelerator by the Belle II detector to find new physics beyond the standard model. The luminosity of e^- and e^+ collision of SuperKEKB accelerator is upgraded to 40 times higher than that of KEKB accelerator in Belle experiment to obtain abundant statistics, thereby the trigger rate for Belle II experiment is expected to increase up to 30kHz. Therefore, in the data acquisition system, we need to handle large data throughput from the whole Belle II detector under a sufficiently small dead time. to supervise and evaluate dead time in data acquisition, a monitoring system for dead time in the data acquisition system is implemented in this thesis. The performance of the data acquisition system in 2019 physics run is evaluated using the monitoring system, and it is confirmed that we can obtain data under 0.1% dead time with a 5kHz trigger rate. In addition to the dead time monitoring, possible bottlenecks of data flow in the data acquisition system are evaluated. If the data throughput rate exceeds the bandwidth of the potential bottlenecks, the large dead time arises due to the backpressure. Therefore, the data rate under high luminosity must be below the potential bottlenecks. In this thesis, the data size under high luminosity is evaluated, and the effect of planned data acquisition system upgrades on those potential bottlenecks is discussed.

Contents

1 Introduction

In today's elementary particle physics, the Standard Model (SM) describes most of the phenomenon in elementary particle physics. SM describes electromagnetic, weak and strong interaction, and consist of 3 generation quark and lepton, gauge boson which intermediate interaction, and Higgs boson. On the other hand, there exists phenomeno which cannot be explained by SM. Various types of experiments are carried out around the world to search for new physics beyond SM.

CP violation in K meson system is first observed in 1964 [4]. In 1973, Kobayashi-Maskawa theory explained the CP violation within SM [9]. Belle experiment, which started data taking in 1999, is a experiment to generate large amount of B meson pairs and observe CP violation in B meson system. Belle experiment is carried out in High Energy Accelerator Research Organization (KEK) at Tskuba, Japan. B meson pairs are produced by KEKB accelerator and the decay process of B meson was observed by Belle detector. Belle experiment succeeded to observe CP violation in B meson and proved the Kobayashi-Maskawa theory.

SM describes most of phenomenon successfully, while there exists problems which cannot be explained by SM. For example, mass hierarchy, neutrino mass, dark matter and dark energy [10]. Belle experiment did not find hint larger than 3 sigma to the new physics beyond SM due to the large statistics error. Based on these background, Belle II experiment is planned as an upgrade of Belle experiment. In Belle II experiment, KEKB accelerator is also upgraded to SuperKEKB accelerator, and aiming to obtain 50 times larger statistics than Belle experiment.

1.1 Physics background

CP violation was first observed in 1964 [4]. K_L usually decays to three π mesons, which is CP odd eigenstate. On the other hand, in the experiment K_L meson was observed to decay to 2 π meson, which is CP even eigenstate. In 1973, M.Kobayashi and T.Maskawa proposed a theory which explains the origin of CP violation within the range of standard model. Kobayashi-Maskawa theory predicted that CP violation occurs if 3 generation, 6 species of quark exist.

The mixing of quarks between generations through weak interaction is described

by Cabibbo-Kobayashi-Maskawa (CKM) matrix in Eq.1

$$V_{\rm CKM} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix}. \tag{1}$$

In the CKM matrix, each component V_{ij} represents transition amplitude from quark j to quark i $(i = u, c, t), j = (d, s, b)$. Using the CKM matrix the mass eigenstate (d, s, b) and flavor eigenstate (d', s', b') can be combined as

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = V_{\rm CKM} \begin{pmatrix} d \\ s \\ b \end{pmatrix}. \tag{2}$$

$V_{\rm CKM}$ can be written in Wolfenstein representation as

$$V_{\rm CKM} = \begin{pmatrix} 1 - \frac{1}{2}\lambda^2 & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{1}{2}\lambda^2 & A\lambda^2 \\ A\lambda^3(\rho - i\eta) & V_{ts} & V_{tb} \end{pmatrix}. \tag{3}$$

$V_{\rm CKM}$ is unitary matrix, thus $V_{\rm CKM}$ satisfies

$$V_{CKM}^{\dagger} V_{\rm CKM} = 1. \tag{4}$$

This equation leads to

$$V_{ub}^* V_{ud} + V_{cb}^* V_{cd} + V_{tb}^* V_{td} = 0. \tag{5}$$

The terms $V_{ij}^* V_{ik}$ can be interpreted as a vector on complex plane, thus condition 5 draws triangle on complex plane as is in Fig.1.

Those ϕ_1, ϕ_2, and ϕ_3 can be represented using V_{ij} in CKM matrix.

$$\phi_1 = arg\left(\frac{V_{cb}^* V_{cd}}{V_{tb}^* V_{td}}\right), \tag{6}$$

$$\phi_2 = arg\left(\frac{V_{ub}^* V_{ud}}{V_{tb}^* V_{td}}\right), \tag{7}$$

$$\phi_3 = arg\left(\frac{V_{cb}^* V_{cd}}{V_{ub}^* V_{ud}}\right). \tag{8}$$

If this triangle is closed, Kobayashi-Maskawa theory is proved and we can explain CP violation within SM, thus it is important to measure those angles precisely. In

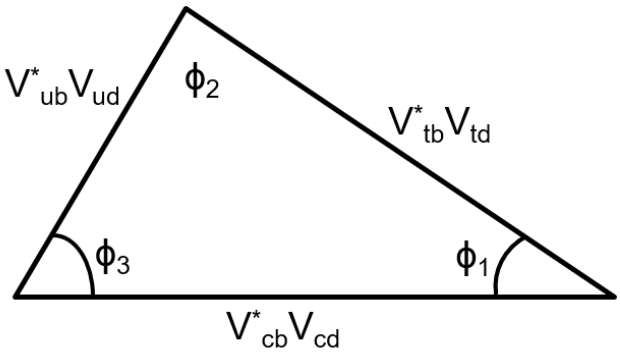


Fig. 1: Unitarity triangle. The closed triangle can be drawn from the unitarity of V_{CKM}

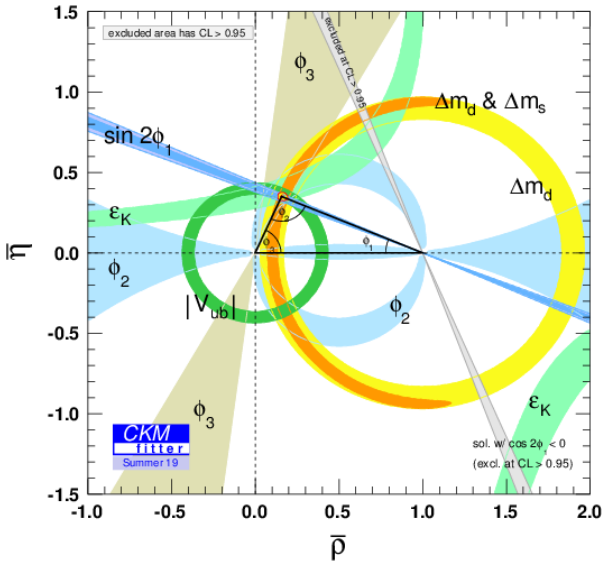


Fig. 2: The constraints of Wolfenstein parameters $(\overline{\rho}, \overline{\eta})$ [3]. Each colored area represents the 95% CL area. The red hashed region represents the 68% CL region of the vertex of unitarity triangle.

order to validate SM and to search new physics beyond SM, various experiments have been measured length of each side or angles of unitarity triangles.

The latest constraints of Wolfenstein parameters $(\overline{\rho}, \overline{\eta})$ from various experiments is shown in Fig.2 [3].

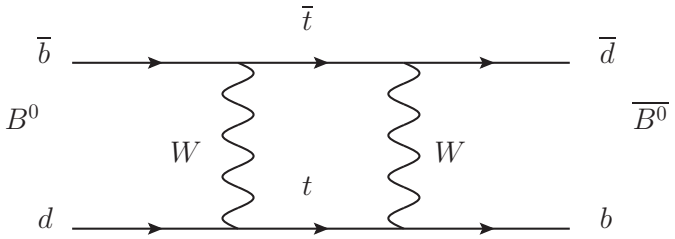


Fig. 3: Feynman diagram for B^0-$\overline{B}^0$ mixing. The neutral B mesons can change its flavor via loop diagram.

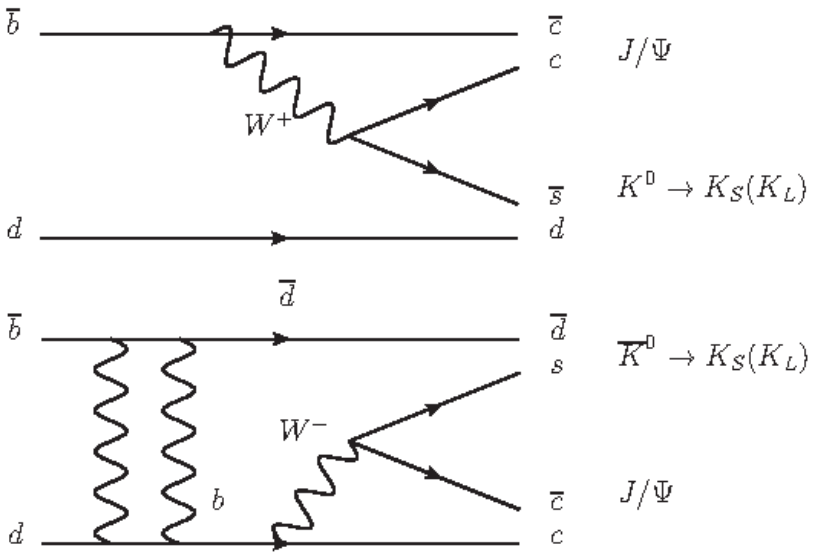


Fig. 4: Feynman diagram for $B^0 \to J/\Psi K_S$. In the lower diagram, initial B^0 transits to $\overline{B}^0$ and decays into $J/\Psi K_S$

1.2 B factory experiment

In Belle, $\Upsilon(4S)$ meson is produced by electron positron collision, and $\Upsilon(4S)$ decays to $B^0\overline{B}^0$. Those neutral B mesons are produced in one state of two possible flavor state $|B^0\rangle\,(\bar{b}q)$ or $|\overline{B}^0\rangle\,(b\bar{q})$. The initial state of neutral B meson evolves into superposition of these two flavor state via flavor changing weak interaction shown in Fig.3.

Both B^0 and $\overline{B}^0$ can decay to the same CP eigenstate f_{CP} through the mixing for example $J/\Psi K_S$ as shown in Fig.4. When B^0 (or $\overline{B}^0$) can decay into f_{CP} through

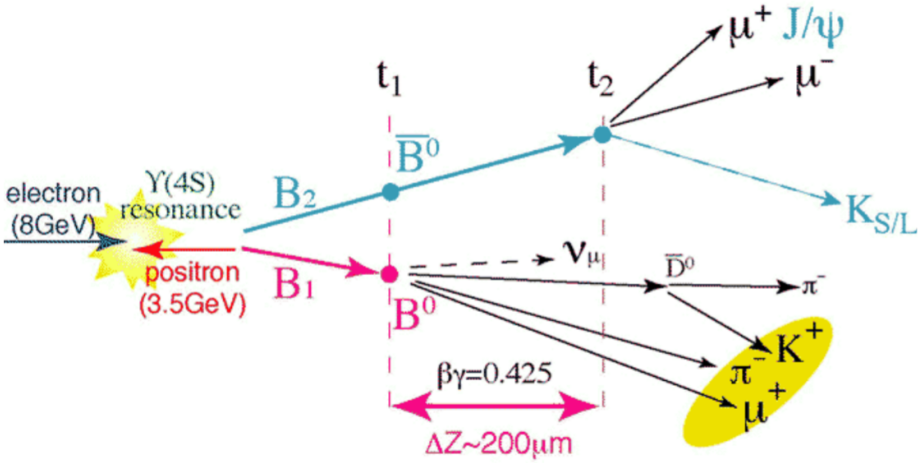


Fig. 5: The concept of asymmetric collision in Belle experiment [1]. The difference in the position of decay vertex between B^0 and $\overline{B}^0$ is enhanced by Lorentz boost.

different decay process, those decay processes interfere. The interference between two processes cause the difference in the decay width $\Gamma(B^0 \to f_{CP})$ and $\Gamma(\overline{B}^0 \to f_{CP})$.

We can define CP asymmetry of this CP violation by

$$A_{CP}(t) = \frac{\Gamma(B^0 \to f_{CP}) - \Gamma(\overline{B}^0 \to f_{CP})}{\Gamma(B^0 \to f_{CP}) + \Gamma(\overline{B}^0 \to f_{CP})} \tag{9}$$

and in the case of $B \to J/\Psi K_S$ this quantity is calculated as

$$A_{CP}(t) = -\xi_{CP} \sin(2\phi_1) \sin(\Delta m t), \tag{10}$$

where ξ_{CP} is an eigenvalue of final state f_{CP}. ξ_{CP} equals to -1 if $f_{CP} = J/\Psi K_S$, and 1 if if $f_{CP} = J/\Psi K_L$. We can determine one of the unitarity triangle angles ϕ_1 by measuring decay width of B^0 and $\overline{B}^0$.

The difference of lifetime between two neutral B mesons is 10^{-12}s. This lifetime difference is too small to be observed directly by detector. In Belle, the difference in the decay time is converted to the difference in the decay position by setting the energy of electron and positron asymmetric (Fig.5). The energy of electron and positron is set to 8 GeV/c and 3.5 GeV/c respectively. This leads to the energy of B meson pair having 4.5 GeV/c. The difference in the decay position of B^0 and $\overline{B}^0$ is expected to be $\Delta z \simeq 200$ us due to Lorentz boost $\beta\gamma = 0.425$. Owing to the asymmetric collision,

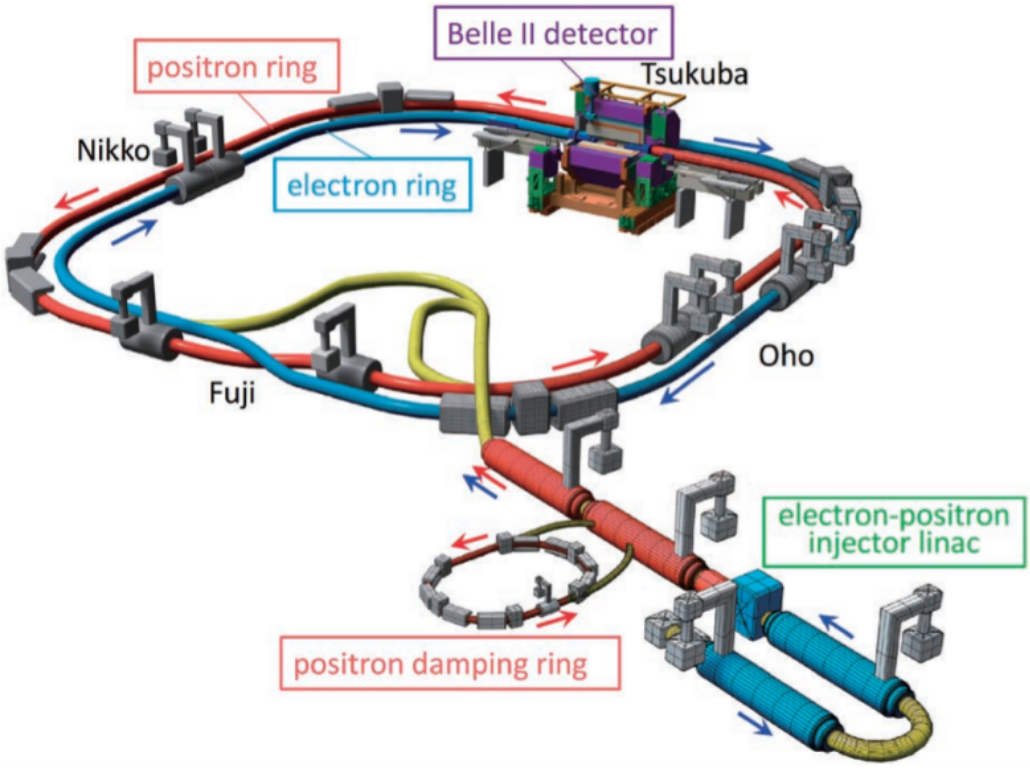


Fig. 6: Overview of SuperKEKB accelerator [1]

$\sin 2\phi_1 = -0.667 \pm 0.023(stat) \pm 0.012(syst)$ is obtained in Belle, and this is consistent with the expected value from SM $\sin 2\phi_1 = -0.667 \pm 0.020$ [2].

Belle experiment proved Kobayashi-Maskawa theory, while no significant hint larger than 3 sigma for new physics beyond standard model is obtained. In Belle II, the upgrade of both KEKB accelerator and Belle detector to SuperKEKB and Belle II detector is planned in order to obtain 50 times larger statistics than Belle experiment and reduce statistical errors.

1.3 SuperKEKB accelerator

The overview of SuperKEKB accelerator is shown in Fig.6. In SuperKEKB, the energy of electron and positron is changed to 7.0 GeV/c and 4.0 GeV/c respectively. SuperKEKB consists of a linear accelerator with 600m length and a ring accelerator with the circumstance of 3km.

		LER (e+)	HER (e-)	units
Beam Energy	E	4	7	GeV
Half Crossing Angle	ϕ	41.5		mrad
Horizontal Emittance	ε_x	3.2(2.7)	2.4(2.3)	nm
Emittance ratio	$\varepsilon_y/\varepsilon_x$	0.40	0.35	%
Beta Function at the IP	β_x^*/β_y^*	32 / 0.27	25 / 0.41	mm
Horizontal Beam Size	σ_x^*	10.2(10.1)	7.75(7.58)	μm
Vertical Beam Size	σ_y^*	59	59	nm
Betatron tune	ν_x/ν_y	45.530/45.570	58.529/52.570	
Momentum Compaction	α_c	2.74×10^{-4}	1.88×10^{-4}	
Energy Spread	σ_ε	$8.14(7.96) \times 10^{-4}$	$6.49(6.34) \times 10^{-4}$	
Beam Current	I	3.60	2.62	A
Number of Bunches/ring	n_b	2503		
Energy Loss/turn	U_0	2.15	2.50	MeV
Total Cavity Voltage	V_c	8.4	6.7	MV
Synchrotron Tune	ν_s	-0.0213	-0.0117	
Bunch Length	σ_z	6.0(4.9)	5.0(4.9)	mm
Beam-Beam Parameter	ξ_y	0.0900	0.0875	
Luminosity	L	8×10^{35}		$\mathrm{cm}^{-2}\mathrm{s}^{-1}$

Fig. 7: The table of machine parameters of SuperKEKB accelerator.

The electron and positron is accelerated to 7.0 GeV/c and 4.0 GeV/c in linear accelerator, and injected to electron storage ring called high energy ring (HER) and positron storage ring called low energy ring (LER). The electron and positron collide at one collision point on these rings. Belle II detector is positioned around the collision point. The center of mass energy is set to 10.58 GeV, which is the mass of $\Upsilon(4S)$.

The number of collision event per unit time R [event/sec] can be represented as

$$R = \mathcal{L}\sigma \tag{11}$$

where $\mathcal{L}$ and σ represents instantaneous luminosity $[m^{-2}s^{-1}]$ and interaction cross section $[\mathrm{cm}^{-2}]$ for target event respectively. In SuperKEKB accelerator, the luminosity is 40 times higher luminosity than that of KEKB accelerator.

The luminosity can be written as is in eq.12.

$$L = \frac{\gamma_\pm}{2er_e}\left(1 + \frac{\sigma_{y\mp}^*}{\sigma_{x\mp}^*}\right)\frac{I_\pm \xi_{y\pm}}{\beta_{y\pm}^*}, \tag{12}$$

where γ is lorentz factor, e is elemental charge, r_e is classical electron radius, I is

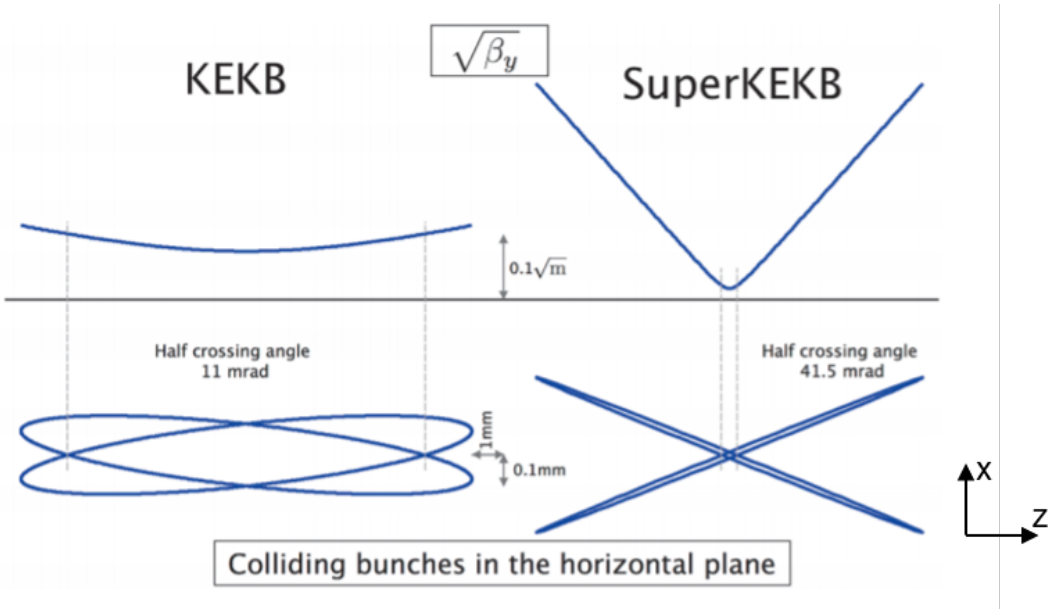


Fig. 8: The concept of nano beam scheme [8]. The left is the schematics in Belle, and the right is the nano beam scheme in Belle II. The angle between the bunch of electron and positron is enhanced in nano beam scheme.

beam current, $\sigma_{x,y}$ is beam size along each axis, and $\beta^*_{y\mp}$ is beta function along y axis. $\xi_{y\pm}$ represents beam-beam parameter, which means the effect of interaction between electron and positron beams. Each $+$ and $-$ represents positron and electron.

When we squeeze $\beta^*_{y\mp}$, hourglass effect and synchrobetatron resonance disturb the luminosity to be maximized. In order to avoid these difficulty, the new schematics called "nano beam scheme" is adopted. The concept of nano beam scheme is shown in Fig.8. In nano beam scheme, the large crossing angle of electron and positron bunches leads to the smaller $\beta^*_{y\mp}$ in the interaction region. Together with the enforcement of beam current, the luminosity in SuperKEKB is expected to become 40 times larger than KEKB.

1.4 Belle II detector

Belle II detector is constructed around the collision point in SuperKEKB. Belle II detector consists of 7 sub-detectors, and measures energy, momentun, charged particle trajectory, and decay vertex of the produced particles.

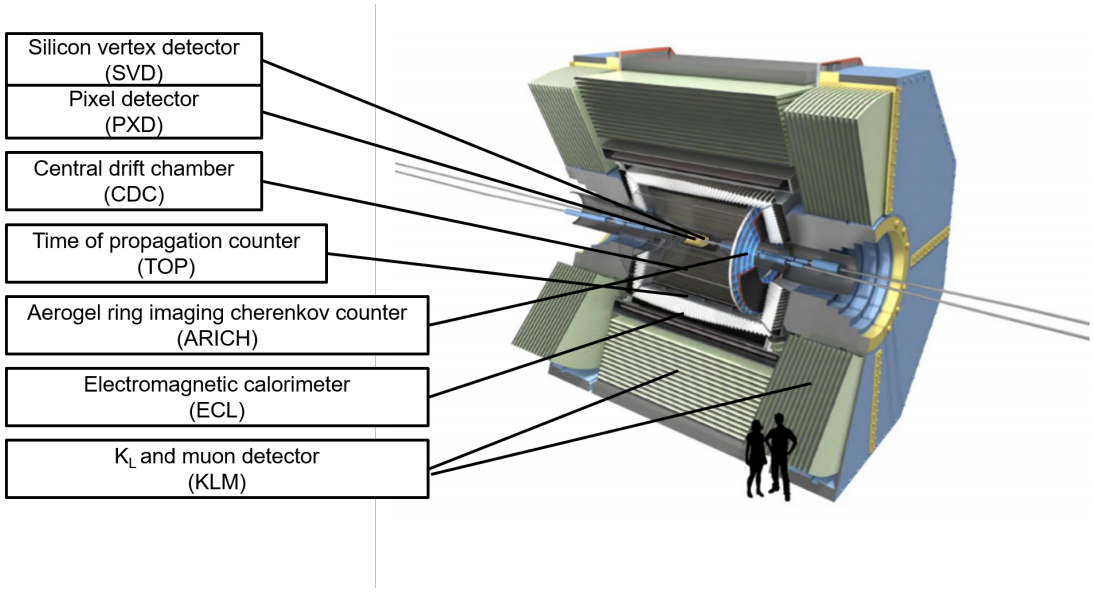


Fig. 9: Overview of Belle II detector

1.4.1 Aerogel ring imaging Cherenkov counter (ARICH)

ARICH is placed on the end cap part of Belle II detector. ARICH ovserves Cherenkov light from aerogel radiator. Particles are identified by measured Cherenkov angle. The comcept of ARICH is shown in Fig.10.

The aerogel radiator consists of multi layers with different refractive index. This corresponds to the focusing of photons within the aerogel radiator, and multi layers eliminate the uncertainty coming from the emission point of Cherenkov photon in the radiator. The Cherenkov ring is collected by the Hybrid Avalanche Photon Detector (HAPD), which is placed 20cm distant from aerogel radiator.

1.4.2 Central drift chamber (CDC)

CDC is a drift chamber placed outside SVD, and measures tracks of charged particles. CDC is filled with He (50%) and C_2H_6 (50%) gas. Axial and stereo wires are stretched along the beam direction. When the charged particle pass through CDC, electrons which is produced by the charged particle are collected to the anode wire. In addition to the reconstruction of particle track, CDC can provides particle identification using the energy loss in CDC gas volume.

The configuration of wire placement is upgraded in Belle II. In order to improve

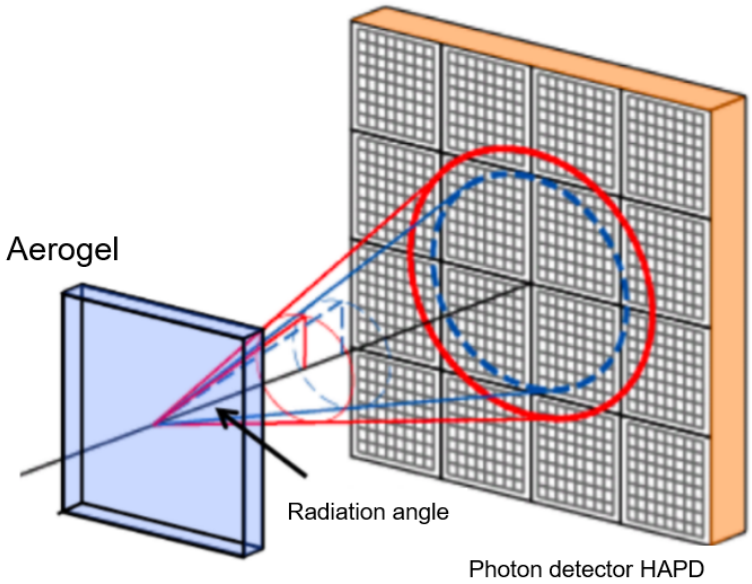


Fig. 10: Concept of ARICH. The radiation angle depends on the mass and velocity of the particle.

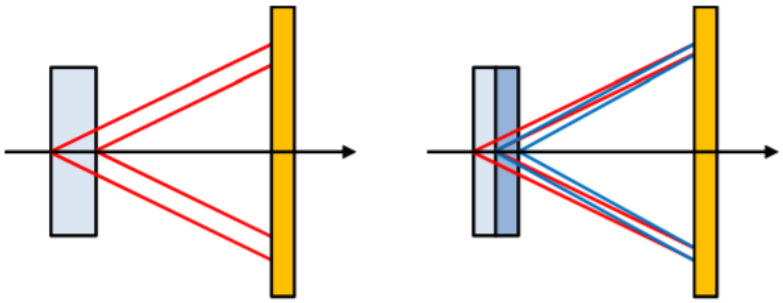


Fig. 11: The structure of aerogel. The left figure is for a single layer, and the right is for multiple layers of aerogel with different reflactive index. The dependence of radiation angle on the emission point of Cherenkov light is decreased in the multi layer radiator.

the position resolution and deal with the increased background and event rate, the density of wires in the inner layer is increased. The information measured by CDC is also used for trigger generation.

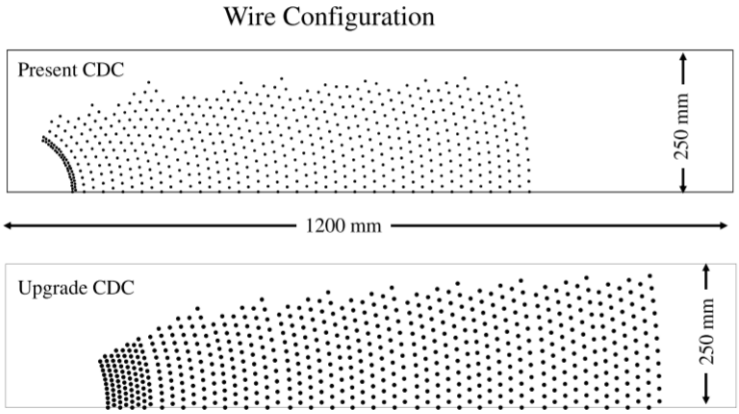


Fig. 12: CDC wire configuretion. The upper is for Belle, and the lower is for Belle II. The density of wires is increased in Belle II CDC.

1.4.3 Electromagnetic calorimeter (ECL)

Electromagnetic CaLorimeter (ECL) is a detector to measure the energy of photon and electron. ECL is placed in the both end cap region and barrel region. The energy and the number of clusters measured by ECL is also used for trigger generation.

In Belle II experiment, the photon energy range from 20 MeV to 4 GeV. In order to achieve high energy resolution, CsI(Tl) is used as the scintillation crystal because of high light output and short radiation length. Photon ,electron and positron losses their energy in the scintillator and forms electromagnetic shower, and the energy of particles are measured by the scintillation light. ECL is able to measure luminosity by detect Bhabha scattering. Combined with the momentun information measured in CDC, ECL can also distinguish electron and positron from other charged particle using its energy.

The structure of ECL unit is shown in Fig.13. The energy deposited in the crystal is collected by two pin photodiodes placed behind the crystal, and send to electronics. The overall structure of ECL is shown in Fig.14. The structure is not changed from Belle experiment, while the readout electronics is renewed in order to handle signal pileup due to high event rate and increased background.

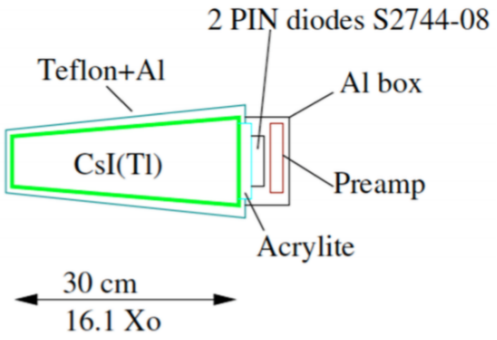


Fig. 13: The unit of ECL. 2 pin diodes are connected to CsI crystal.

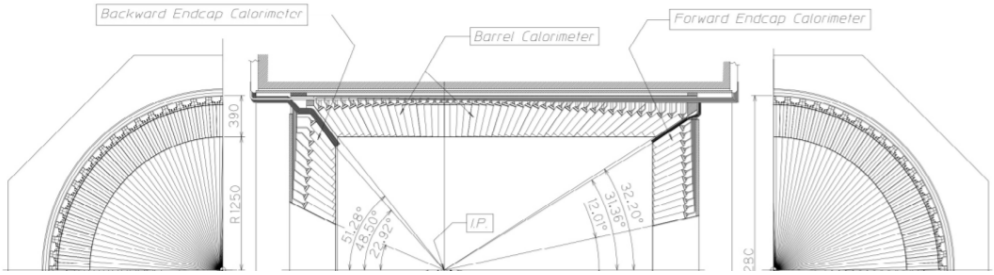


Fig. 14: ECL overall configuration

1.4.4 K_L and muon detector (KLM)

K_L^0 and μ detector (KLM) is a detector to identify K_L^0 and μ from other particles. KLM is placed outside ECL and divided into two regions : endcap region KLM (EKLM) and barrel region KLM (BKLM). KLM covers angle between $20° < \theta < 155°$ from the beam axis in total. The overall layout of KLM is shown in Fig.15.

KLM consists of the alternating sandwich of iron plates and detector layers. μ interacts with material via electromagnetig interaction, while charged hadron like π receives the effect from strong interaction. Using this property μ is identified by penetrating iron plates. K_L produces hadron shower in iron plate layer, and K_L is identified by observing particles from hadron shower.

In Belle experiment, glass-electrode resistive plate chambers (RPC) are used as detector layer. RPC has the property of large dead time about few seconds due to the long recovery time of the electric field in RPC after a discharge. In Belle

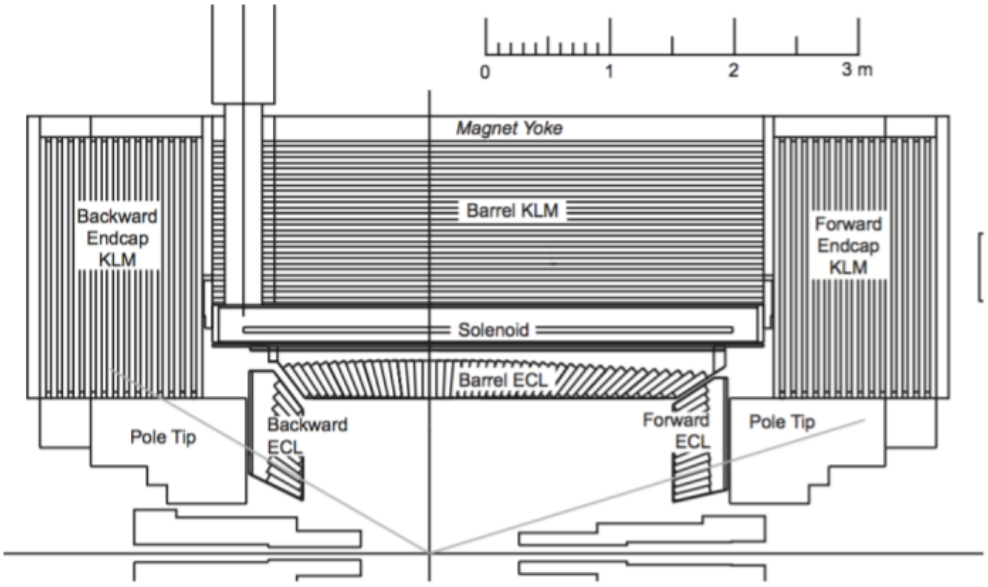


Fig. 15: KLM configuration in Belle II. KLM consists of Barrel KLM and End-cap KLM.

II experiment, large amount of neutrons produced in electromagnetic shower from background processes causes large dead time especially in the endcap region and the innermost layers of barrel region, and reduces particle detection efficienty. In order to avoid the problem from background neutron in these region, detector layer using scintillator strips and wavelength shifting fibers are newly developed and installed for the end cap region and two innermost layers of barrel region. This detector layer using scintillator strips has smaller dead time than Belle experiment and tolerance for increased background in Belle II experiment.

1.4.5 Time of propagation counter (TOP)

Time of propagation counter is placed in the barrel region outside CDC, and identify charged particles. TOP uses Cherenkov light to detect particle. Quartz bars are used as a radiator of Cherenkov light, and 16 $\times$ 2 micro channel plate PMT (MCP-PMT) is attached at the side of quartz bar as is shown in Fig.16.

The produced Cherenkov light is delivered to the end of scintillator, and detected by MCP-PMT. Because of the different angle of Cherenkov light between different types of particle, the time interval which takes Cherenkov light to reach MCP-PMT is

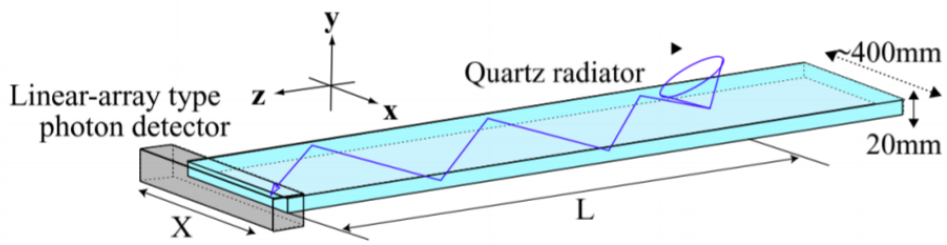


Fig. 16: The structure of TOP. Cherenkov lights are collected the photon detector at the side of scintillator.

different between particles. Thus we can identify types pf particles by measuring time-of flight (TOF). The difference in propagation time is about 200 ps, thus MCP-PMT is required to have time resolution less than 50 ps.

1.4.6 Pixel detector(PXD)

Pixel detector is the innermost sub-detector among 7 detectors covering angle of $17° < \theta 150°$ along the direction of beam. PXD is used to measure the tracks of charged particles and reconstruct decay vertex precisely combined with silicon vertex detector (SVD).

The pixel sensor is based on pixelated DEPleted p-channel Field Effect Transistor (DEFPET), and consist of two layers of sensors surrounding interaction point. The structure of DEFPET is shown in Fig.17. The electron-hole pair produced by charged particles entering the depletion layer is accumulated to the internal gate in Fig.17 and read out. Due to the large amount of channel it is impossible to read out all the channel at the same time. Thus data is read out for each line of DEFPET matrix by controlling gate voltage of FET. It takes 100 ns to read out and clear charge per line, and 20 μs to read out all the pixel channel. The full data size of PXD reaches 30GB/s under 30kHz trigger rate, therefore we cannot read out whole PXD data. Tracks of particles are reconstructed and extrapolated to PXD region. Then PXD data only in the region of interest is read out in order to reduce PXD data.

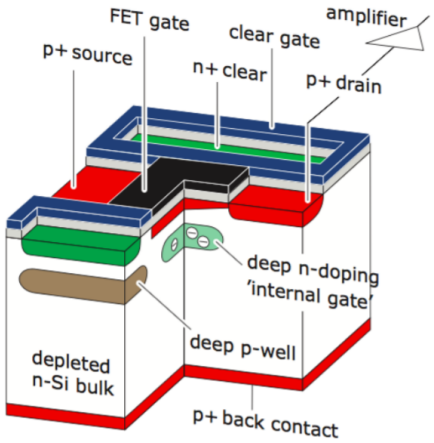


Fig. 17: The structure of DEFPET.

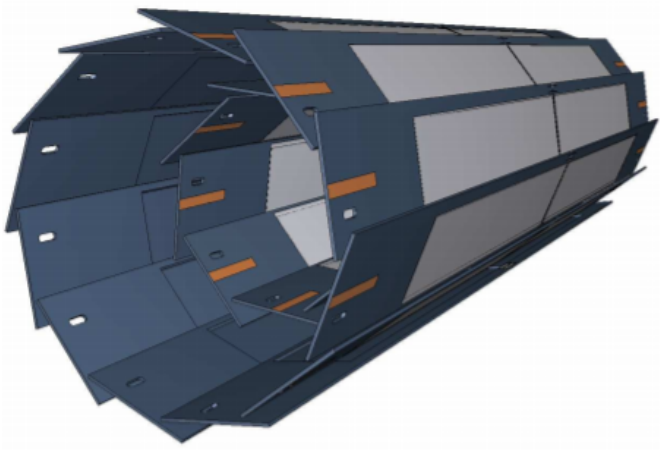


Fig. 18: The overview of PXD. PXD consists of two layers of sensors.

1.4.7 Silicon vertex detector(SVD)

Silicon vertex detector is placed outside PXD, and used to reconstruct tracks of charged particles. SVD consists of 4 layers of silicon detector called double sided Si-strip detector (DSSD) shown in Fig.19. Silicon strips are placed in both side of the sensor in such a way that the n-side strip is perpendicular to the beam direction. Charged particles create electron-hole pair in the n bulk, and the electron and hole is collected in n-side and p-side respectively and read out.

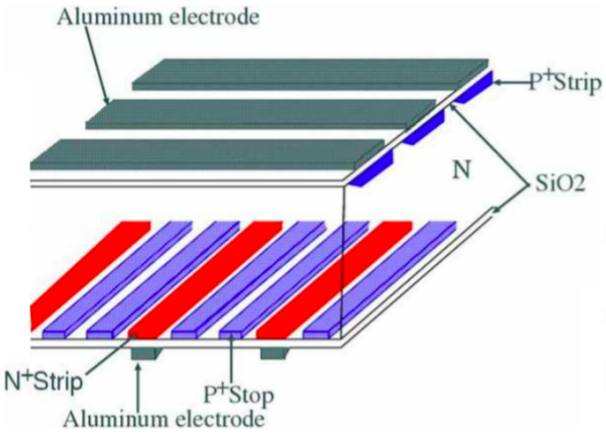


Fig. 19: The structure of DSSD. Silicon strips are put on both sides of N bulk orthogonally.

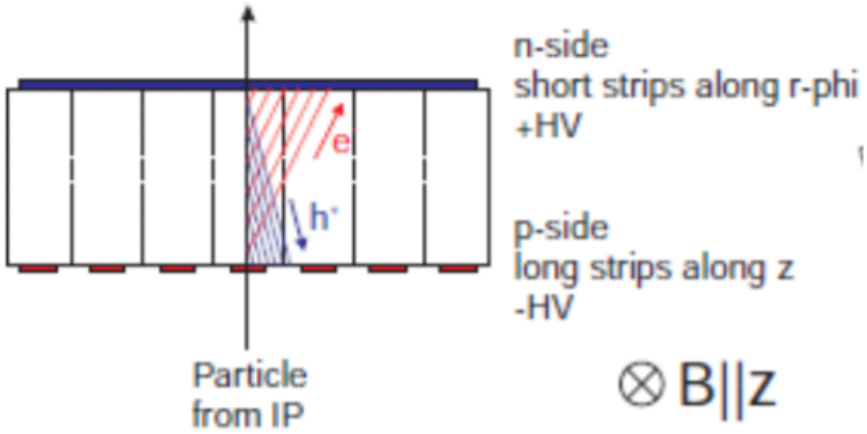


Fig. 20: The detection mechanism of DSSD. The produced electron and hole are collected to silicon strips and read out by electrodes.

SVD uses ASIC called APV25 to read data from strips in order to achieve fast read out. In Belle II experiment, we expect 30kHz trigger rate under target luminosity $\mathcal{L} = 8 \times 10^{35}$. Due to the limited buffer size of APV25, SVD is expected to produce 3.4% dead time under 30kHz.

Table 1: Table of expected trigger rate for each process under SuperKEKB target luminosity [14]. Due to the 30kHz upper limit of trigger rate, the trigger rate from beam background signals must be below 15kHz.

Process	σ (nb)	Rate (Hz)
$\Upsilon(4S)$	1.2	960
Continuum	2.8	2200
$\mu^+\mu_-$	0.8	640
$\tau^+\tau_-$	0.8	640
Bhabha	44	350
$\gamma\gamma$	2.4	19
Two photon	12	10000
Total	67	15000

1.4.8 Trigger system (TRG)

Trigger system (TRG) is a system which is responsible for issuing trigger. In Belle II experiment, we need to take data under high trigger rate up to 30kHz due to high luminosity in SuperKEKB. Thus trigger system is required to achieve high efficiency for physics event trigger and at the same time suppress event from beam background event as small as possible. The expected cross section and trigger rate for dominant process under target luminosity $\mathcal{L} = 8 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ is shown in the Table.1. The requirements for trigger system are as listed below.

- Maximum trigger rate of 30kHz
- 100% trigger efficiency for $\Upsilon(4S)$ decay event
- Trigger distribution latency under 5μs
- The timing resolution is under 10ns

The overview of trigger system is shown in Fig.21. There exist 4 sub triggers : from CDC,ECL,TOP, and KLM. Each sub trigger system works independently, and the information from those four detectors are sent to global decision logic (GDL) and final decision for trigger signal is done by GDL. The trigger decision for physics event is mainly done using sub triggers from CDC and ECL. TOP sub trigger is used mainly

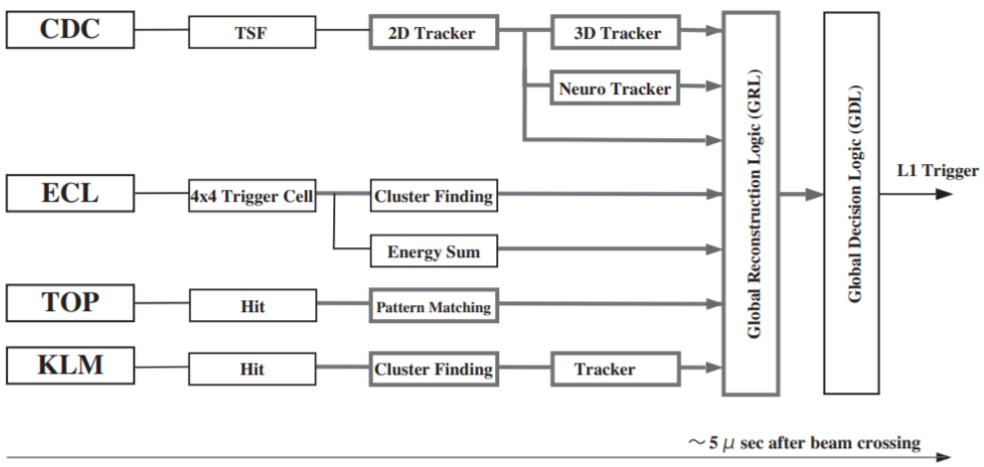


Fig. 21: The overview of trigger system [7]. Level 1 trigger is generated using information from four sub-trigger systems.

for the trigger with better timing resolution, and the muon identification from KLM sub trigger is used in combination with CDC and ECL sub trigger.

1.4.9 Data acquisition system (DAQ)

Data acquisition system (DAQ) is a system responsible for reading out and processing data from all sub-detectors. The data rate from all detectors is expected to become as large as 30GB/s, and DAQ need to process the large amount of data in real time and store it. The detail of DAQ is explained int the next section.

2 Data acquisition system

In Belle II, the instantaneous luminosity of SuperKEKB accelerator is 40 time higher than that of KEKB accelerator in Belle. Owing to the upgrade of detectors in Belle II detectors, the data size per event is expected to be greater than 1MB/s in total under the target luminosity $\mathcal{L} = 8 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The maximum trigger rate is expected to be 30kHz, therefore We need to handle 30GB/s data flow in the on line data processing. The overall structure of the Belle II data acquisition system is shown in Fig.22. The clock signal is common among all the modules in data acquisition system, and made by the 508MHz radio frequency of SuperKEKB. The 508MHz clock is divided by four, and the generated 127MHz clock is used as a common clock. The trigger signal is delivered from GDL.The trigger signal and the clock signal is then delivered to all the front-end electronics, which is placed near the Belle II detector. The obtained data is digitized on these front-end electronics and send to a module named Common Pipelined Platform for Electronics Readout (COPPER). Front-end electronics and COPPERs are connected by optical fiber, and data from sub-detectors are sent using original communication protocol named Belle2link. COPPER receives data from front-end electronics, and sends data to readout PC after data formatting. Each readout PC carries out a partial event reconstruction using data collected to the one readout PC, and send data to high level trigger (HLT). HLT is responsible for carrying out full event reconstruction and select events to be recorded. Combined with PXD data the final event reconstruction is done, and event data is stored to the storage system.

2.1 Trigger timing distribution system (TTD)

Trigger timing distribution system (TTD) is a system responsible for distributing system wide clock and trigger signal for whole Belle II detector. The clock signal and trigger signal is distributed to more than a thousand of front-end electronics. The detailed structure of TTD is explained in section 3.

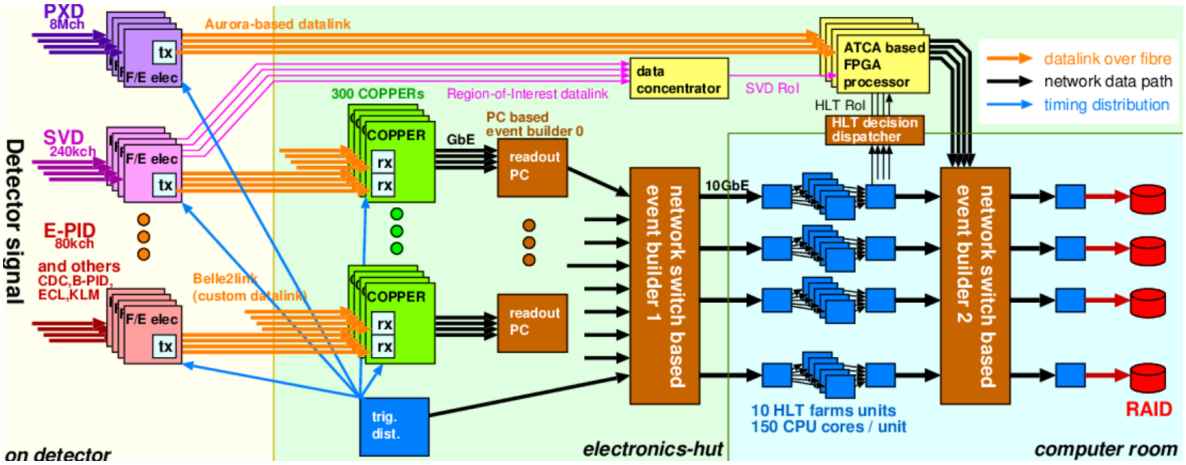


Fig. 22: The overview of data acquisition system [6]

2.2 Common Pipelined Platform for Electronics Readout (COPPER)

COPPER is a module to receive signals from detectors, process signal data, and send data to readout PC. COPPER is first developed in Belle in need for larger data throughput. COPPER has been upgraded to COPPER II and COPPER III. The original motivations for the developing of COPPER are as follows.

- Flexibility to fit various experiments
- Wide acceptance of trigger rate up to 30kHz
- Under 1% dead time using pipelined read out system
- Easy handling for writing readout software

2.2.1 Concept and motivation for COPPER

The schematics of the first version of COPPER is shown in Fig.23.

In the first version of COPPER, COPPER receives analog signal from detector electronics, and the analog signal is sent to a daughter mezzanine module called Front-end INstrumentation Entity for Subdetector Specific Electronics (FINESSE). FINESSE is responsible to convert analog signal from detector to up to 32bit digital signal using time to digital converter (TDC) or analog to digital converter (ADC), and store it to event first-in-first-out buffer (FIFO) on the COPPER board. The implementation of FINESSE is defined by each sub-detector. Data in the event FIFO

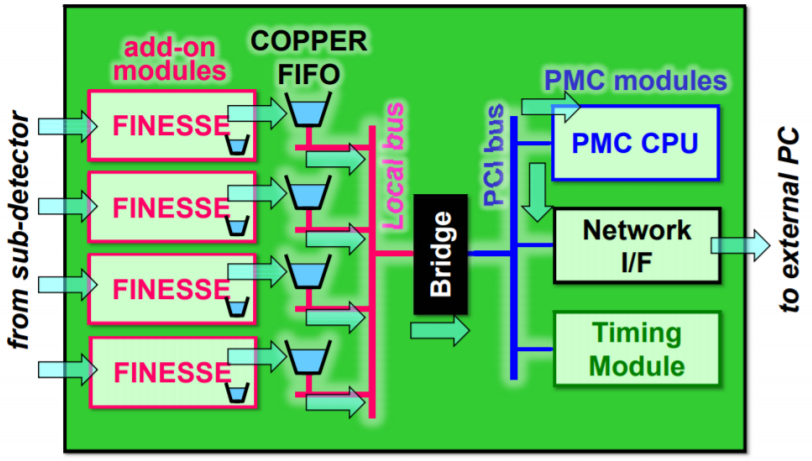


Fig. 23: The block diagram of COPPER version 1. Event data from detector is received by FINESSE, and digitized using ADC or TDC.

is then read by processor PMC module (PrPMC) via direct memory access, and data formatting and data size suppression is carried out. Data processed by PrPMC is finally sent to readout PC using ethernet port.

2.2.2 Upgrade of COPPER to version 2 and 3

In the first COPPER, the content of FINESSE depends on each sub-detector. In order to unify the treatment of data readout, the concept of Belle2link and remote FINESSE is introduced as is shown in Fig.24.

In this scheme, analog signals from sub-detectors are digitized in each front-end electronics on detector. The digitized signal is sent to COPPER version 2 and 3 via optical fiber. FINESSE on the COPPER is replaced by a receiver card called High Speed Link Board (HSLB). The data link protocol between front end electronics and COPPER via optical fibers is called Belle2link.

The Belle2link protocol has the function to send measured data from front end electronics to COPPER, and at the same time receives various parameter settings from COPPER. The communication is done by 2.54 Gbps serial link. An original communication protocol for Belle2link is developed.

Belle2link data transmitter on front end electronics adds trigger timing and CRC checksum information to the digitized data. HSLB stores data from front end elec-

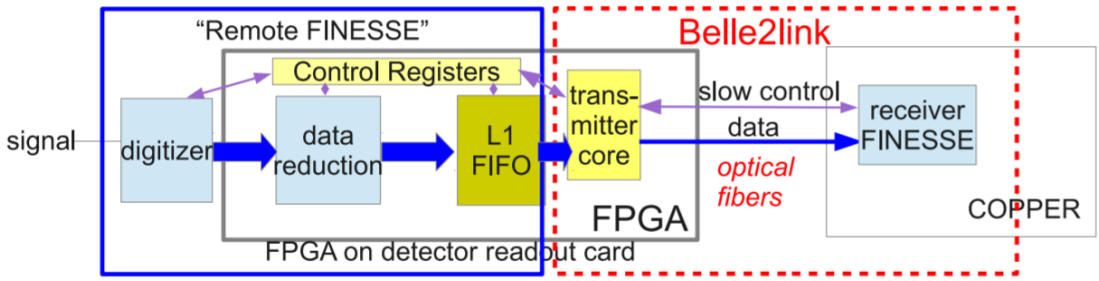


Fig. 24: The schematics of Belle2link [6]. The function of ADC or TDC on the COPPER FINESSE is moved to the front-end electronics on sub-detector readout cards. HSLB cards, which receive digitized data from front-end electronics is newly implement on COPPER version 2.

tronics on the event buffer in COPPER after checking CRC checksum and adding header.

Event data stored in the event buffer is read by on-board processor PrPMC via direct memory access, and sent to readout PC after being added header and footer by PrPMC. PrPMC uses Intel Atom CPU 1.6GHz and 512MB memory, and is booted by readout PC using network boot.

2.3 Event building

The process of event building consists of three steps : Event builder 0 (EB0), Event builder 1 (B1), and Event builder 2 (EB2). EB2 is explained in section 2.4 since EB2 is deeply related to HLT.

2.3.1 Event Builder 0

EB0 is done in readout PC. Each readout PC receives data via 1GBit ethernet cable from up to 16 COPPER via a network switch. These data fragment are combined to one data and sent to the upstream network switch.

2.3.2 Event Builder 1

In event builder 1 (EB1), all the event fragment from readout PCs are combined together, and sent to High Level Trigger (HLT). EB1 consists of 6 network switches as is shown in Fig.26.

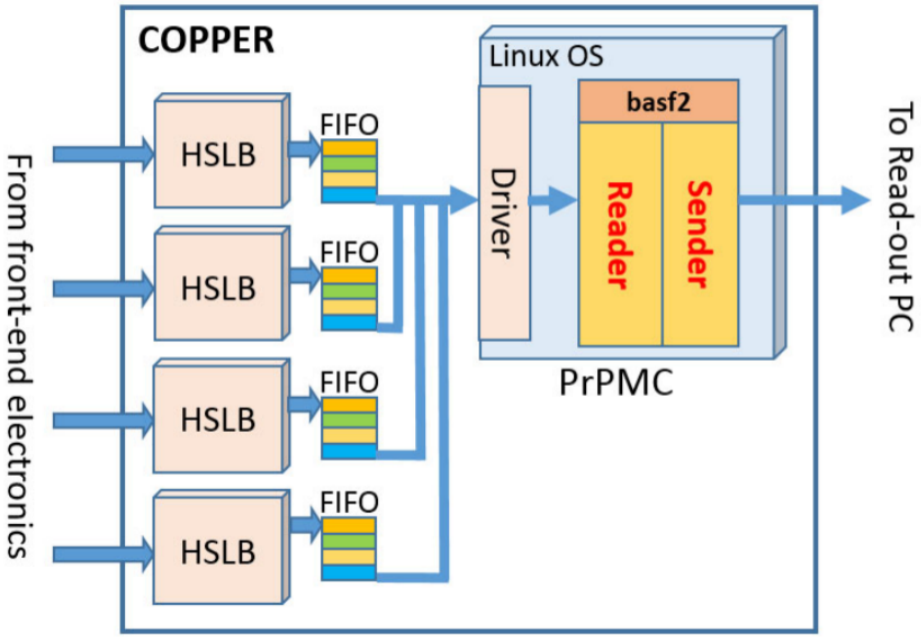


Fig. 25: The data flow in COPPER version 2 and 3. The digitized data from sub-detectors are received by HSLB cards and stored to FIFO event buffer. Data in event buffer is read by CPU via PCI bus.

Data is first sent to 4 network switches (ARISTA 7050T) and then sent to 2 network switches (ARISTA 7150). These two types of network switches are connected by 10Gbit ethernet cable in full-mesh connection.

2.4 High level trigger

High level trigger (HLT) is a system to reconstruct events and generate software triggers. By selecting only necessary events using software triggers, we can reduce the data size to be recorded to storage system. Measured data except for PXD is sent to HLT from EB1 network switch via 10Gbit connection. One HLT node consists of a multi-core PC. Event data is stored in a large ring buffer and processed by each CPU in parallel.

High level trigger (HLT) is a system to process and reconstruct each event in the exact same way as offline analysis. Measured data except for PXD is sent to HLT from EB1 network switch via 10Gbit connection. One HLT node consists of a multi-

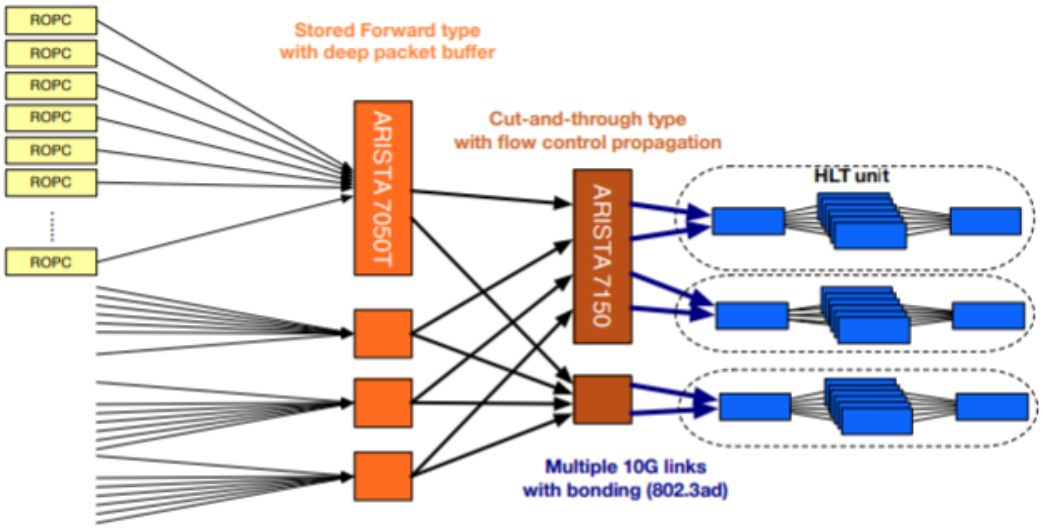


Fig. 26: The structure and connection of event builder 1. The data for readout PCs are first connected to 4 ARISTA 7050T network switches. Those 4 network switches are connected to 2 ARISTA 7150 network switches. Finally data is sent to HLT units.

core PC. Event data is stored in a large ring buffer and processed by each CPU in parallel.

Particle tracks which is reconstructed in HLT are used for selecting which PXD region to be read. Particle tracks is extrapolated to PXD and the region of interest (ROI) is defined. The information of ROI is sent to PXD readout system. Only PXD data in ROI is sent to EB2. EB2 receives data from HLT and PXD readout system, and event reconstruction using whole Belle II detector is done. Collected data is finally sent to storage system.

2.5 Slow control system

Slow control system is a system to control power supply for detectors, the configuration of components of data acquisition system, and run condition. As a method for slow control, two types of systems are used : Experimental Physics and Industrial Control System (EPICS)[5] and Network Shared Memory 2 (NSM2) [11].

EPICS is a software tool to develop and implement distributed control system, which is widely used in large scale high energy physics experiments and accelerator

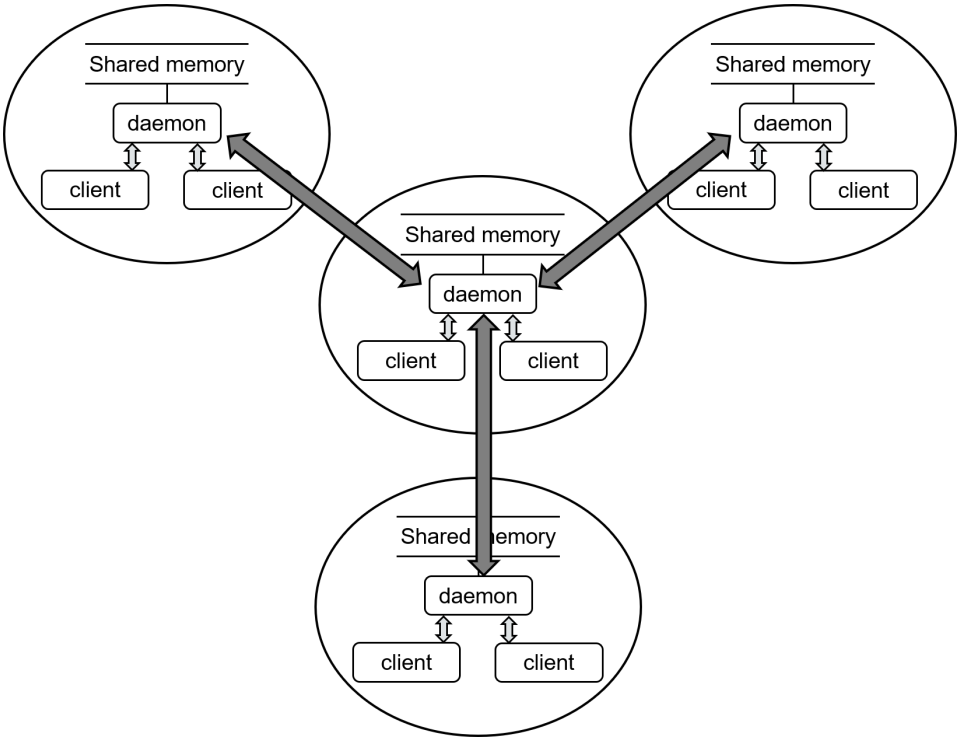


Fig. 27: The structure of NSM2 processes. In each CPU, the daemon process manages the shared memory on each CPU and communicates with other daemon processes on other hosts on the network. The client process can send and accept command via the daemon process.

projects. EPICS is developed originally by Argonne National Laboratory.

Network Shared Memory (NSM) is a tool to share information between different CPUs [11] . NSM is originally developed in Belle experiment, NSM2 is the upgrade of NSM for Belle II experiment. NSM2 has the function to share information and send commands between different processors. NSM2 consists of two types of processes, which are "daemon" and "client" as in Fig.27.

One daemon exists per one CPU. The daemon process is responsible for managing connection between daemons on the other CPUs on a network and accept connection from clients on the same CPU. The daemon process also manage the shared memory on the CPU. In one CPU, multiple client processes can exist. These client processes communicate with the daemon process. The client process can send and accept command via the daemon process.

3 Monitoring system of Trigger Timing Distribution System

Before Belle II phase 2 operation in 2018, there exists no monitoring or logging system for Trigger Timing Distribution system (TTD). If we don't record information about the performance of TTD, it is difficult to distinguish what is the cause of trouble when Belle II operation stops due to some problem. Thus monitoring system of TTD is important for future Belle II operation. In this section we first overview the component of TTD. Next, the structure of the monitoring system for TTD is explained. This TTD monitoring system is operated during Belle II phase 3 operation in 2019 spring, and the performance of monitoring system is evaluated by using data taken in phase 3 run.

3.1 Overview of TTD

TTD is a component of Belle II detector which is responsible to distribute trigger and clock information to all the detectors. SVD requires triggers to be distributed to the front end electronics within 5 μs from collision event of electron and positron, and this is the most strict constraint among all the front end electronics of detectors. The deadtime of SVD is expected to be 3% at 30kHz of trigger rate because of the limited buffer size in the current SVD data readout system. The improvement of SVD readout system is under study. After the upgrade of SVD readout system it is expected that the amount of triggers rejected can be reduced from 3% to 1.5%[reference]. It is desirable that TTD can distribute trigger below 1% dead time.

As a summary, requirement on TTD are

- Trigger distribution to whole Belle II electronics within 5 us from a collision event.
- Trigger distribution to whole Belle II detector within 1% dead time under 30kHz trigger rate.

3.1.1 Front-end trigger-timing swtch

TTD consists of 140 modules named Frontend Timing SWitch (FTSW) shown in Fig.29. FTSWs are connected in a tree structure shown in Fig.30. The root of

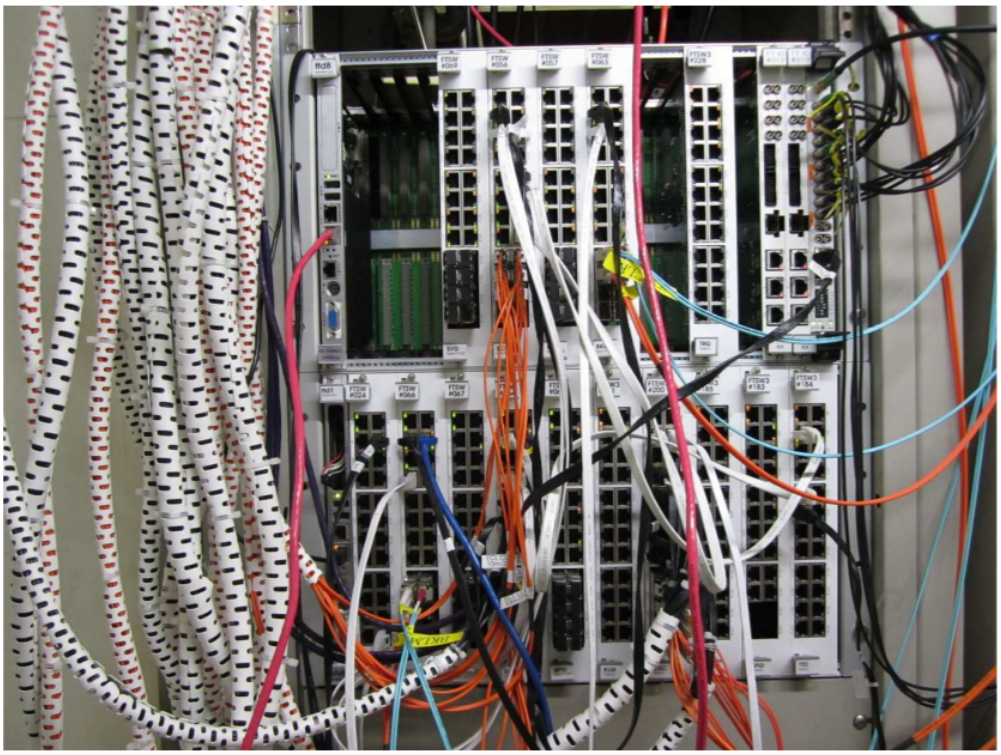


Fig. 28: The picture of the VME crate for TTD. FTSWs and a VME CPU board is placed in one VME crate.

this FTSW tree is called master FTSW as shown in Fig.30. Each square in Fig.30 represents a FTSW and a COPPER.

Trigger information is first created by Global Decision Logic (GDL) using signal from CDC, ECL, KLM, and TOP. The trigger information from GDL is then injected to master FTSW, and distributed to all Front-End Electronics (FEE) on sub-detectors. Trigger information can be delivered to all the electronics within three intermediating FTSW from master FTSW.

Master FTSW is driven by a clock of 127MHz, which is commom for all the DAQ related electronics. Distributing clock signal is one of the important function of FTSW. FTSW uses Xilinx Virtex-5 FPGA, and has 24 RJ-45 ports including one input from upper stream FTSW and twenty output to down stream FTSW.

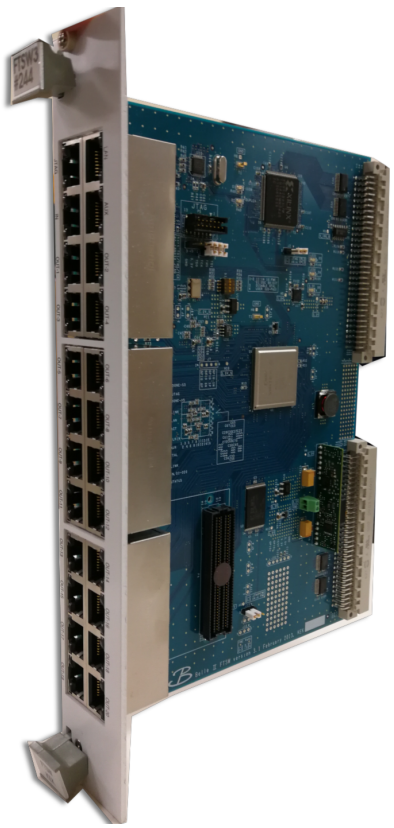


Fig. 29: The picture of the FTSW board

3.1.2 Communication protocol

The communication between FTSWs is done by a 254MHz serial link through a CAT7 cable or a pair of optical fibers. The trigger information is embedded into an 8b10b encoded data package and distributed from master FTSW to down stream FTSWs. The serialization of trigger information is done directly inside the FPGA, which enables a timimg distribution with low latency.

As a communication protocol for the communication between FTSWs, original protocol developed by Belle II DAQ group is used. The structure of trigger distribution protocol is as shown below.

The structure of the protocol is shown in Fig.31. The electron and the positron takes 10 us to go one round in SuperKEKB accelerator ring, and this corresponds to 1280 clock under 127MHz clock. We can send 2560 bit information using double-data-rate transfer. The structure of distributed stream is periodical under 2560 bit

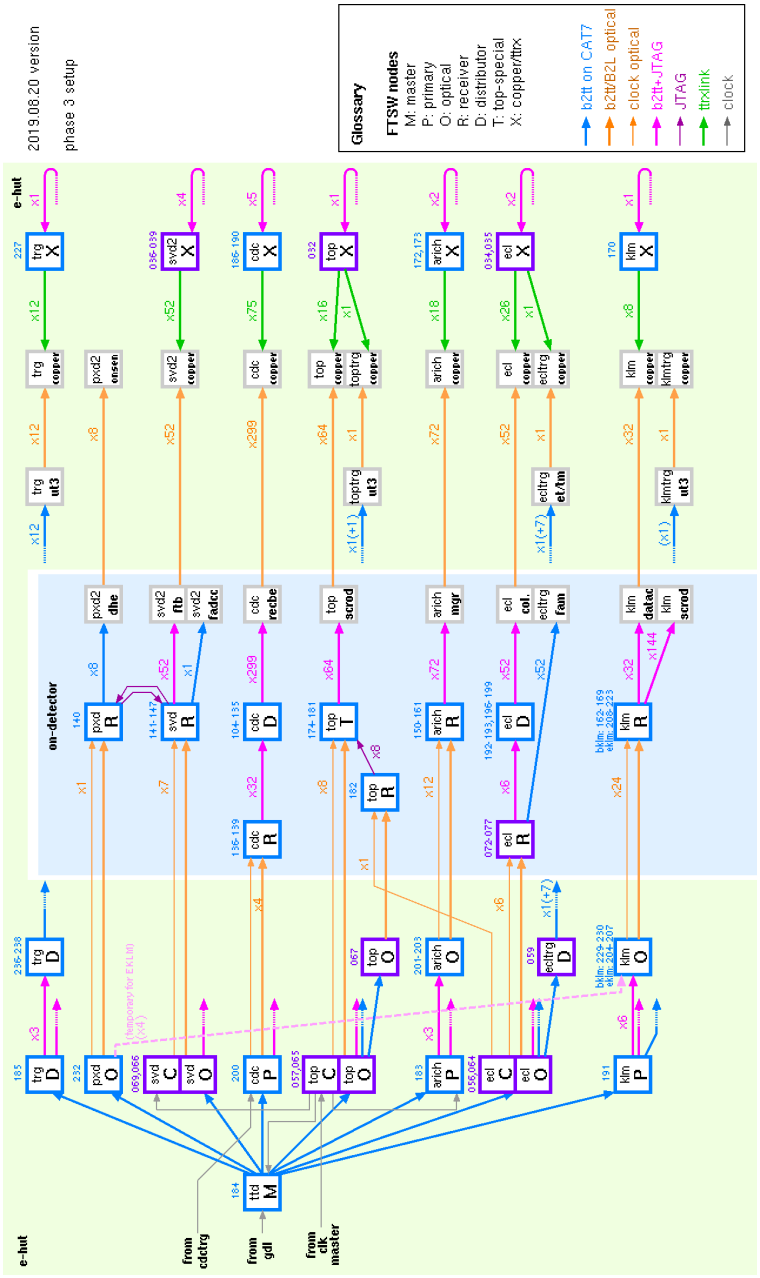


Fig. 30: Tree structure of FTSW [6]. In this figure, blue squares represents FTSW. Gray squares represents front-end electronics and COPPER boards.

data, and here we define 2560 bit stream as a frame.

One data frame consist of 16 data packet, and one data packet consists of 16 octet (=10bit). When trigger information needs to be distributed, trigger information octet can be inserted to an arbitrary octet in one data packet. The octets behind the trigger

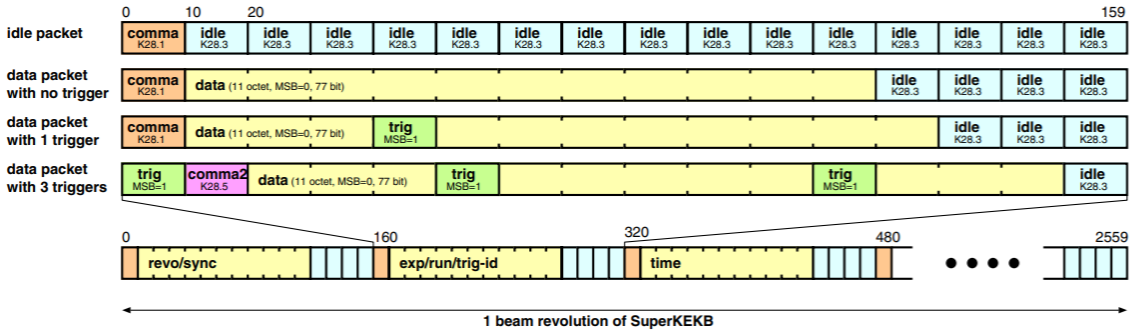


Fig. 31: Structure of Trigger timing distribution packet [12]. One data frame corresponds to 2560 bit, 10 μs. One data frame consists of 16 data packet. One data packet consists of 16 octets. Up to 3 trigger information can be inserted to one data packet.

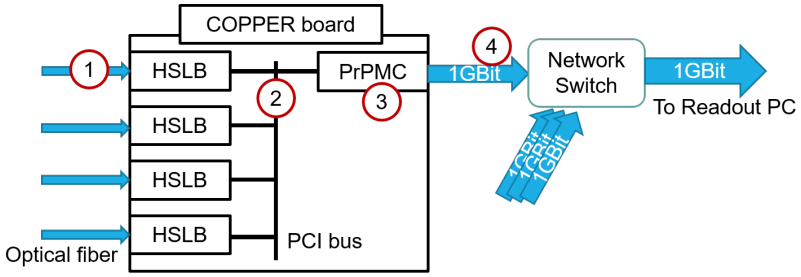


Fig. 32: Four kinds of bottleneck around COPPER. The data transfer rate using PCI bus, the data output line using 1GBit ethernet cable, and the data processing rate in CPU are the dominant bottlenecks around COPPER board.

information octet in the same packet is shifted by one octet to the later octet, and one idle octet is removed. At most three trigger information can be inserted to one data packet, and we avoid more than 4 triggers per one data packet by ensuring 190ns minimum interval between triggers.

3.2 Data flow bottleneck

In the data flow in data acquisition system, there exists potential bottlenecks in various places of data flow. If data throughput rate exceeds the limit by bottlenecks, dead time is expected to arise due to the back pressure. In this subsection, we explain

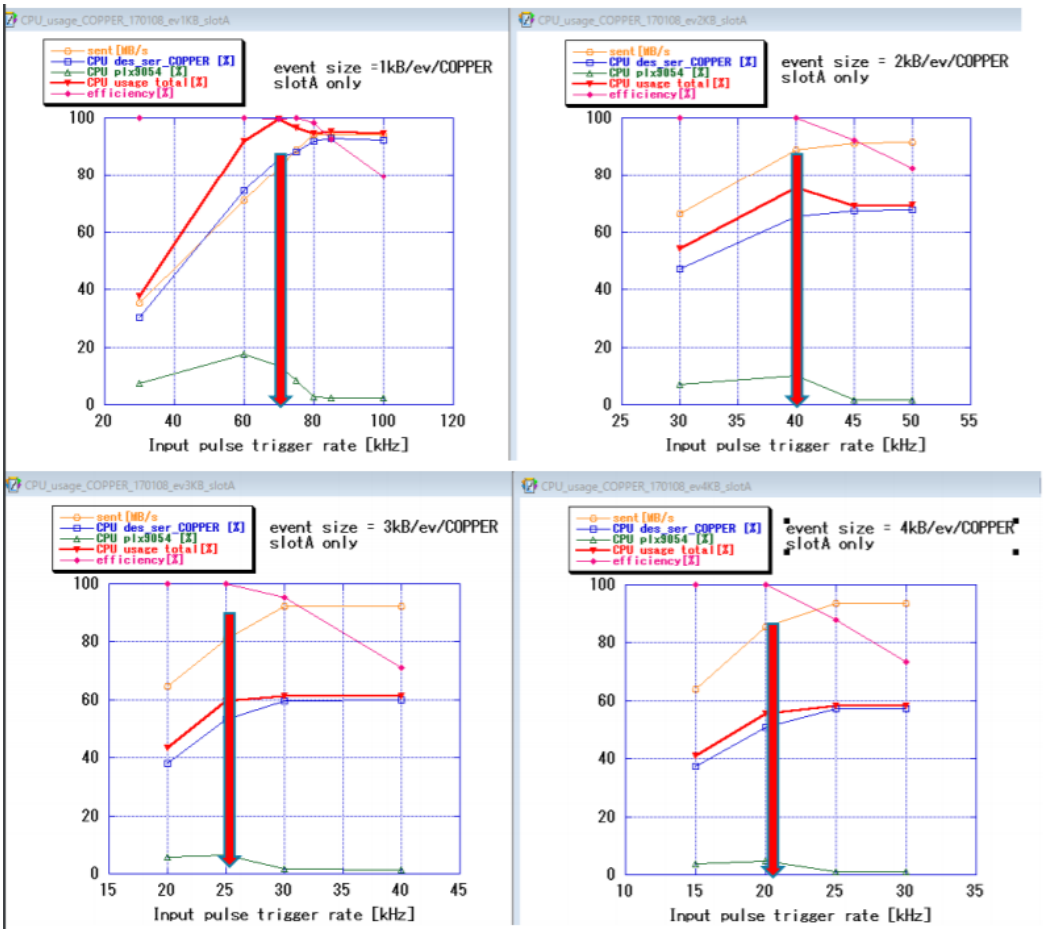


Fig. 33: The figure of the relation between data size, trigger rate and CPU usage of COPPER [15]. The red line represents the total CPU usage. The pink line represents the efficiency defined as input data rate/output data rate. The red arrow represents the trigger rate where the efficiency begins to drop from 100%

potential bottlenecks of data flow in data acquisition system.

3.2.1 The bottleneck in COPPER

There exist mainly four kinds of potential bottlenecks around COPPER board as shown in Fig.32.

The bottleneck 1 is the data input to the HSLB. The speed of Belle2link between front-end electronics and HSLB is 2.54Gbps.

The bottleneck 2 is the data transfer speed of PCI bus between HSLB and PrPMC. The data transfer rate of PCI bus is 133MB/s.

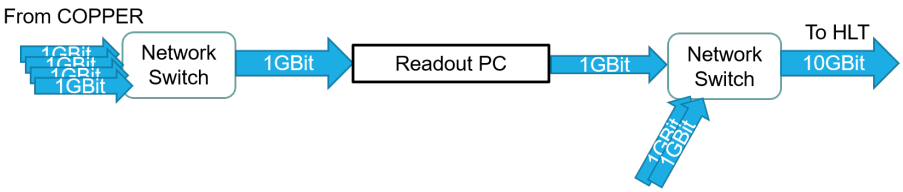


Fig. 34: The bottleneck around Readout PC. The input and output line of readout PC are 1GBit ethernet cable, and these are the bottlenecks.

The bottleneck 3 is the processing speed in PrPMC. The relation between the event size per event, trigger rate and CPU usage of COPPER is shown in Fig.33. The red line and pink line represents CPU usage and data throughput efficiency. We begin to lose input data above 80MB/s data throughput.

The bottleneck 4 is the data output from PrPMC to network switch. In this part 1GBit ethernet cable is used, thus the limit of data rate is under 125MB/s.

As a summary of the potential bottlenecks around COPPER, data throughput for these four types of bottlenecks is $1 >> 2 \simeq 4 \geqq 3$, thererfore the bottleneck 3 is dominant among bottlenecks around COPPER board.

3.2.2 The bottleneck in Readout PC

The readout PC receives event data from multiple COPPER board via network switch. 10GBit ethernet cable is used for data input, thus bottleneck for data input is 1.25GB/s. On the other hand, 1GBit ethernet cable is used for data output from readout PC. Thus 125MB/s event data per one readout PC is the maximum data throughput under the current readout system.

3.3 Collection of busy signal

The up stream FTSW and the down stream FTSW are connected using one 1GBit ethernet cable. We can transfer 4 signals by one ethernet cable. Among 4 signals, two signals, clock and trigger information respectively, are send from upper stream FTSW to down stream FTSW. At the same time, one signal, which is called busy signal, is collected from down stream FTSW to upper stream FTSW 35. Busy collection protocol is in Fig.36.

As shown in the trigger timing distribution protocol, one data packet consists of

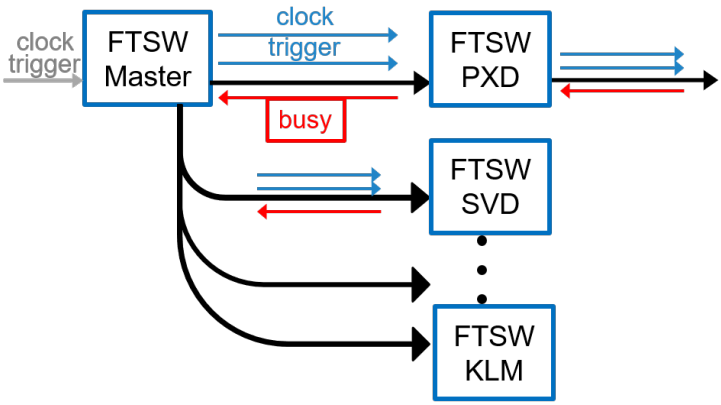


Fig. 35: Overview of signal flow. The clock and trigger signal is sent from up to down stream FTSW. At the same time, the busy signal is collected from down to up stream FTSW.

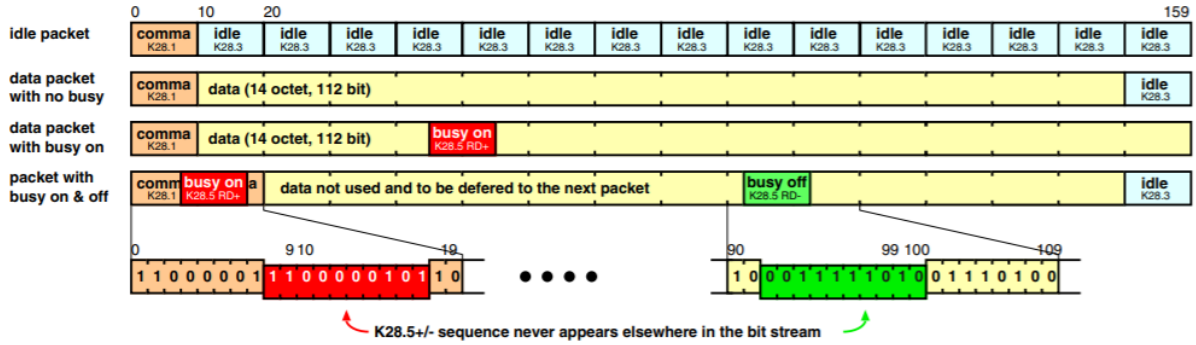


Fig. 36: The structure of busy protocol. When the busy signal is issued by downstream electronics, the octet indicating busy state is inserted to the data packet which is sent to upstream FTSW. The busy octet can be inserted to any 10 bit in the data packet.

16 octet. When FTSW connected to Front end electronics or COPPER receives busy signal from them, octet indicating beginning of busy state can be inserted instantly to arbitrary position in busy collection protocol. An octet indicating end of busy state is inserted if busy signal from down stream electronics disappears.

In each FTSW, busy signal sent from each down stream FTSW is decoded and merged into one busy signal by taking OR of the all busy signals from downstream FTSW. The busy signal is then sent to upper stream FTSW. All the busy signals are

collected to the master FTSW. This busy collection schematics makes 70ns latency per one protocol decode/encode step.

When master FTSW receives busy signal from any FTSW, master FTSW stops trigger distribution, and wait until busy signal disappears. Thus TTD cannot distribute trigger if any one busy signal is detected, and this corresponds to "dead time" in data acquisition system. By supervising the amount of busy signal collected in master FTSW, dead time can be evaluated.

Source of busy signal can be classified to two types : from COPPER, and from Front-End Electronics.

3.3.1 From COPPER

The overview of the busy signal from COPPER is shown in Fig.37. COPPER board receives digitized signal from front-end electronics on each sub-detectors by a board named HSLB. The data received by HSLB is then sent to FIFO and read by CPU. Each of four HSLB has its own FIFO and each FIFO sends busy signal to FTSW respectively when FIFO is about to become full.

Belle II data acquisition system adopts a pipeline readout system as shown in Fig.38. The pipeline readout system consists of chained readout modules. Each module sends data to the downstream module, and at the same time receives data from the upstream module. In the pipeline readout scheme, we don't need to wait starting the processing of next event until the previous event is completely read out. This is the advantage of pipeline readout against event by event readout.

In Belle II experiment, pipeline readout system provides the advantage of shorter dead time and larger data throughput in data acquisition system. On the other hand, pipeline readout system has the feature that single stagnation of data flow in whole data acquisition causes Belle II detector unable to take data. In such a case where there exists data flow stagnation, back pressure from upper stream data readout system can cause buffer of COPPER full.

The busy signal from COPPER not only means any error in COPPER itself but also other back pressure from data acquisition system.

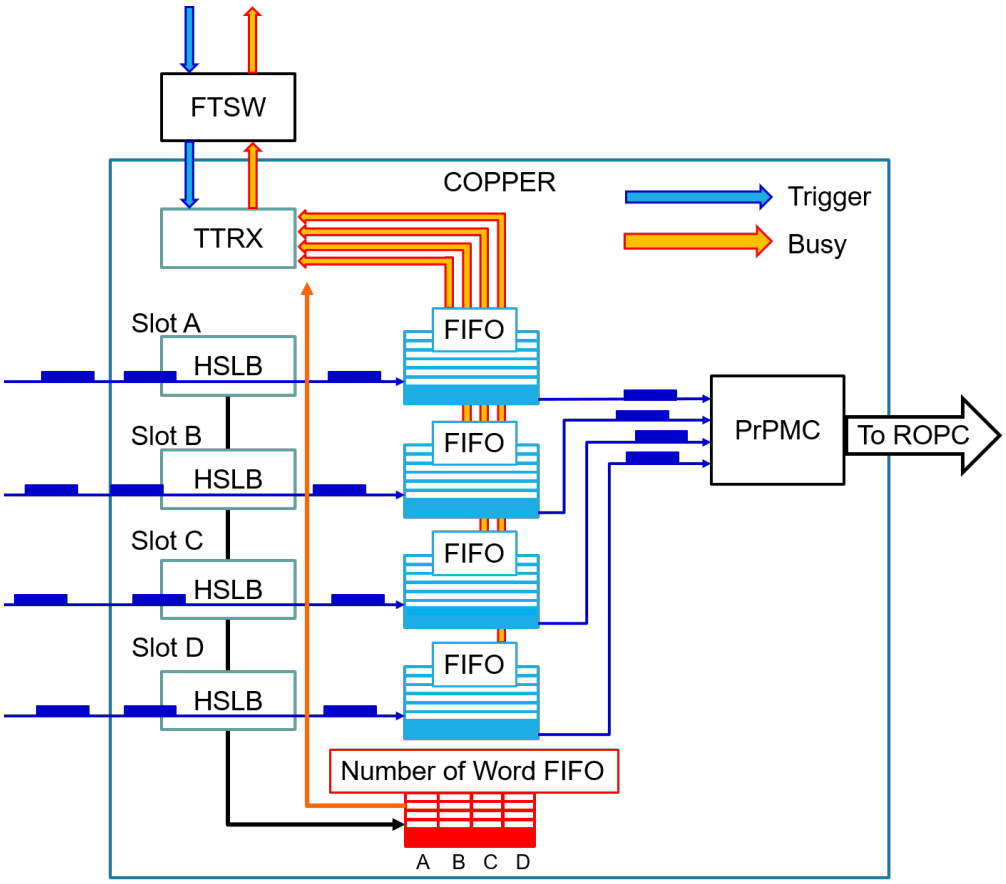


Fig. 37: The flow of busy signal issued by COPPER board. When the data size being stored in the event FIFO for each HSLB exceeds a threshold, the busy signal is issued from event FIFO. The number of word FIFO, which stores the data size for each HSLB slot, also issued the busy signal when the number of word FIFO is almost full.

3.3.2 From front-end electronics

In addition to the busy signal from COPPER, FTSW is also possible to collect busy signal from Front-end electronics.

The most stringent constraint among all the front end electronics is the buffer size of the SVD ASIC. In order to prevent overflow of SVD ASIC buffer, an emulator of the buffer of SVD ASIC is implemented to FPGA in the master FTSW. A trigger which causes buffer overflow is vetoed by this emulator even if there exists no busy signal from down stream FTSW. Owing to this veto system, it is expected that most of the buffer overflow in the front end electronics are suppressed beforehand. Thus

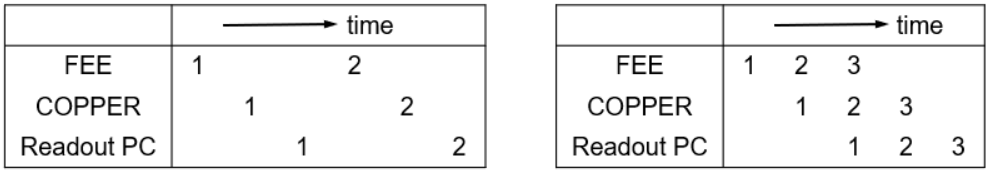


Fig. 38: The concept of the data processing flow for event-by-event readout (left) and pipeline readout (right). Each number means the trigger number which each module is processing. In the pipeline readout, a module can receive data from upstream module and at the same time send data to downstream module.

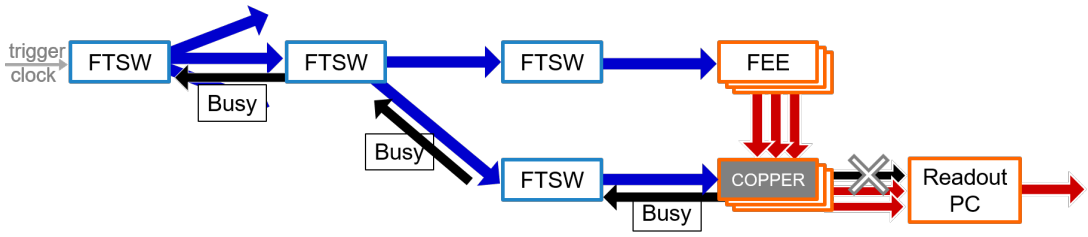


Fig. 39: Flow of busy signal collection. When a COPPER board issues busy signal, the busy signal is collected to master FTSW via intermediate FTSWs.

the amount of busy signal from front-end electronics is expected to be small compared to the busy signal from COPPER during a stable data acquisition system operation.

3.4 Monitoring system for Trigger timing distribution system

If any busy signal is issued from down stream FTSW TTD caanot distribute triggers anymore, thus the amount of busy signal can be regarded as a dead time of Belle II data acquisition. Dead time in TTD directly causes decrease in the amount of data obtained by Belle II experiment, so it is necessary to keep watch to the behavior or functionality of busy signal in TTD during experiment. Before Belle II phase2 run, the state of TTD was not recorded to log, and it was difficult to restore the amount of dead time or the cause of dead time.

Here in this work, a monitoring system which extract information of busy signal from master FTSW was implemented to TTD, and information of TTD begins to be recorded into log.

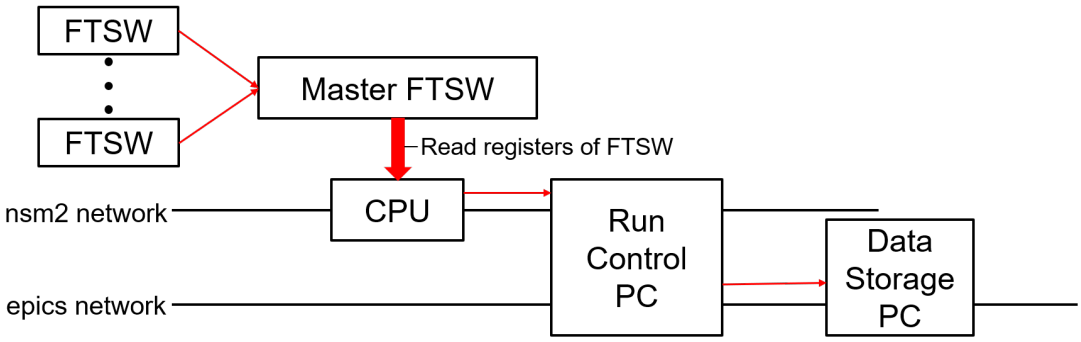


Fig. 40: The schematics of busy signal monitoring. The information about busy signal in the master FTSW is read by the CPU which is placed in the same VME crate as the master FTSW. The obtained busy information is shared with other PCs using NSM2.

3.4.1 Structure of TTD monitoring system

The master FTSW and CPU are placed in the same VME crate near Belle II detector. Registers of master FTSW can be accessed from the CPU.

One of the main FTSW component is Field Programmable Gate Array (FPGA), Xilinks Vertex 5, and the function of FTSW can be modified by reprogramming FPGA in FTSW. In order to observe the behavior of busy signal, the amount of busy signal is counted inside FPGA, and recorded into registers of FPGA. A program to access master FTSW runs in CPU which is connected to master FTSW via VME crate.

We prepared counters, named "cbusy" for busy signals from sub-detectors. At each clock, counters "cbusy" are added one if busy signal is being issued from downstream FTSW. These counters are read out each second from the program. The dead time for each sub-detector is calculated as

$$D = \frac{\mathrm{cbusy} - \mathrm{cbusy}_{\mathrm{prev}}}{\mathrm{ctime} - \mathrm{ctime}_{\mathrm{prev}}} \tag{13}$$

where D is the dead time, ctime is a counter for system clock of FTSW, and $\mathrm{cbusy}_{\mathrm{prev}}$ and $\mathrm{ctime}_{\mathrm{prev}}$ are values of counters which is read 1 second ago.

The overview of TTD monitoring system is shown in Fig.40. Sharing of data among PCs on network is done using NSM2, which is explained in Section 3.6. In addition to NSM2, EPICS are used as a method to archive information from FTSW. Network

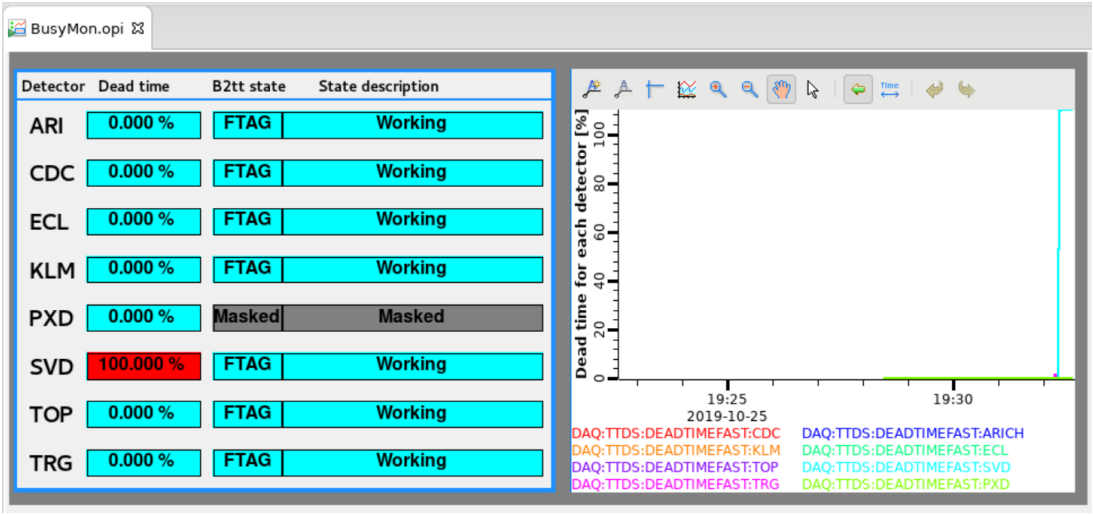


Fig. 41: Appearance of monitoring screen prepared for Belle II shifters.

for NSM2 and network for EPICS are discrete, so busy information is stored via a PC named Run Control PC, which is connected to both networks.

3.4.2 Monitoring screen

Not only archiving busy information to storage, experimental shifters should be able to supervise how much dead time there is when data acquisition is on-going. Monitoring screen for experiment shifters are prepared as is shown in Fig.41.

3.5 Performance of monitoring system in Phase 3 run

The busy monitoring system has been in operating during phase3 run in 2019. The performance of TTD monitoring system was analyzed using data taken in phase 3 run.

The relation between dead time and trigger rate is analyzed using the information from monitoring system for TTD. Only stable physics runs are used for this performance analysis. The selection criteria is

- During phase 3 operation, May 9, 2019 - June 26, 2019
- Run which has more than 10 minutes run length
- Trigger input from Global Decision Logic (GDL)

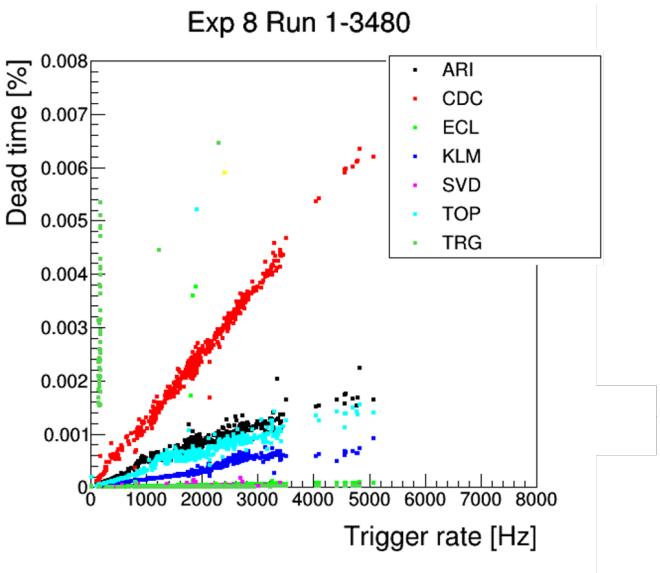


Fig. 42: The relation between trigger rate and dead time in linear scale. Each point represents the average of trigger rate and dead time during a run. Each color represents each sub-detectors.

3.5.1 Observed dead time in phase3

The relation between trigger rate and dead time is in Fig.42 and Fig.43. Under the run selection criteria, the maximum input trigger rate for master FTSW is 5000 Hz.

The relation between trigger rate and dead time from each sub-detector except for PXD is plotted respectively. Each point represents the average of trigger rate and dead time for each run, and each color represents each detector. The structure of read out system for PXD is different from other detectors as explained in Section 4.1, so we will consider detectors except for PXD.

As seen in Fig.42 and 43, in phase3 run linear relationship between trigger rate and dead time is observed for all sub-detectors, although the scale of the gradient of lines are 100 times different between sub-detectors. The relation between trigger rate and dead time is fitted for each sub-detector by $y = Cx$ where C is the fit variable. The fit results and their errors for parameter C are listed in Table.2.

In Belle II physics run under 5kHz trigger rate it is expected that dead time among data acquisition system is negligibly small, because no data flow bottleneck in data acquisition system is expected. Using this monitoring system, we proved that dead

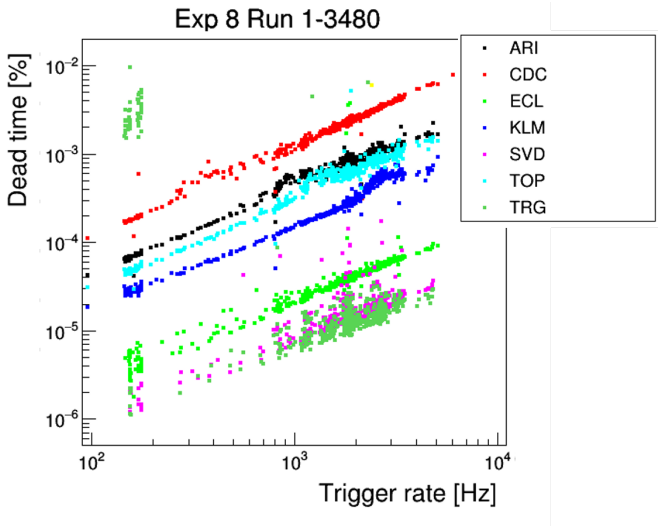


Fig. 43: The relation between trigger rate and dead time in logarithmic scale. Each point represents the average of trigger rate and dead time during a run. Each color represents each sub-detectors.

Sub-detector	Value of fitted parameter [10^{-6}%/Hz]
ARICH	0.34 ± 0.004
CDC	1.1 ± 0.009
ECL	0.023 ± 0.004
KLM	0.14 ± 0.002
SVD	0.0055 ± 0.0002
TOP	0.28 ± 0.01
TRG	0.024 ± 0.008

Table 2: The fitted values and their errors

time is smaller than 0.01% in stable runs.

In order to understand this linear relationship, the relation between the gradient of line and the number of COPPER for each sub-detector is analyzed.

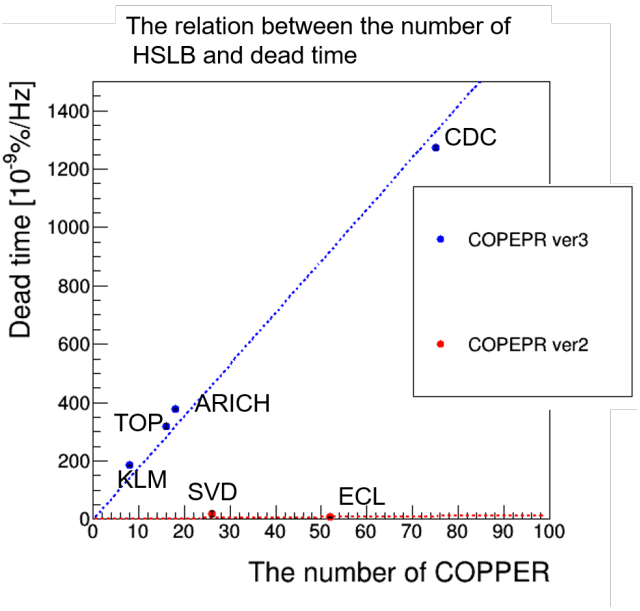


Fig. 44: The relation between the number of COPPER and the amount of dead time. Blue and red points represents detectors using COPPER version 3 and COPPER version 2 respectively.

3.5.2 A relation between dead time and the number of COPPER

Fig.44 and Fig.45 show the relation between dead time and number of COPPER or HSLB for each sub-detectors. In the figure, blue points and red points represent detectors using COPPER version 3 and version 2 respectively.

ARICH, CDC, KLM and TOP are using COPPER version 3. For those detectors there exists the linear relationship between the number of copper and the amount of dead time per one trigger. In phase3 run, 4 HSLB are used for one COPPER in those detectors using COPPER version 3, thus the dependence of dead time on the number of COPPER and HSLB is exactly same. The plot is fitted by line. From the result of fitting with a straight line, the amount of dead time is calculated to be

$$(1.77 \pm 0.07)^{-8} \quad [\%/\text{trigger/copper}]$$
$$(4.44 \pm 0.02)^{-9} \quad [\%/\text{trigger/hslb}]$$

On the other hand, for those which use COPPER version2, ECL and SVD, the amount of dead time is 100 times smaller compared to detector with COPPER version

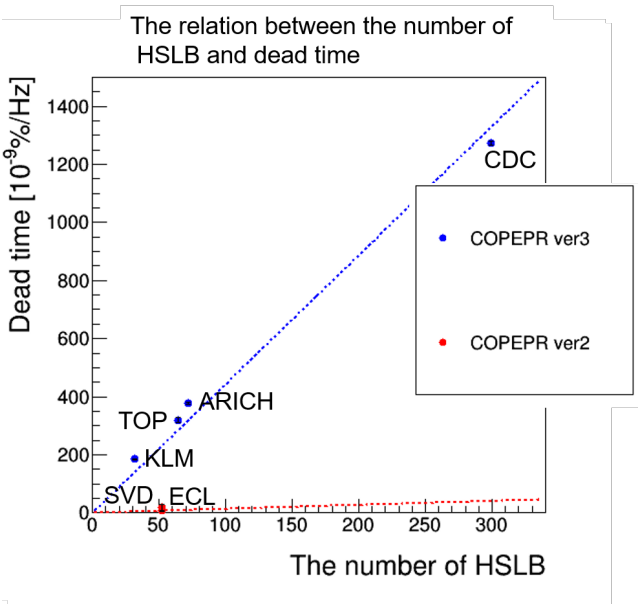


Fig. 45: The relation between the number of HSLB and the amount of dead time. Blue and red points represents detectors using COPPER version 3 and COPPER version 2 respectively.

3. No dependence of dead time on the number of copper or HSLB observed for these two detectors.

As mentioned in the previous subsection, the FIFO buffer between HSLB and PrPMC is the source of busy signal from COPPER. This buffer is prepared for each HSLB, thus the amount of dead time should depend on the number of HSLB used per 1 COPPER. In Belle II phase3 run, four HSLB are used for 1 COPPER board in all detectors using COPPER version3, two HSLB in ECL and one HSLB in SVD. No dependence of the amount of dead time is observed in Fig.45. Thus the observed dead time among ARICH, CDC, KLM and TOP is considered to be specific problem for COPPER version 3.

The differencde between COPPER version 2 and 3 is:

- Upgrade of clock distribution from TTRX to HSLB module
- Upgrade of On-board ethernet transceiver to Gigabit transceiver

and these upgrades don't change the handling of busy signal or the whole readout scheme in COPPER board.

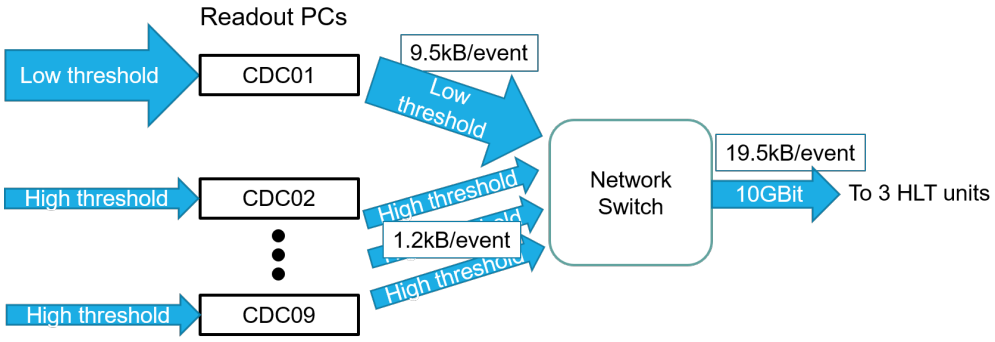


Fig. 46: The setup for the analysis of dead time due to the data flow bottlenecks. Data size for only CDC01 is increased by lowering threshold.

3.6 Analysis of the behavior of dead time due to data flow bottleneck

Based on the implemented monitoring system, we analyzed the behavior of dead time due to the backpressure from data flow bottlenecks.

Each readout PC and event builder 1 network switch is connected using two 1GBit ethernet cable for readout PC of SVD, and one cable for PC of other detectors. Thus if data flow from each readout PC exceeds 250MB/s for SVD or 125MB/s for other detectors, COPPER is expected to issue busy signal due to the backpressure from readout PC.

3.6.1 Setup for the analysis

Only CDC is used for this analysis. The setup for this work is shown in Fig.46. We can change the zero suppression threshold of CDC data via CDC COPPER, thereby we can increase data size per one COPPER by lowering the threshold. CDC uses 299 COPPER and 9 readout PCs to obtain data. 9 readout PCs are named CDC01 CDC09. In this analysis, we increased data size for only read out PC CDC01. The average input data size for readout PCs are shown in Table.3. Data size is 9.5 kByte per event in CDC01, and under 2 kByte in other readout PCs. The bottleneck by the 1GBit ethernet between readout PC and EB1 network switch is 125MB/s. The total data rate from CDC01 reaches 125MB/s around the 13kHz trigger rate, thus it is expected that we observe the dead time due to the bottleneck under trigger rate higher than 13kHz. We analyzed the behavior of dead time with the trigger rate

Read out PC	Input data size [kByte]
CDC01	9.5
CDC02	1.6
CDC03	1.2
CDC04	1.2
CDC05	1.3
CDC06	1.2
CDC07	1.3
CDC08	1.1
CDC09	1.1
Total	19.5

Table 3: The input data size for each readout PCs in the dead time analysis. In this analysis, data size for only CDC01 is increased by lowering threshold for measured voltage in CDC.

between 11kHz 13kHz.

3.6.2 The result of the bottleneck analysis

Under trigger rate higher than 12.5kHz, dead time larger than 50% begins to be observed. Fig.47 shows the behavior of input and output trigger rate. In the run shown in Fig.47, trigger output rate begins to drop three minutes after the run start. The close-up of the behavior of trigger rate and dead time around the timing large dead time begins to be observed is Fig.48 and Fig.49. Dead time larger than 50% is observed once in about 10 second after three minutes from run start.

The relation between the length of data taking without large dead time from run start and trigger rate is shown in Fig.50. As trigger rate and data throughput rate increases, large dead time begins to be observed faster from run start.

The relation is fitted by inverse relationship graph. The fit result is

$$y[second] = \frac{1045[\mathrm{MByte}]}{9.5[\mathrm{KByte/event}] \times x[\mathrm{Hz}] - 117[\mathrm{MByte/s}]} \tag{14}$$

Fig. 47: The behavior of input and output trigger rate for master FTSW under 12.7kHz input trigger rate. The blue and orange lines represent input and output trigger rate respectively. Output trigger rate begins to drop three minutes after the run start.

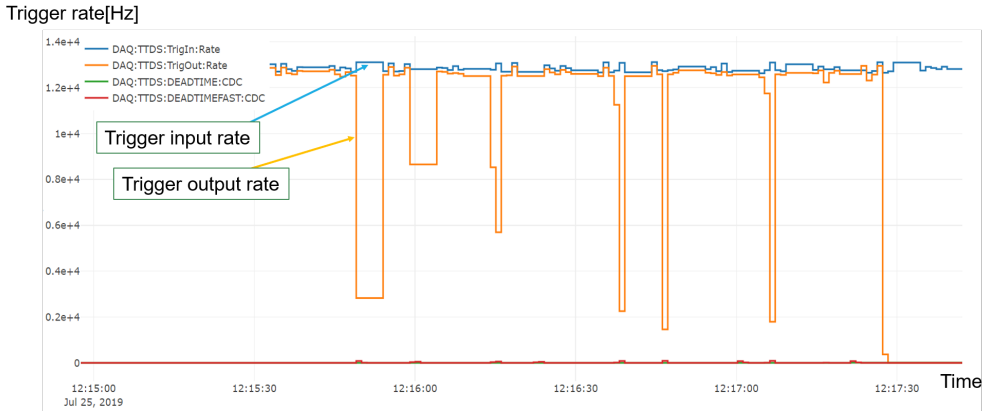


Fig. 48: The detailed figure of the behavior of the trigger rate around the timing when large dead time begins to be observed. The blue and red lines represents trigger input and output rate for master FTSW respectively.

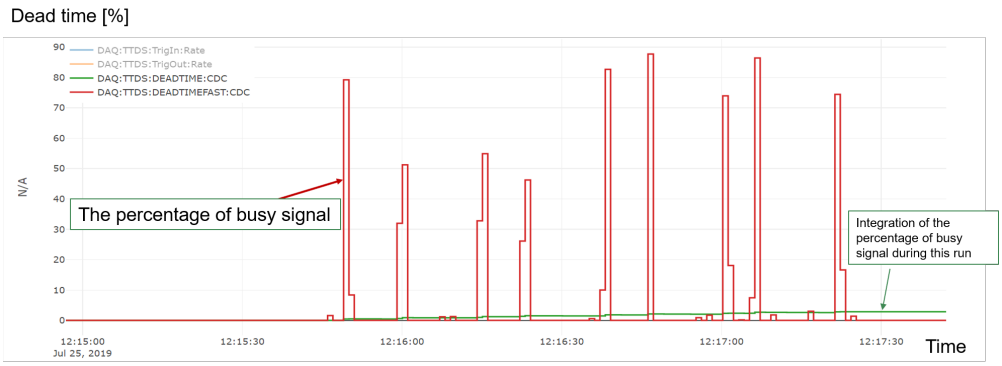


Fig. 49: The detailed figure of the behavior of dead time around the timing when large dead time begins to be observed. The red line represents the dead time per 1 second.

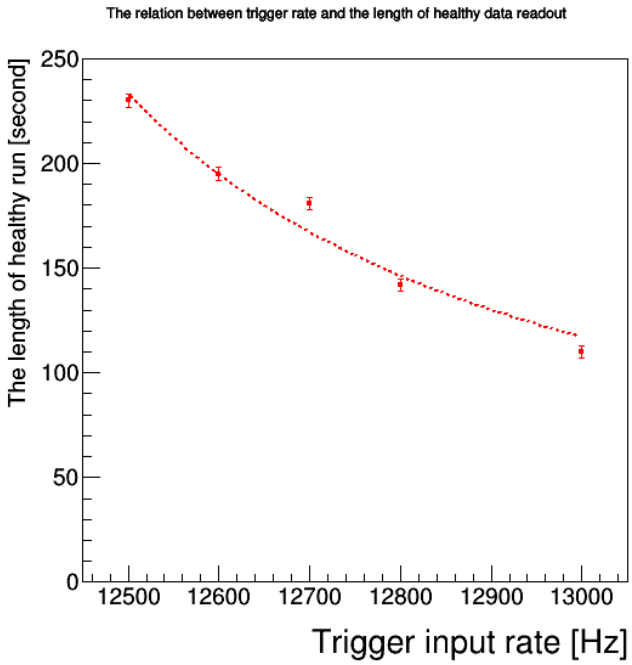


Fig. 50: The relation between input trigger rate and the length of data acquisition without large dead time from the run start. As the trigger rate increases, the large dead time begins to be issued sooner after run start.

The fit result can be modeled as follows: 1GB buffer for receiving data from sub-detectors and sending data to the EB1 network switch is prepared in each readout

PC. When data throughput in a readout PC exceeds the bottleneck due to the 1GBit ethernet cable, unsendable data is stored to the buffer. When the buffer is fully occupied by unsent data, readout PC cannot receive data from COPPERs anymore and begins to cause backpressure to COPPERs.

In the fit result, the 1045 MByte in the nominator represents the buffer size, and the 117 MByte/s in the denominator represents the maximum throughput of data in the readout PC.

3.6.3 Summary of the monitoring system for TTD

In this section, the implementation of the monitoring system for TTD is explained. The performance of the monitoring system for TTD is evaluated using information archived in phase 3 run. Using the monitoring system, we confirmed that the data acquisition system has sufficiently small dead time under 0.01% in phase 3 stable runs.

In addition to the performance evaluation of the monitoring system, we found that COPPER version 3 itself issues a busy signal proportional to the number of triggers distributed to COPPER. This dead time leads to 0.062% dead time under 30kHz from ARICH, CDC, KLM, and TOP.

4 Estimation of data size under high luminosity

The amount of background signal increases with the increase of the luminosity of SuperKEKB. Under high luminosity, both trigger rate and data size increase, thus data throughput rate might exceed the limit of data acquisition capability.

In this section, we observe data flow in Belle II phase 3 run to estimate future data throughput rate and to analyze what kinds of upgrades will be needed for DAQ.

4.1 Sources of beam background

In this analysis, mainly two types of beam background sources is considered : single beam background, luminosity dependent background. The amount of background from these sources increases with beam current and luminosity. These background signal reduces performance of detectors, and at the same time increases data size to be read out. Thus large data size due to background signals can cause stagnation of data readout.

4.1.1 Single beam background

Single beam background can be divided to three types of background : (i) beam gas, (ii) Touschek effect, and (iii) synchrotron radiation.

(i) The first comes from beam gas background. A beam particle in beam bunch is deflected from nominal orbit by bremsstrahlung and coulomb scattering between gas atomic in the beam pipe. When those deflected beam particles hit beam pipe wall, secondary particles is produced in electromagnetic shower. The secondary particle reaches detectors and becomes background.

(ii) The second comes from Touschek effect. Touschek effect is caused by intra-bunch scattering of beam particles. The energy of beam particles is changed from its nominal value by elastic scattering between two particles in the same beam bunch. Beam particles whose energy is deviated from beam bunch then becomes background.

(iii) The third comes from synchrotron radiation. When beam particles are strongly bent by magnet, beam particles emit photons. This is the synchrotron radiation (SR) process. These photons hit beam pipe and scattered to the detector. The effect of SR in Belle II is predicted to be negligible by Monte Carlo sumulation. In this analysis,

we do not include the effect of SR in data size estimation.

4.1.2 Luminosity dependent backgrounds

Background signal can be produced by collision processes, for example radiative Bhabha scattering. In case of radiative Bhabha scattering, the produced photon can travel straight along beam pipe. The photon then collides with beam pipe as beam pipe bends, and produces neutrons. This causes background particle to enter detectors.

4.2 Method to analyze data flow

In this analysis, we discuss about the potential bottlenecks around COPPER boards and ROPCs. Data size for each COPPER board and ROPC is obtained from physics data obtained in Belle II operation. Parameters related to SuperKEKB accelerator are obtained from records on EPICS archiver. Using these information, the relation between data size, luminosity and beam current is analyzed.

We selected phase 3 runs to be used for this analysis by the following criteria.

- Run which has more than 10 minutes run length
- Trigger input from Global Decision Logic (GDL)

For runs which fulfills this criteria, the averages of data size per event are calculated. The relation between average data size and SuperKEKB accelerator parameters are analyzed.

4.3 Data size for each sub-detectors

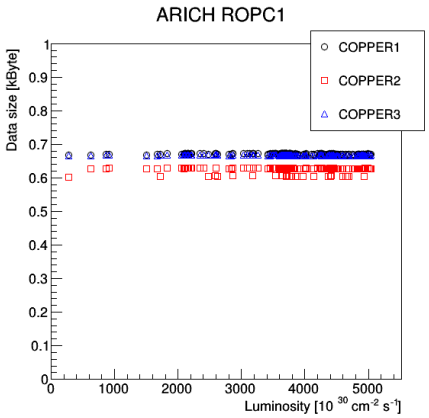
We will analyze data size for 6 sub-detectors, ARICH,CDC,ECL,KLM,SVD,TOP.

4.3.1 ARICH

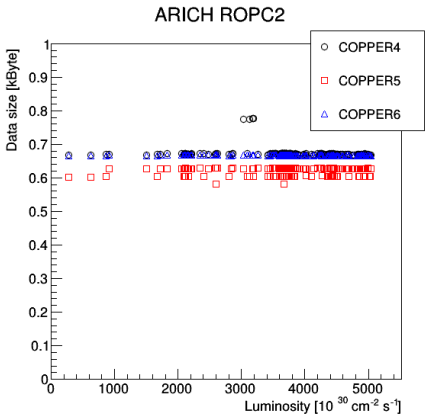
The relations between luminosity and data size for ARICH COPPERs are shown in Fig.51. The relation for ARICH readout PCs are shown in Fig.52.

ARICH observes Cherenkov rings from particles, therefore one particle coming from collision event is detected by multiple MPPC channels. However, a background particle like photon is detected by only a few channel, thus the effect of background on data size is small in ARICH. This tendency is observed in Fig.51 and Fig.52, where

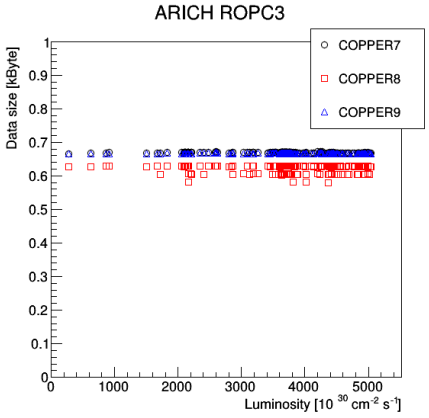
data size for COPPERs and readout PCs are almost constant against luminosity. For COPPERs represented as red points in the figure, the data size is smaller than the rest of COPPERs. This is because of the difference in the number of HAPDs connected one merger boards.



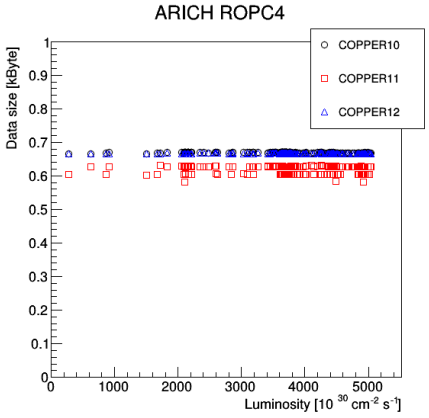
(a) ARICH ROPC01



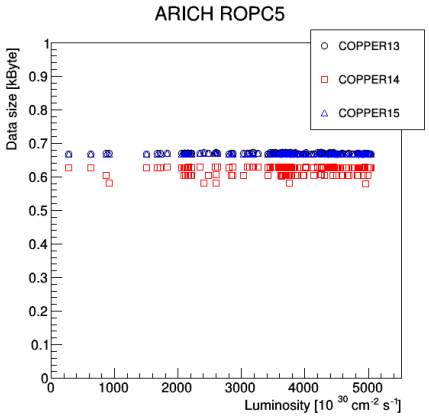
(b) ARICH ROPC02



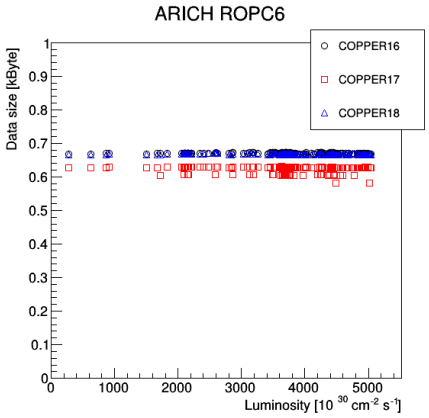
(c) ARICH ROPC03



(d) ARICH ROPC04

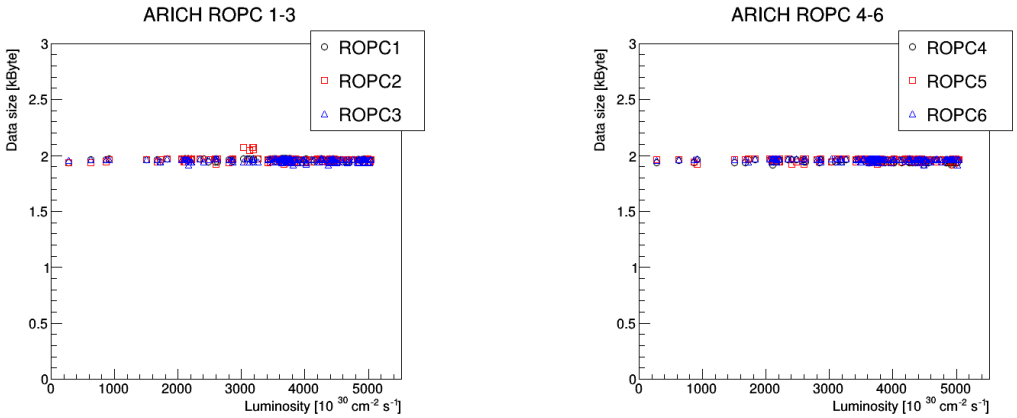


(e) ARICH ROPC05



(f) ARICH ROPC06

Fig. 51: The relation between luminosity and data size for ARICH COPPER. The data size for each COPPER is constant against luminosity.



(a) ARICH ROPC01-03

(b) ARICH ROPC04

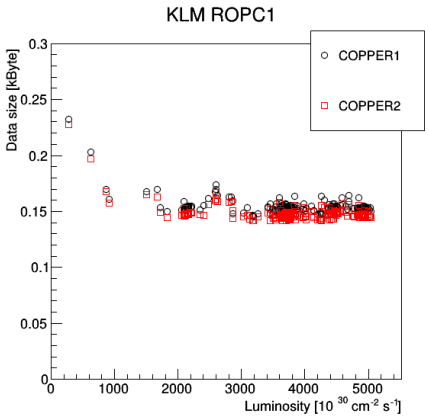
Fig. 52: The relation between luminosity and data size for ARICH Readout PC.

4.3.2 KLM

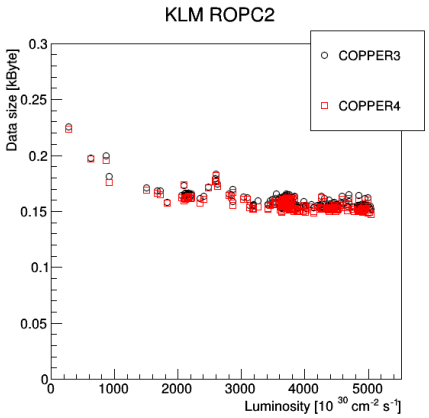
The relations between luminosity and data size for KLM COPPERs are shown in Fig.53. The relation for KLM readout PCs are shown in Fig.54b.

As explained in section 2, KLM consists of BKLM and EKLM. Resistive plate chambers are used for BKLM. On the other hand detector using scintillator strips are used for EKLM. COPPERs 1-4 and readout PCs 1-2 corresponds to data from BKLM, and the rest COPPERs and readout PC from EKLM. In Fig.53a and 53b, data size decreases with increasing of luminosity.

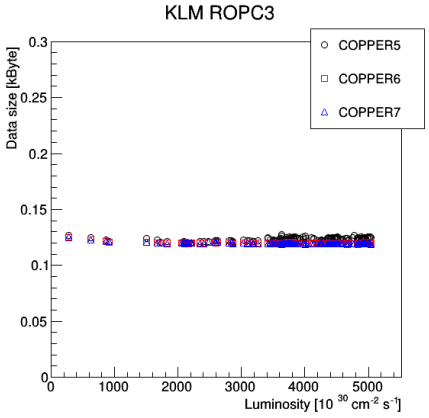
This is due to the effect of neutron background. A discharge of the RPC induced by the background neutron suppresses the electric field in the RPC gap for 1 millisecond. Until the electric field recovers, the RPC becomes temporarily blind to the passage of a true muon. This negative correlation between data size and luminosity is not observed in the EKLM region in Fig.53c and Fig.53d, where RPCs are replaced by a detector using sillicon strip. In this analysis, we do not estimate data size under high luminosity from phase 3 data.



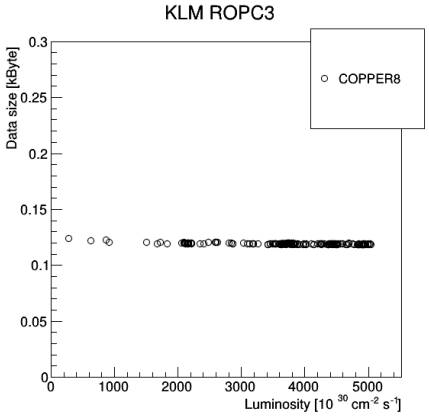
(a) COPPERs connected to KLM ROPC01



(b) KLM ROPC02

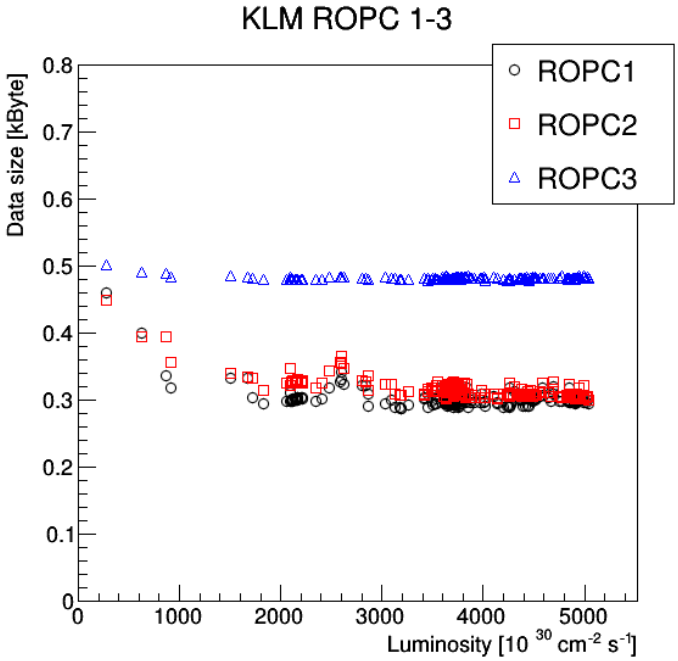


(c) KLM ROPC03 COPPER5-7



(d) KLM ROPC03 COPPER8

Fig. 53: The relation between luminosity and data size for KLM COPPER. ROPC1 and ROPC2 correspond to BKLM, and ROPC3 corresponds to EKLM. The data size for COPPERs connected to BKLM decrease against luminosity, while the data size for COPPERs connected to EKLM do not decrease.



(a) KLM ROPC01-03

(b) The relation between luminosity and data size for KLM Readout PC. ROPC1 and ROPC2 correspond to BKLM, and ROPC3 corresponds to EKLM. The data size for ROPCs connected to BKLM decrease against luminosity

4.3.3 SVD

SVD is the most inner detector except for PXD, thus most affected by beam background effect. The effect of luminosity dependent background is estimated to be more than 10 times smaller than single beam background under the target luminosity. The single beam background effect is expected to be dominant. Thus SVD receives the effect of SuperKEKB accelerator condition such as the settings of collimator.

An dedicated analysis about SVD strips occupancy has carried out by SVD group [13].In this analysis, we quote the result of [13] and estimate future data size. In the SVD occupancy analysis, SVD strip occupancies in phase 3 runs in May 2019 are compared to Monte Carlo simulation, and scale factors $(\text{data/MC})_{\text{May-2019}}$ are calculated. Furthermore, SVD strip occupancies under phase 3 target luminosity and beam current are estimated by Monte Carlo simulation. Finally, future SVD strips occupancies are calculated as

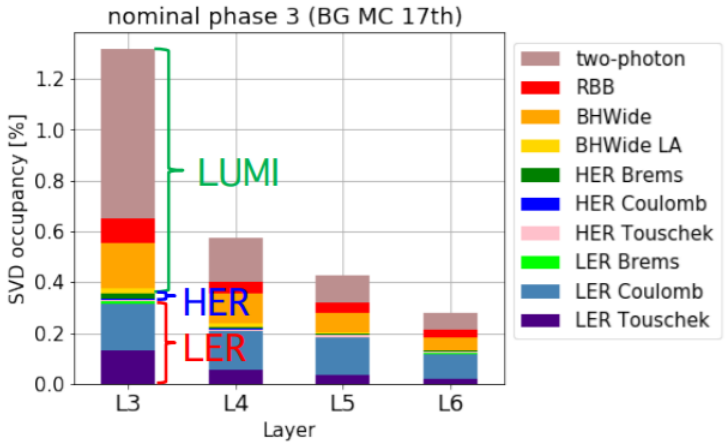


Fig. 55: Strip occupancy for SVD layer 3-6 estimated by Monte Carlo simulation [13]. Each color in the figure represents each background component.

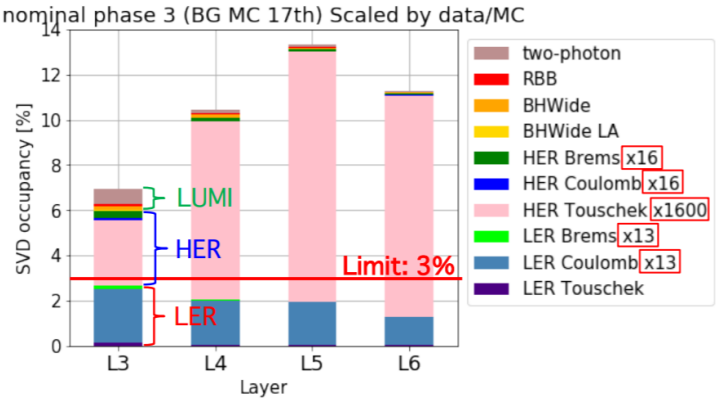


Fig. 56: Strip occupancy for SVD layer 3-6, which is estimated by Monte Carlo simulation in Fig.55 and scaled by the ratio data/MC in May 2019 run [13].

$$\text{Occupancy}_{\text{nominal}} = \text{MC}_{\text{nominal}} \times \frac{\text{Occupancy}_{\text{May-2019}}}{\text{MC}_{\text{May-2019}}} \tag{15}$$

where MC is the occupancy estimated by simulation under nominal phase 3 condition.

Future data size for SVD COPPERs and ROPCs are calculated based on the estimated SVD strip occupancy under the target luminosity. The data size estimation for COPPERs and readout PCs using the previous analysis [13] are shown in Fig.57 and 58. The red points represent the data size under nominal SuperKEKB parameters Table.7. The upper limit of strip occupancies are 3%, while it is estimated

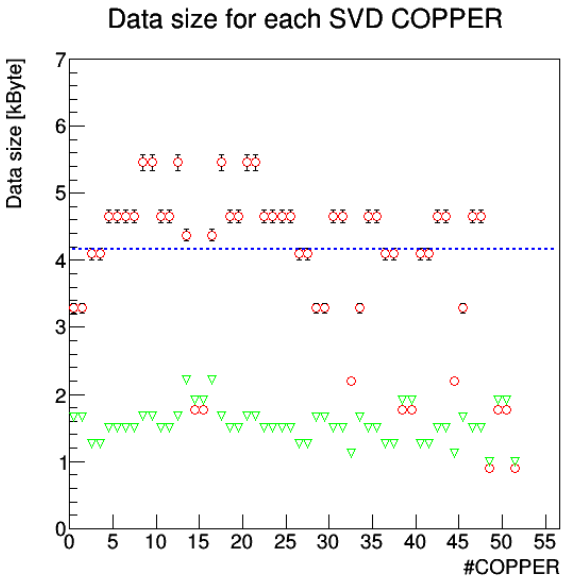


Fig. 57: The figure of estimated data size for each COPPER under phase 3 nominal condition. The blue line shows the upper limit of data size under 30kHz trigger rate due to 1GBit ethernet cable bottleneck. The red points are the data size under nominal SuperKEKB parameters Table.7. For green points, the strip occupancy for all SVD layers in phase 3 run are scaled so as to have 3% layer 3 strip occupancy, and data size is calculated.

that occupancies will exceed 3% under the nominl SuperKEKB parameters in phase 3 run. Therefore, we need to reduce the amount of background signals by modifying SuperKEKB collimator setups. For green points in the Fig.57, the strip occupancy for all SVD layers in phase 3 run are scaled so as to have 3% layer 3 strip occupancy. If the data size still exceed the COPPER bottleneck even with 3% layer 3 strip occupancy, we need to upgrade the data throughput of COPPER boards.

For SVD readout PCs, two 1GBit cables are connected per one PC. Therefore the bottleneck from SVD readout PCs is 250MB/s. The upper limit of data size per event is 8.2 kB/event under 30kHz trigger rate. As shown in Fig.57, data size from both COPPERs and readout PCs can exceed 8 kB/event.

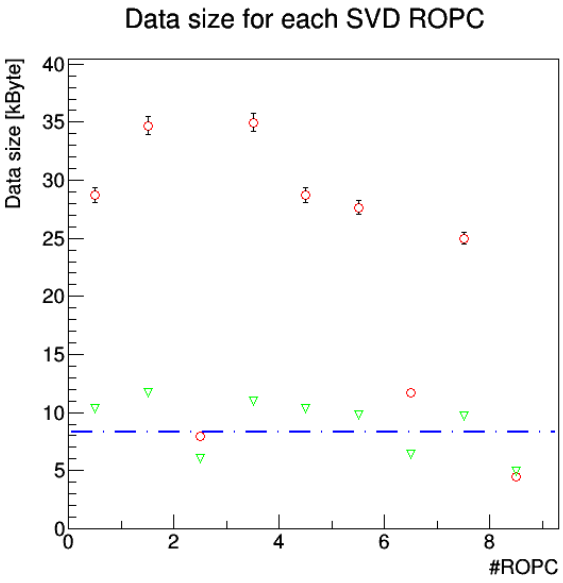


Fig. 58: The figure of estimated data size for each readout PCs under phase 3 nominal condition. The blue line shows the upper limit of data size under 30kHz trigger rate due to 1GBit ethernet cable bottleneck. The red points are the data size under nominal SuperKEKB parameters Table.7. For green points, the strip occupancy for all SVD layers in phase 3 run are scaled so as to have 3% layer 3 strip occupancy, and data size is calculated.

4.3.4 CDC,TOP, and ECL

The relation between luminosity and data size from COPPERs for these three sub-detectors are shown in Fig.59, 60 and 61.

For these three sub-detectors, data size is observed to increase with luminosity. As explained in section 4.1, there exists two kind of beam background. We parametrize data size as following equation.

$$S = f(C, B_H, T_H, B_L, H_L, D) \tag{16}$$

$$= C + B_H P_H I_H + T_H \frac{I_H^2}{(\sigma_y)_H n_b} + B_L P_L I_L + T_L \frac{I_L^2}{(\sigma_y)_L n_b} + \mathcal{L} D. \tag{17}$$

Here S is an average data size per event, C is a constant component including header and trailer for read out data and electrical noise, B and T are coefficients for beam gas background and Touschek effect, I is a beam current, P is an average

pressure over SuperKEKB ring, σ_y is a vertical beam size, n_b is a number of bunch, $\mathcal{L}$ is luminosity, and D is a coefficient for luminosity dependent component. The suffix H or L for each variable denotes a value for HER and LER respectively.

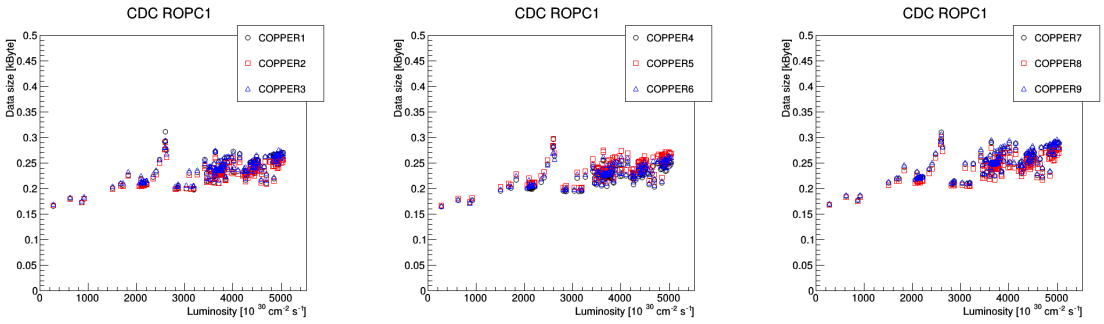
Among values in Eq.17, we fit C, B, T, and D for averaged data size obtained in phase 3 run, and extrapolate data size for phase 3 nominal accelerator setup.

Data size fit is done by minimizing χ^2 which is defined as

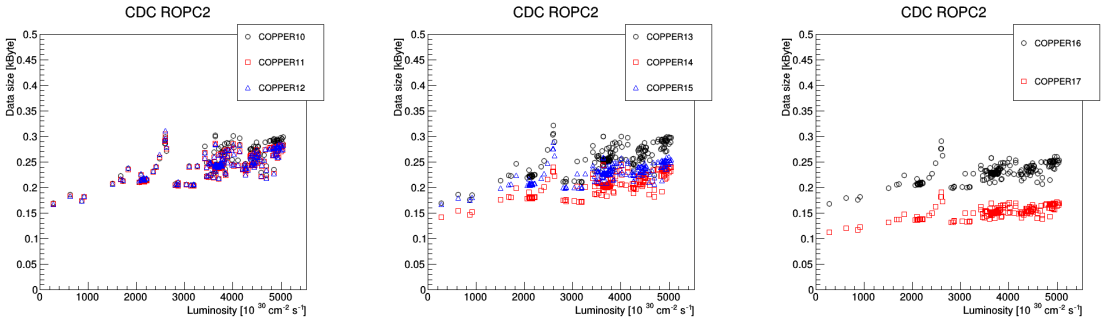
$$\chi^2 = \sum_{\text{good runs}} \left(\frac{y - f(C, B_H, T_H, B_L, H_L, D)}{\sigma} \right)^2 \tag{18}$$

where y is a measured average data size during a run and σ is an error for the average data size during a run. Errors for fitted parameters are calculated from 1σ confidence intervals.

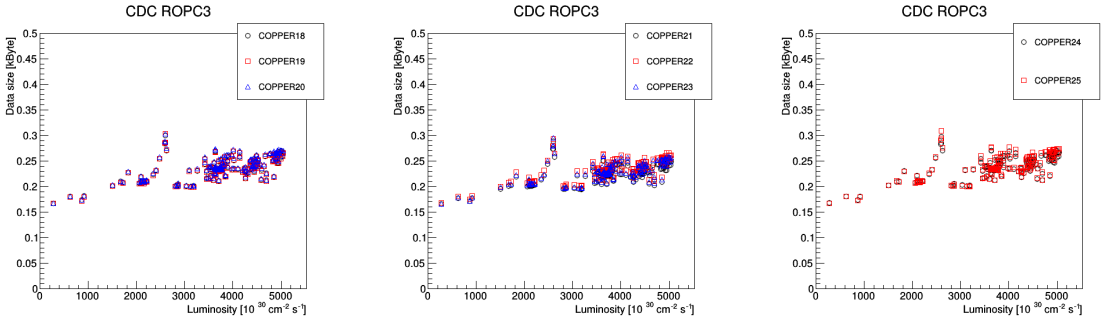
The fit results for data size in CDC, TOP ECL COPPERs are shown in Fig.62. Fit results for readout PCs are also shown in Fig.63. Red lines in those figures are the upper limit of data size per event due to 1GBit ethernet cable under 30kHz trigger rate.



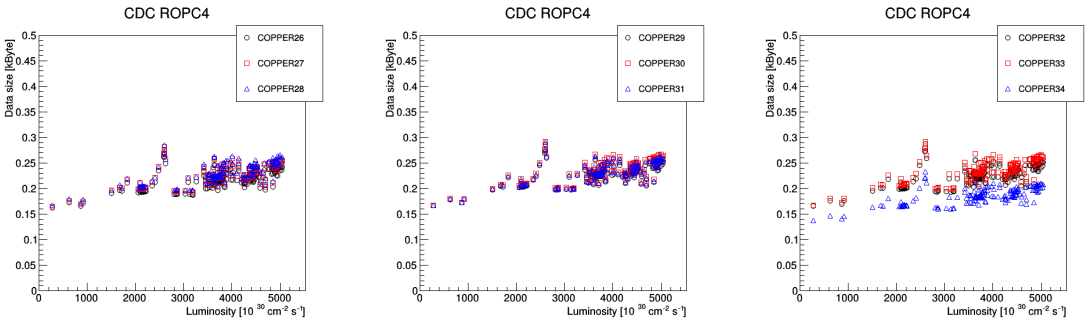
(a) Data size for COPPERs connected to CDC readout PC 01.



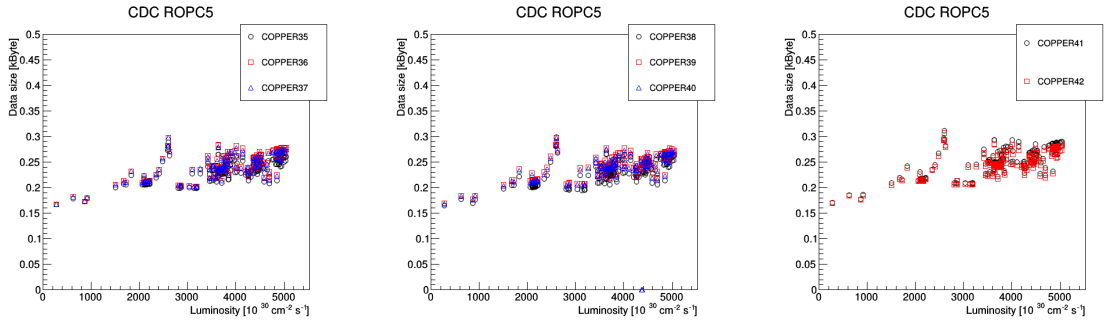
(b) Data size for COPPERs connected to CDC readout PC 02.



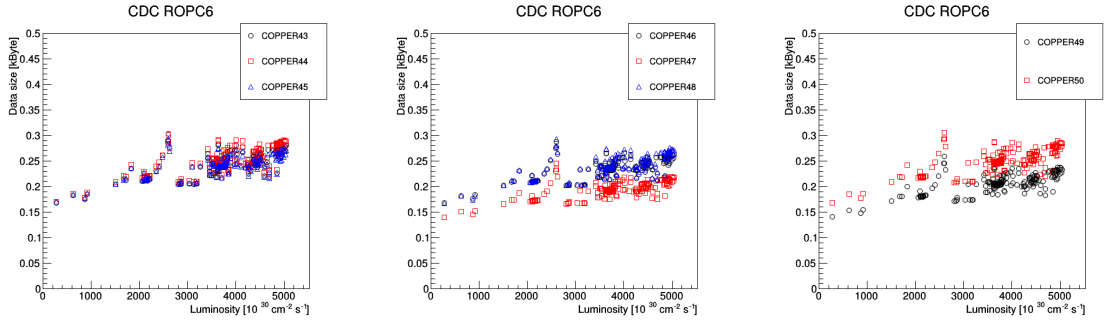
(c) Data size for COPPERs connected to CDC readout PC 03.



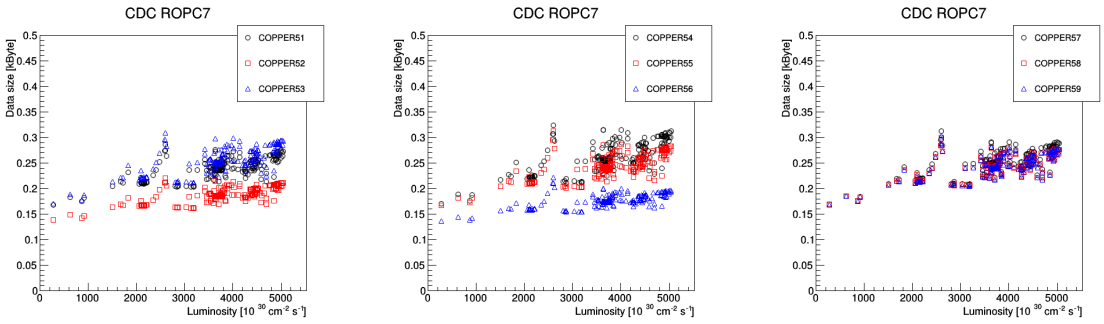
(d) Data size for COPPERs connected to CDC readout PC 04.



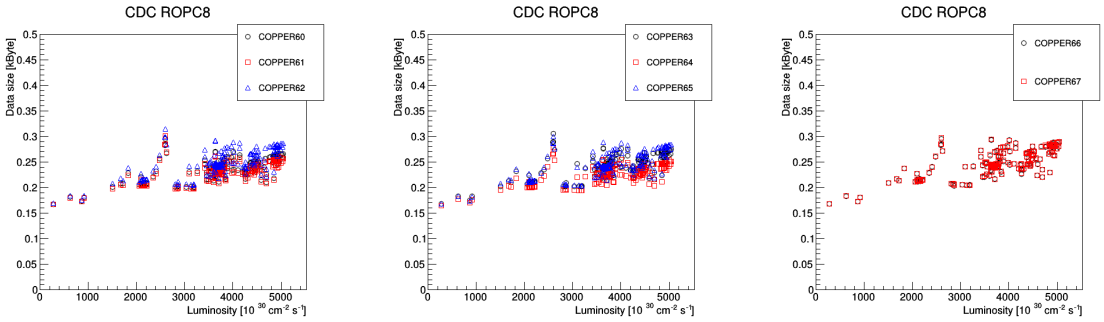
(e) Data size for COPPERs connected to CDC readout PC 05.



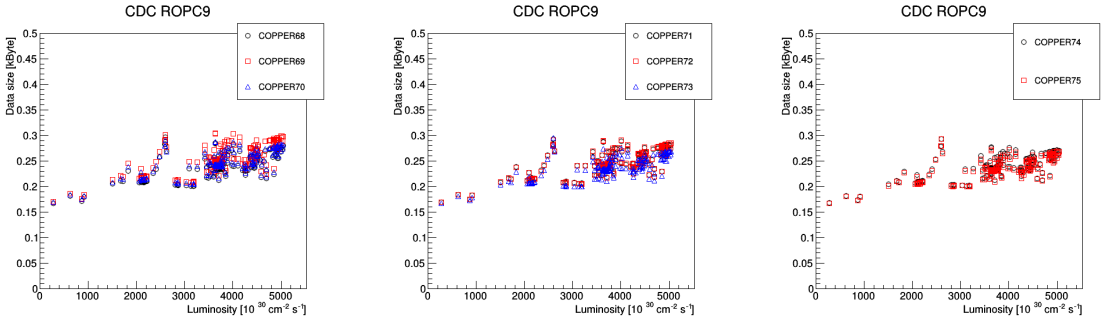
(f) Data size for COPPERs connected to CDC readout PC 06.



(g) Data size for COPPERs connected to CDC readout PC 07.

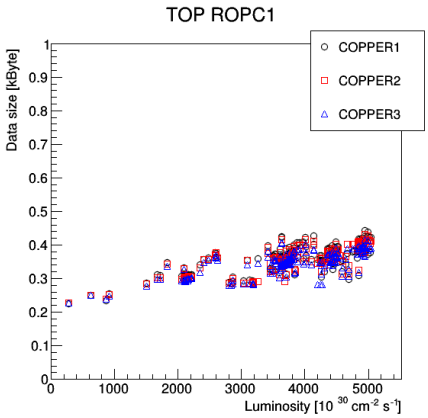


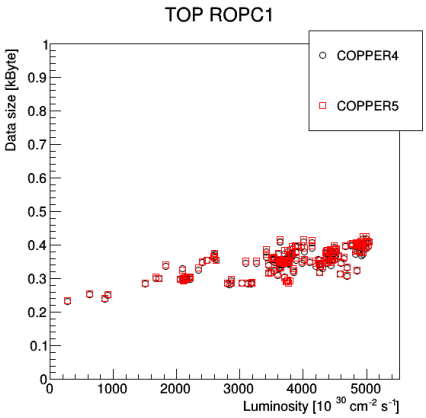
(h) Data size for COPPERs connected to CDC readout PC 08.



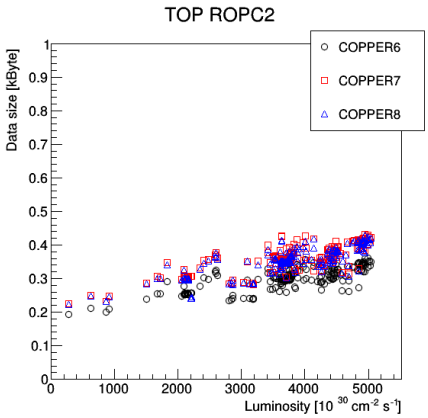
(i) Data size for COPPERs connected to CDC readout PC 09.

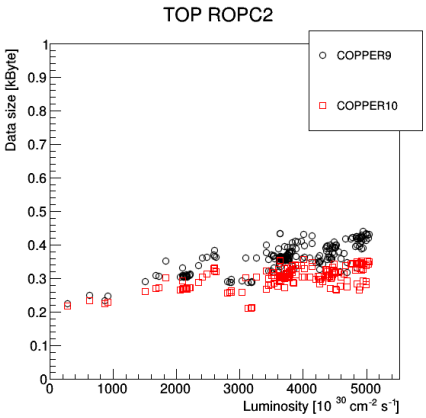
Fig. 59: The relation between luminosity and data size for CDC COPPER.



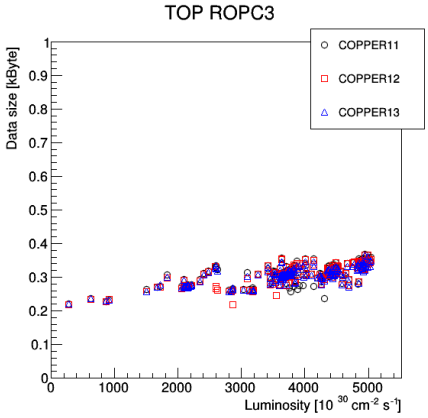


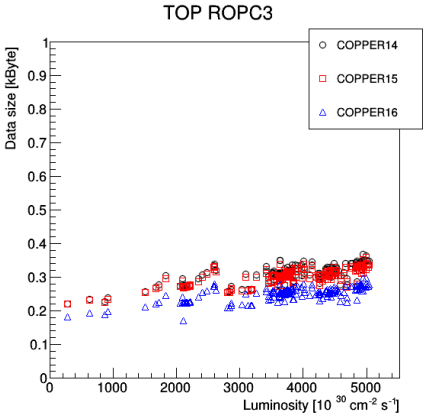
(a) Data size for COPPERs connected to TOP readout PC 01.





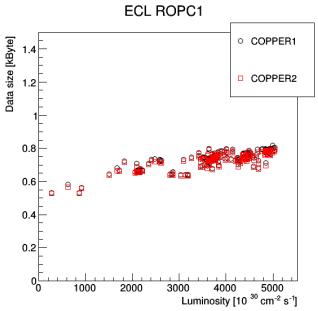
(b) Data size for COPPERs connected to TOP readout PC 02.



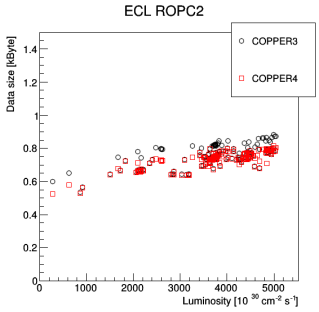


(c) Data size for COPPERs connected to TOP readout PC 03.

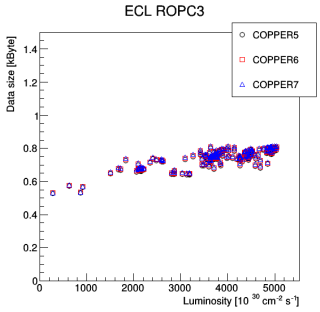
Fig. 60: The relation between luminosity and data size for TOP COPPER.



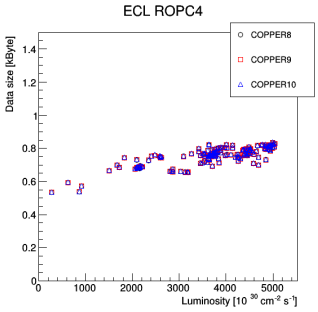
(a) COPPERs connected to ECL ROPC01



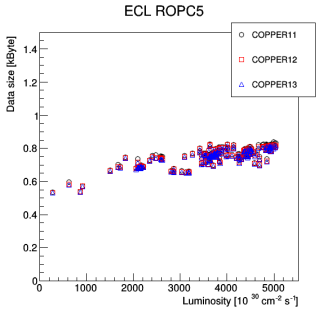
(b) ECL ROPC02



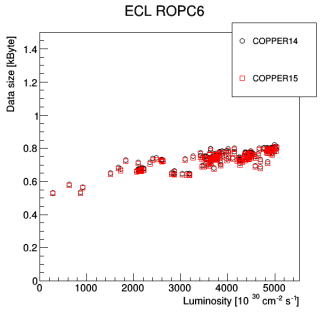
(c) ECL ROPC03



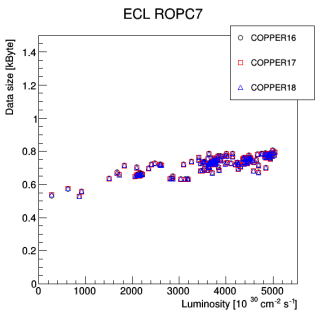
(d) ECL ROPC04



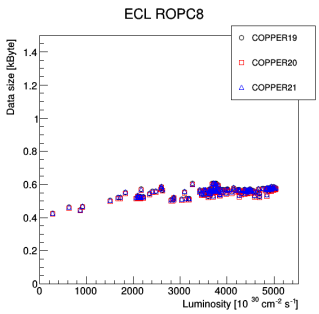
(e) ECL ROPC05



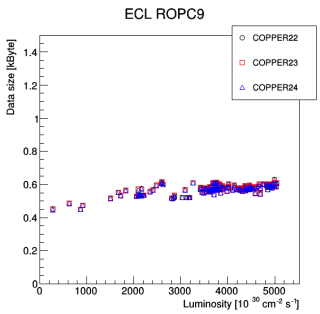
(f) ECL ROPC06



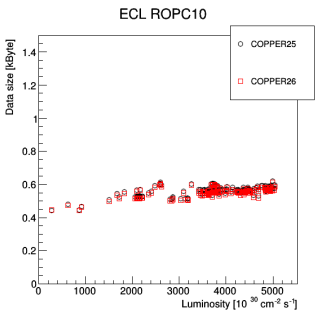
(g) ECL ROPC07



(h) ECL ROPC08

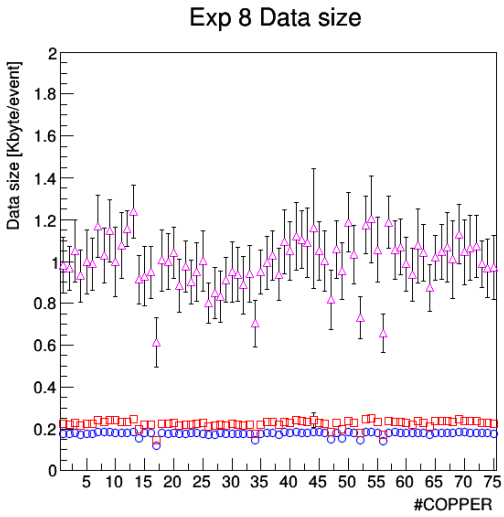


(i) ECL ROPC09

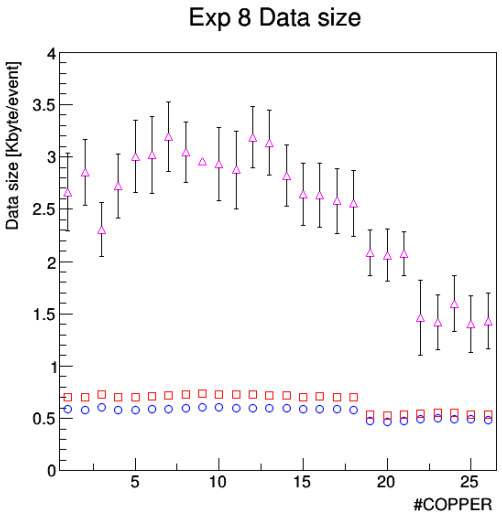


(j) ECL ROPC10

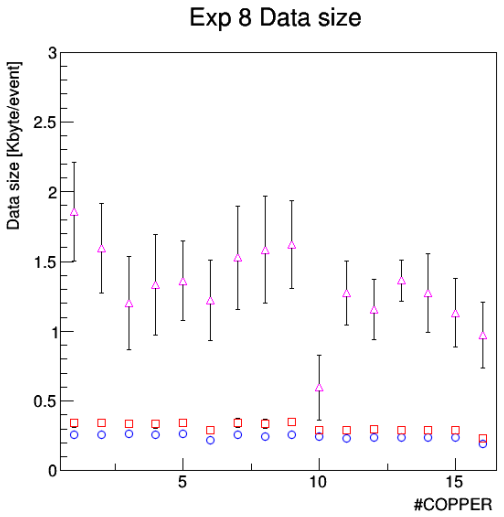
Fig. 61: The relation between luminosity and data size for ECL COPPER.



(a) Data size for 75 CDC COPPERs.

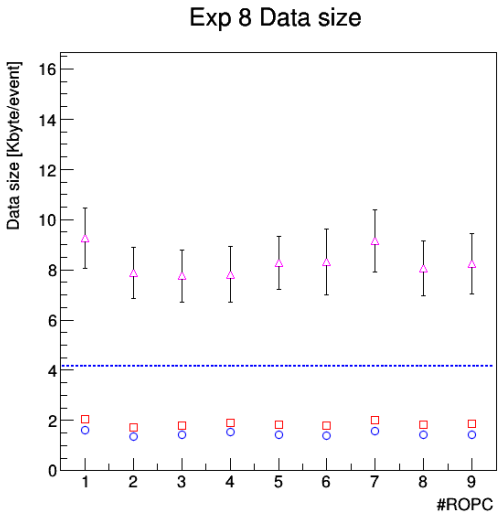


(b) Data size for 26 ECL COPPERs.

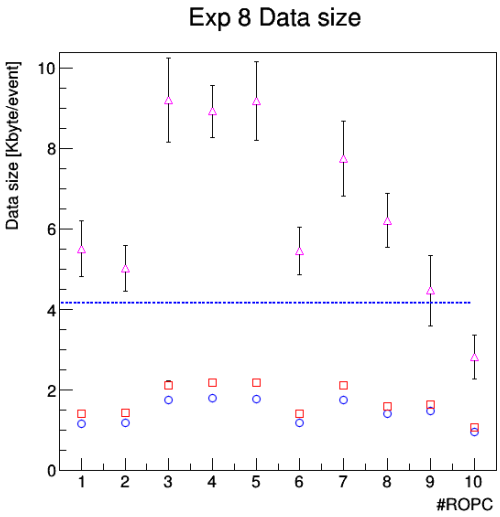


(c) Data size for 16 TOP COPPERs.

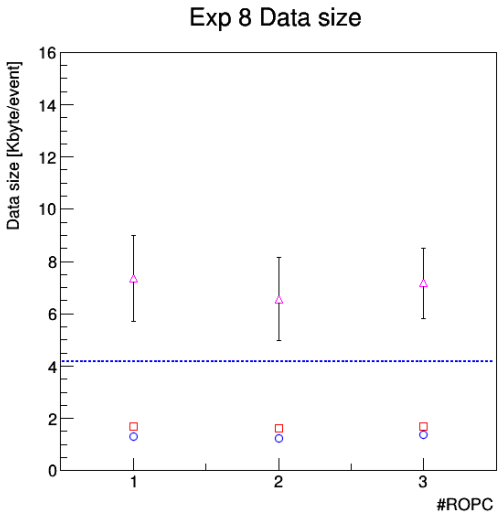
Fig. 62: The estimated data size per event for COPPERs in CDC, TOP and ECL. The blue points represent data size under luminosity and beam current equal to zero. The red points represent data size under accelerator parameters in a run (Phase 3 experiment 8 run 2549). The magenta points represent data size under target accelerator parameters in phase 3 run.



(a) Data size for 9 CDC readout PCs.



(b) Data size for 10 ECL readout PCs.



(c) Data size for 3 TOP readout PCs.

Fig. 63: The estimated data size per event for readout PCs in CDC, TOP and ECL. The blue points represent data size under luminosity and beam current equal to zero. The red points represent data size under accelerator parameters in a run (Phase 3 experiment 8 run 2549). The magenta points represent data size under target accelerator parameters in phase 3 run.

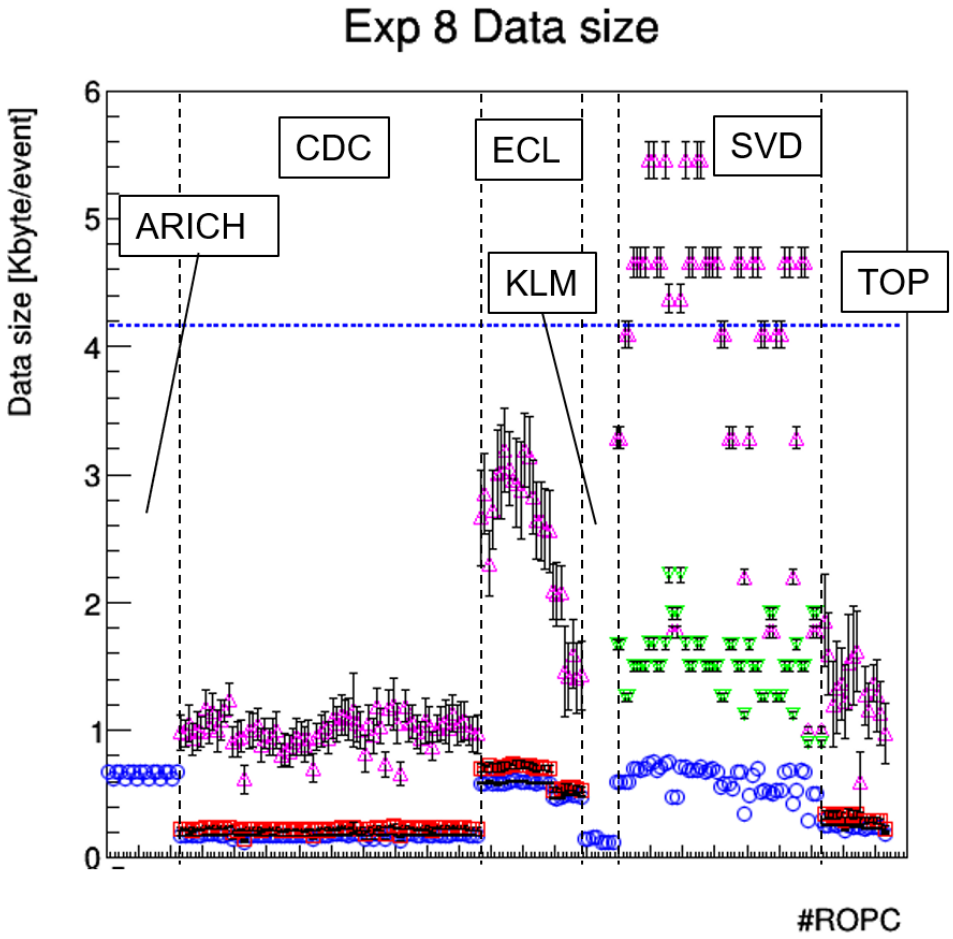


Fig. 64: The estimated data size per event for COPPERs in six sub-detectors. The blue points represent data size under luminosity and beam current equal to zero. The red points represent data size under accelerator parameters in a run (Phase 3 experiment 8 run 2549). The magenta points represent data size under target accelerator parameters in phase 3 run. For green points, the strip occupancy for all SVD layers in phase 3 run are scaled so as to have 3% layer 3 strip occupancy, and data size is calculated.

4.4 Summary of data size under high luminosity

The summary of estimated data size under high luminosity for COPPERs and readout PCs are shown in Fig.64 and Fig.65.

As shown in Fig.64, data size for SVD COPPERs can exceed 4 kByte/s, therefore

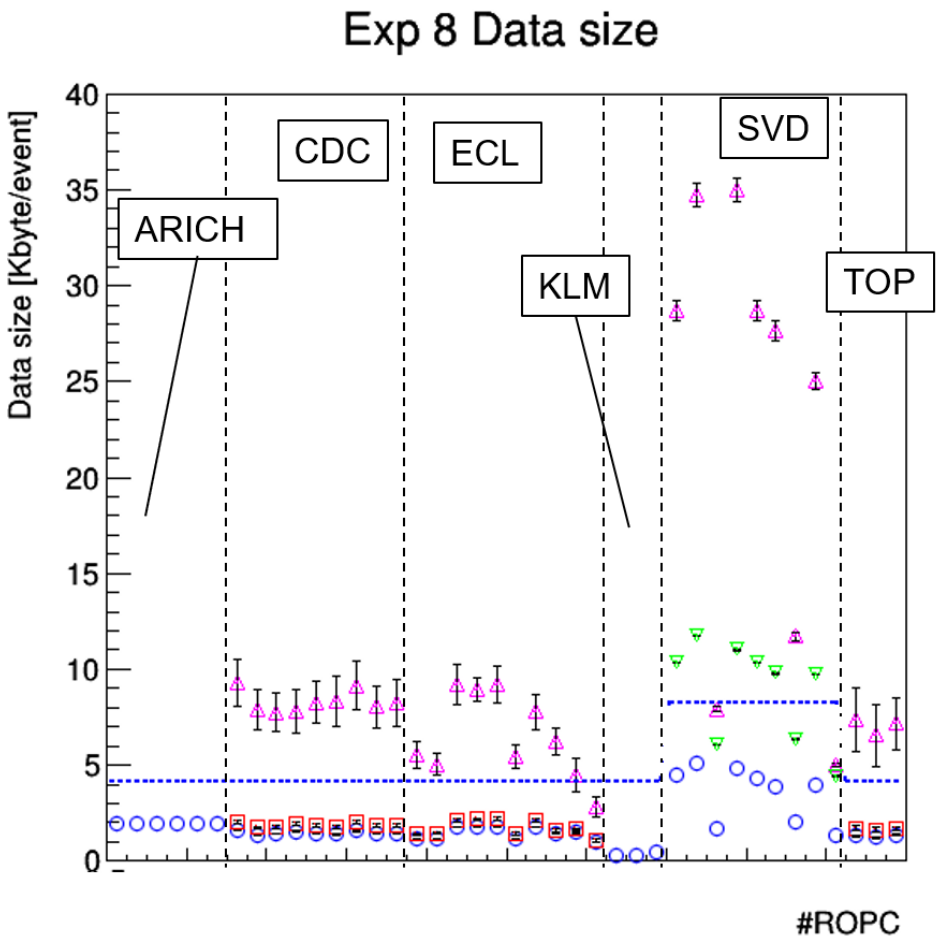


Fig. 65: The estimated data size per event for readout PCs in six sub-detectos. The blue points represent data size under luminosity and beam current equal to zero. The red points represent data size under accelerator parameters in a run (Phase 3 experiment 8 run 2549). The magenta points represent data size under target accelerator parameters in phase 3 run. For green points, the strip occupancy for all SVD layers in phase 3 run are scaled so as to have 3% layer 3 strip occupancy, and data size is calculated.

1GBit ethernet cable from SVD COPPERs can become one of data flow bottlenecks. Data size for COPPERs in the rest of sub-detectors are below potential bottlenecks of 125MB/s.

Data size for SVD readout PCs also exceed the bottleneck. In addition to SVD, data size for CDC, ECL and TOP can also exceed the 125MB/s bottleneck.

4.5 Discussion

4.5.1 Possible solution to the potential bottlenecks

For sub-detectors except for SVD, the output lines from COPPERs are not considered to be bottleneck of data flow in the future run, while output lines from readout PCs might becomes bottlenecks. It is able to solve these bottlenecks by adding readout PCs for those sub-detectors.

On the other hand, output lines from both readout PCs and COPPERs become bottlenecks. For SVD COPPERs, only one HSLB among 4 HSLBs on a COPPER board is used for data input from SVD front-end electronics. Therefore under current data readout system with COPPER boards, we need to not only add another COPPER board but also modify SVD front-end electronics to have additional Belle2links between front-end electronics and COPPER boards.

The other possible solution for this bottleneck is to develop a module which split data from one Belle2link to multiple COPPER boards. This solution also requires additional COPPER board.

4.5.2 Plan of DAQ upgrade for future run

In order to handle large data size in the future run, an upgrade plan for data acquisition system is ongoing [16].

The schematics for upgraded readout system is shown in Fig.66. In the upgraded readout system, the new readout board is connected to readout PC server via PCI Express. The data transfer rate between new readout board and readout PC server using PCI express Gen3 is 15.75GB/s. Therefore, the two potential bottlenecks, PCI bus on COPPER board and the 1GBit ethernet cable from COPPER board, is resolved by this upgrade. The output cables from readout PCs are also replaced to 10GBit ethernet cable.

The upgraded readout system has 12 time larger number of input channels. COPPER board receives data via 4 HSLB, while the new readout board accept at most 48 channels. The upgrade of network switch between readout PC and EB1 is also required. The potential bottleneck in the upgraded system is the output from readout PC using 10GBit ethernet cable. In the new readout system, we can handle more data throughput rate in one Belle2link, therefore we can solve the bottlenecks around

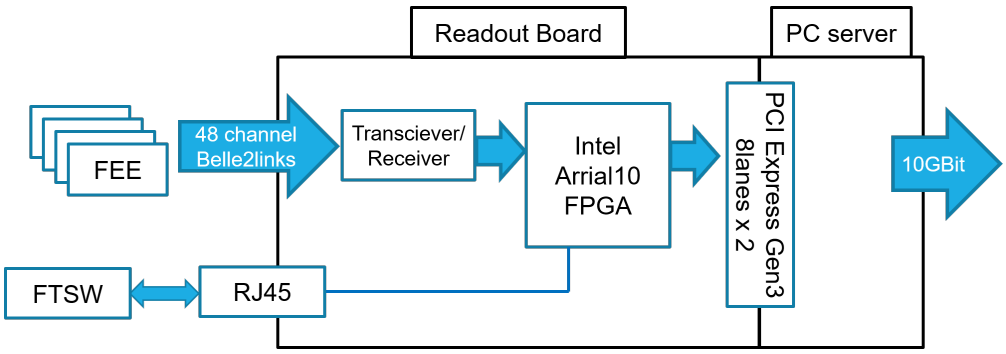


Fig. 66: The overview of upgraded readout system. The COPPER board is replaced by new readout board with 48 channel inputs. The new readout board is connected to PC server via PCI Express 3.0. The output line from PC server is upgraded from 1GBit to 10GBit ethernet cable.

COPPER boards without upgrading SVD front-end electronics.

The total event size for sub-detectors and the numbers of the new readout board required for sub-detectors are listed in Table.4.

Table 4: The expected total event size for sub-detectors under the target luminosity $\mathcal{L} = 8 \times 10^{35}$. The values in the parenthesis for SVD is assuming that SVD layer 3 occupancy is 3%.

Sub-detector	Total event size [kB/event]	Total data throughput at 30kHz [MB/s]	The necessary number of the new readout board
ARICH	11.9	357	1
CDC	74.7	2241	2
ECL	64.6	1938	2
KLM	1.4	42	1
SVD	204.1(80.0)	6123(2400)	5(2)
TOP	21.1	633	1
Total	377.8(253.7)	11334(7611)	12(9)

4.6 Summary of the data flow analysis

In this section, we analyzed the data size in phase 3 data and estimated future data size under high luminosity. For CDC, ECL, and TOP, the 1GBit output from readout PC can be bottlenecks in data flow, and these bottlenecks can be solved by adding readout PCs. On the other hand, SVD COPPERs can be the bottlenecks due to the large effect of beam background. Therefore, if we are to obtain data under target luminosity $\mathcal{L} = 8 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the reduction of beam background or upgrade of COPPERs to new readout system with large data throughput rate is necessary.

In the planned readout system upgrade, the bottlenecks due to the output line from COPPER disappear. Therefore, using at most 12 new readout board, the bottlenecks discussed in this section is thought to be solved.

5 Conclusion

In this thesis, we reported the analysis of the Belle II data acquisition system. The luminosity of the SuperKEKB accelerator is 40 times higher than that of the KEKB accelerator, therefore large data size and trigger rate are expected due to the increased beam background. The data acquisition system with more than 1GB/s data throughput is required to be operated under 1% dead time to obtain large statistics in Belle II.

In this analysis, we implemented the monitoring system for the Trigger Timing Distribution system to supervise the condition of trigger distribution. In the physics run in 2019, we observed the dead time of the data acquisition system using the TTD monitoring system and confirmed that the data acquisition system works under a sufficiently small dead time of about 0.1%. Furthermore, we found that large dead time is induced by the backpressure due to the data flow bottleneck.

To obtain as many events as possible, the data throughput rate under high luminosity must below the potential data flow bottlenecks. The future data size for sub-detectors is estimated using data taken in 2019, assuming that data size receives effect of single-beam background and luminosity dependent background. Under 30kHz and the target luminosity $\mathcal{L} = 8 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the estimated data throughput rate exceed the bottlenecks of current data acquisition system, therefore an upgrade of data acquisition system is necessary. The upgrade plan of the data acquisition system is ongoing, and we observed that the data flow bottlenecks can be solved by the new readout system.

The luminosity in the runs used in this analysis is at most $\mathcal{L} = 5 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, and this luminosity is more than 10 times smaller than the target luminosity $\mathcal{L} = 8 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. We need to analyze whether the data size extrapolation in this thesis also holds for future data size under high luminosity.

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